



1. Description

1.1. Project

Project Name	kavir_lcd_1_3
Board Name	custom
Generated with:	STM32CubeMX 6.8.0
Date	11/26/2023

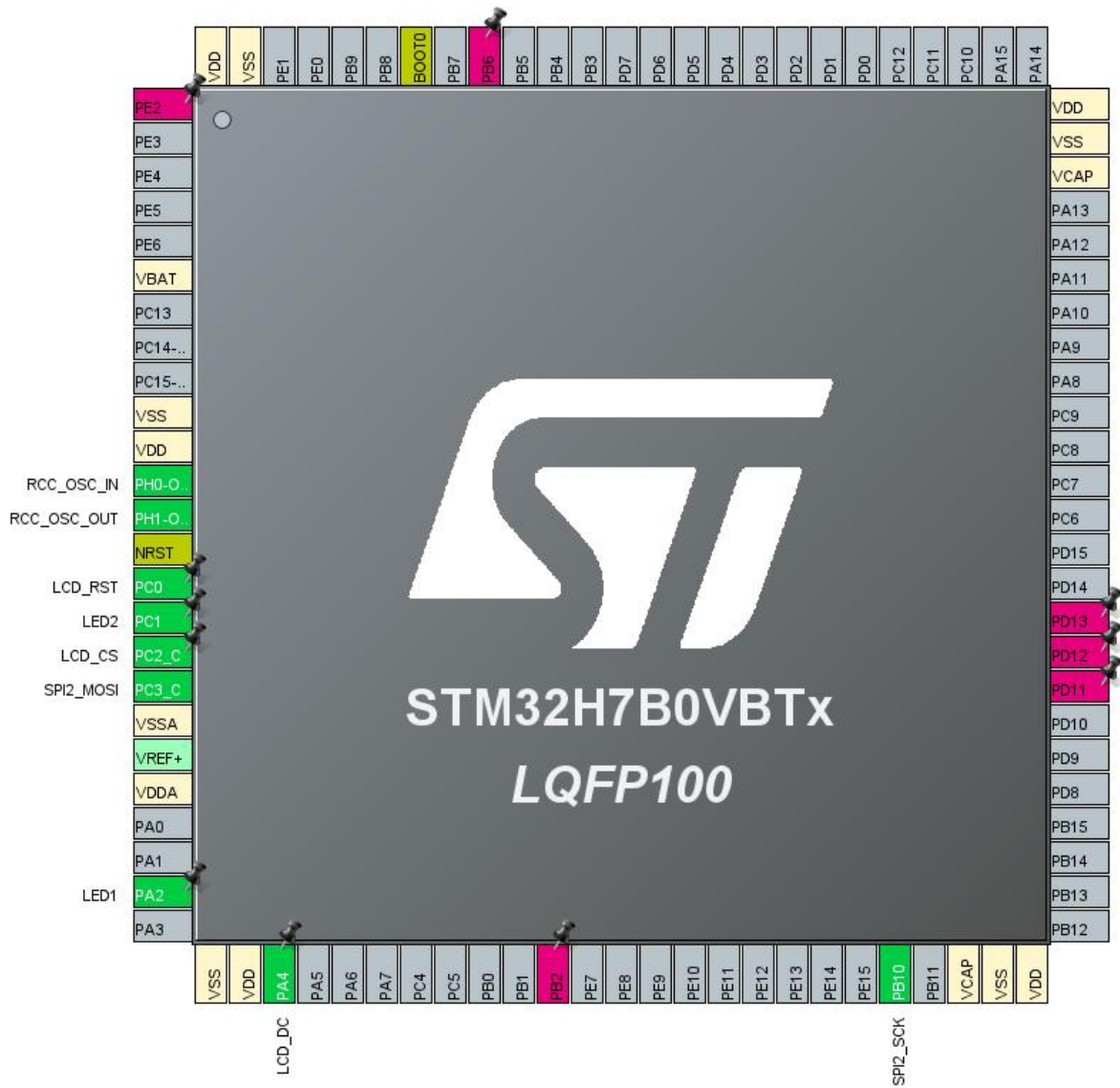
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H7B0 Value line
MCU name	STM32H7B0VBTx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M7
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2. Pinout Configuration

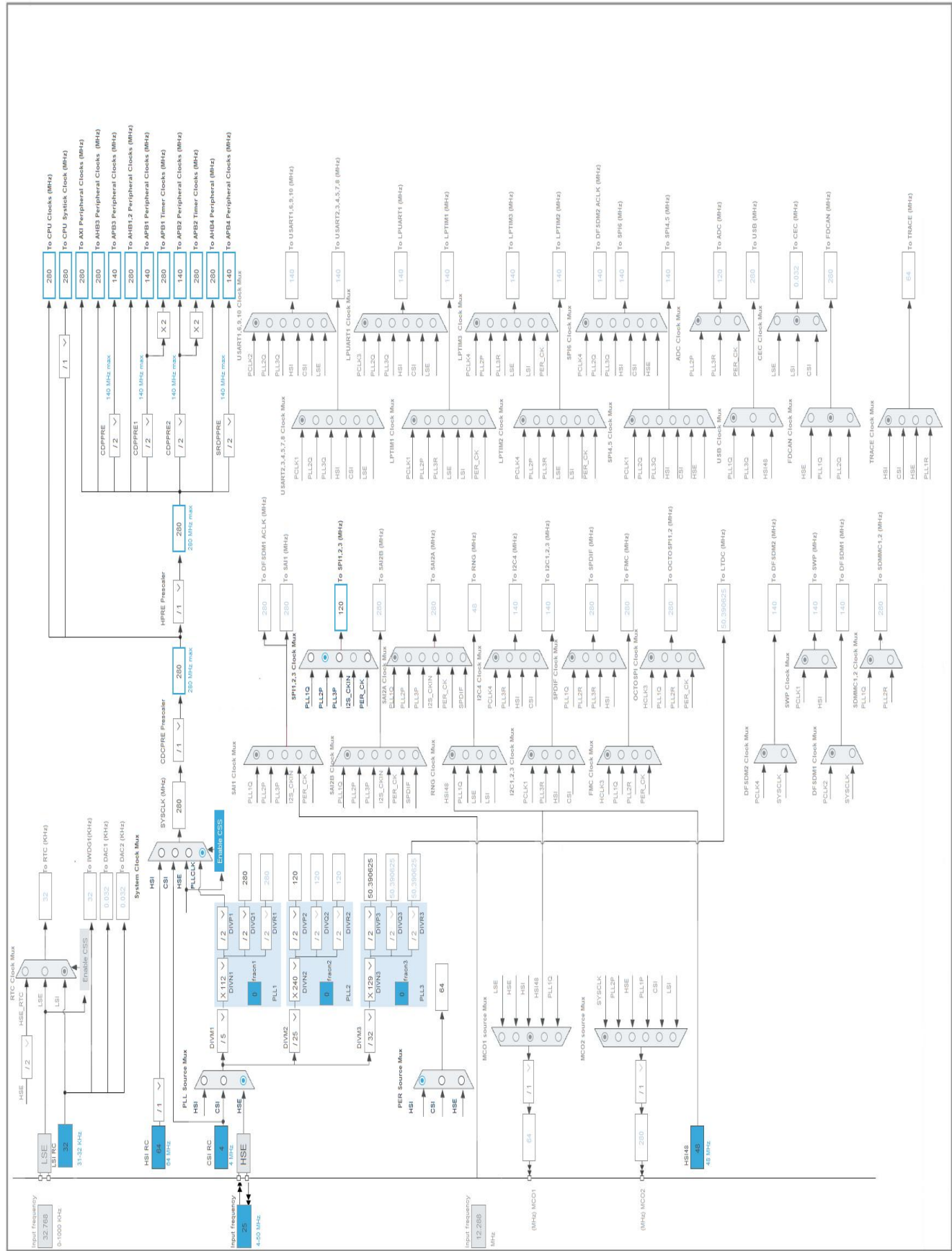


3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O		
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0 *	I/O	GPIO_Output	LCD_RST
16	PC1 *	I/O	GPIO_Output	LED2
17	PC2_C *	I/O	GPIO_Output	LCD_CS
18	PC3_C	I/O	SPI2_MOSI	
19	VSSA	Power		
21	VDDA	Power		
24	PA2 *	I/O	GPIO_Output	LED1
26	VSS	Power		
27	VDD	Power		
28	PA4 *	I/O	GPIO_Output	LCD_DC
36	PB2	I/O		
46	PB10	I/O	SPI2_SCK	
48	VCAP	Power		
49	VSS	Power		
50	VDD	Power		
58	PD11	I/O		
59	PD12	I/O		
60	PD13	I/O		
73	VCAP	Power		
74	VSS	Power		
75	VDD	Power		
92	PB6	I/O		
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	kavir_lcd_1_3
Project Folder	D:\Masoud\github_projects\240x240_lcd
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.11.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x4000
Minimum Stack Size	0x2000

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_SPI2_Init	SPI2

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H7B0 Value line
MCU	STM32H7B0VBTx
Datasheet	DS13139_Rev0

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

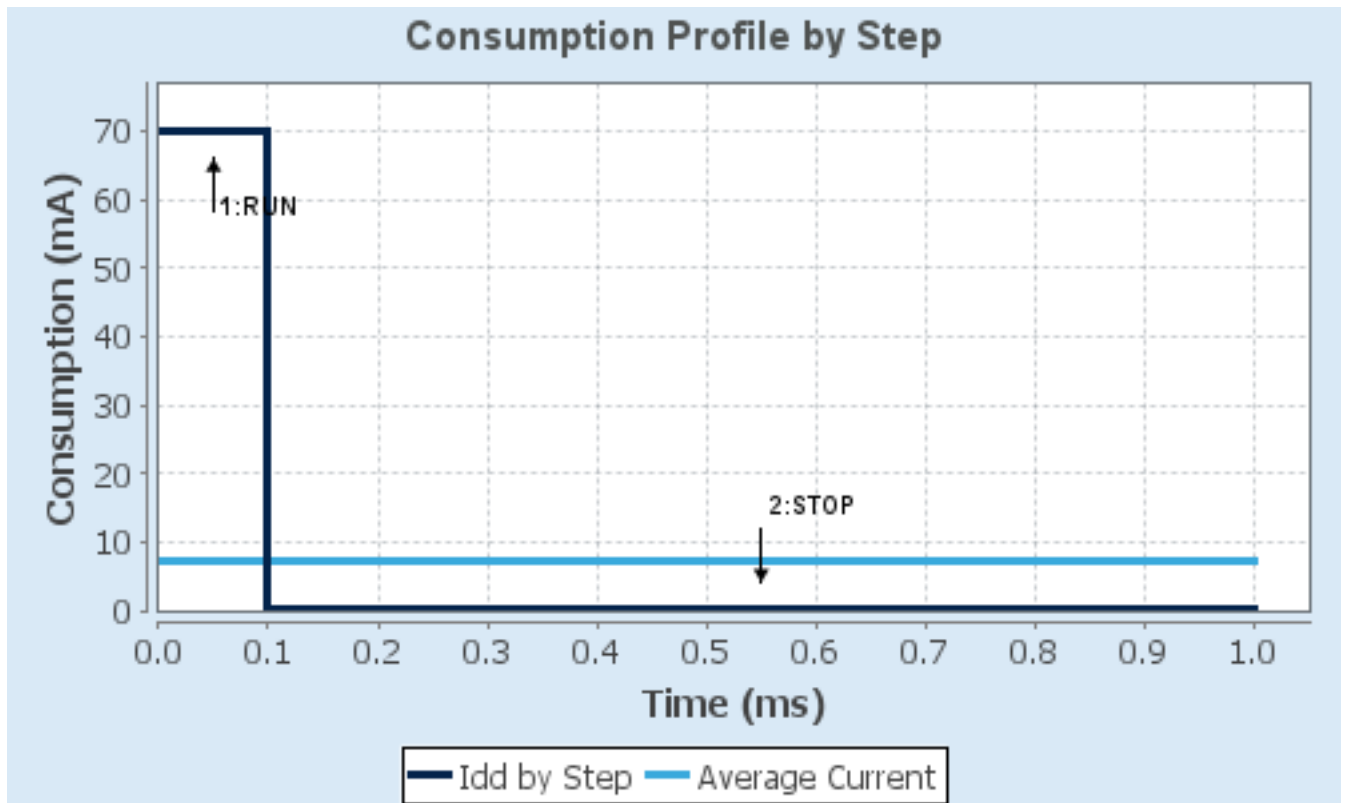
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0	SVOS5
SRDomain	DRUN	DSTOP
n/a	SRDRUN	SRDSTOP
Fetch Type	ITCM/DTCM/Cache	NA
CPU Frequency	280 MHz	64 MHz
Clock Configuration	HSE PLL	HSI Flash-ON
Clock Source Frequency	16 MHz	64 MHz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	69.92 mA	263.82 μ A
Duration	0.1 ms	0.9 ms
DMIPS	599.0	0.0
Ta Max	115.56	124.96
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	7.23 mA
Battery Life	19 days, 14 hours	Average DMIPS	599.2 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.1.1. Parameter Settings:

Power Parameters:

SupplySource	PWR_LDO_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 0

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	64

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

PLL range Parameters:

PLL1 input frequency range	Between 4 and 8 MHz
PLL2 input frequency range	Between 1 and 2 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range

7.2. SPI2

Mode: Transmit Only Master

7.2.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits *
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	4 *
Baud Rate	30.0 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.3. SYS

Timebase Source: SysTick

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI2	PC3_C	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_RST
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2
	PC2_C	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	LCD_CS
	PA2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Medium *	LCD_DC

8.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI2_TX	DMA1_Stream0	Memory To Peripheral	Low

SPI2_TX: DMA1_Stream0 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

8.3. BDMA1 configuration

nothing configured in DMA service

8.4. BDMA2 configuration

nothing configured in DMA service

8.5. MDMA configuration

nothing configured in DMA service

8.6. NVIC configuration

8.6.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
DMA1 stream0 global interrupt	true	0	0
SPI2 global interrupt	true	0	0
PVD and PVM interrupts through EXTI line	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
FPU global interrupt	unused		
HSEM1 global interrupt	unused		
ECC diagnostic Global Interrupt	unused		

8.6.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream0 global interrupt	false	true	true
SPI2 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware								
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing	Trace and Debug	Power and Thermal
BDMA1			SPI2 ✓					
BDMA2								
CORTEX_M7 ✓								
DMA ✓								
GPIO ✓								
MDMA								
IVIC ✓								
RCC ✓								
SYS ✓								

10. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32h7_bsd1.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32h7_svd.zip
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IBIS models	https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32h7_svd.zip
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