Digital Logic Design

Problem Set #4

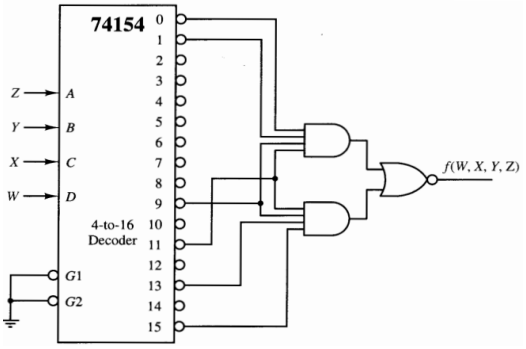
Due Date: 1400/08/19 - 23:59

1. Consider the function below *(30 points)*

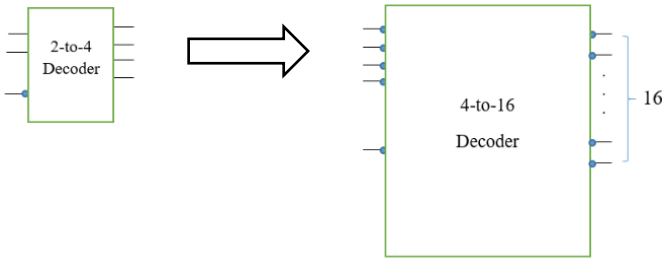
$$f(a,b,c,d) = c'd + b'd' + abc$$

   a. Draw the K-map in its current form and find all the potential hazards.
   b. Assume all gates have the same propagation delay of 4 ns. Draw the timing diagram to determine if the potential hazard 1101 ↔ 1111 leads to real hazard or not. (The literals are present in both un-complemented (a,b,c,d) and complemented (a',b',c',d') forms).
   c. Add <u>minimum</u> necessary terms to avoid all potential hazards (There's no need to draw the circuit).

2. Given the circuit in the figure below, with the decoder having active-low outputs as shown, find the minimum SOP for the function $f(W,X,Y,Z)$. *(30 points)*



3. Try to build a 4-to-16 decoder with active low inputs, active low outputs, and active low enable by cascading minimum numbers of 2-to-4 decoders with active low enable and active high inputs and outputs. Use as less extra gates as possible. *(40 points)*



Good Luck!
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Do not hesitate to ask your question
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