Digital Logic Design

Problem Set #8

Due Date: 1400/9/15

1. Implement and simulate the following circuit Using verilog gate-level coding. Remember to perform as many tests as necessary to validate the behaviour of your circuit.
    a. Problem 2 in problem set #5

Note 1: You should at least provide two Verilog files for each question: one for the module, and one for the testbench. There should be enough test cases in your testbenches to test modules for different input and output values.

Note 2: This exercise must be done individually; thus, in case of any similarities between the codes provided by the students, all of those will receive a "-200".

Note 3: Upload your codes as one zip file. Each question must be placed in a separate folder inside the zip file.

Note 4: Please name your files as below:

{Your_Last_Name}.{Your_First_Name}.{Student_Number}.{Module_Name}.v

{Your_Last_Name}.{Your_First_Name}.{Student_Number}.{Module_Name}.Testbench.v

Example: Cruise.Tom.98777777.Main.Testbench.v

Note 5: Provide a report in pdf format alongside with project files. It should contain several screenshots from your simulation waves and your descriptions about them.

Good Luck!

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Do not hesitate to ask your question
Via eeXBee@gmail.com