North South University

Department of Electrical & Computer Engineering

LAB REPORT

Course Name: **CSE231L**

Experiment No: 03

Experiment Name: **Combinational Logic Design**

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Section: 05

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Score

Remarks:

LAB-03: Combinational Logic Design

Objectives:

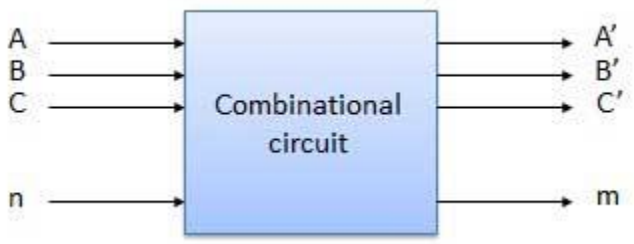
1. To familiarized with the analysis of combinational logic networks.
2. To learn the implementation of networks using the two canonical forms.

Apparatus:

- 1 x IC 4073 Triple 3-input AND gates
- 2 x IC 4075 Triple 3-input OR gates
- 1 x IC 7404 Hex Inverters (NOT gates)

Theory:

Combinational logic design: A combinational circuit consists of logic gates whose outputs at any time are determined by the current input values, i.e., it has no memory elements. The combinational logic design can be done using two methods such as a sum of products and a product of sums. Combinational logic circuits are generally designed by connecting together or combining the basic logic gates. Combinational logic gates react to the values of the signals at their inputs and produce the value of the output signal, transforming binary information from the given input data to a required output data.



Canonical forms: In Boolean algebra, Boolean function can be expressed as Canonical Disjunctive Normal Form known as min term and some are expressed as Canonical Conjunctive Normal Form known as max term.

In Min term, we look for the functions where the output results in "1" while in Maxterm we look for function where the output results in "0". We perform Sum of min term also known as Sum of products (SOP). We perform Product of Maxterm also known as Product of sum (POS).

Boolean functions expressed as a sum of min terms or product of maxterms are said to be in canonical form.

Min terms and Max terms: Min terms are AND terms with every variable present in either true or complemented form.

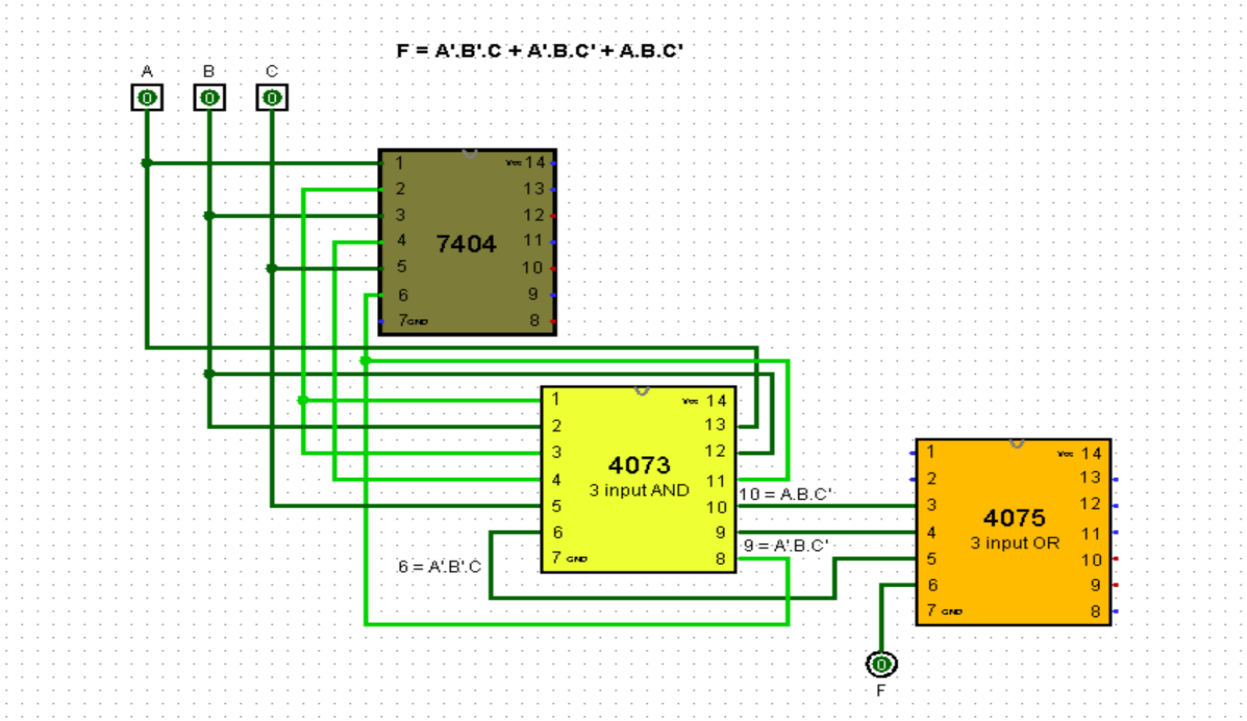
Max terms are OR terms with every variable in true or complemented form.

Truth table of Min terms and Max terms:

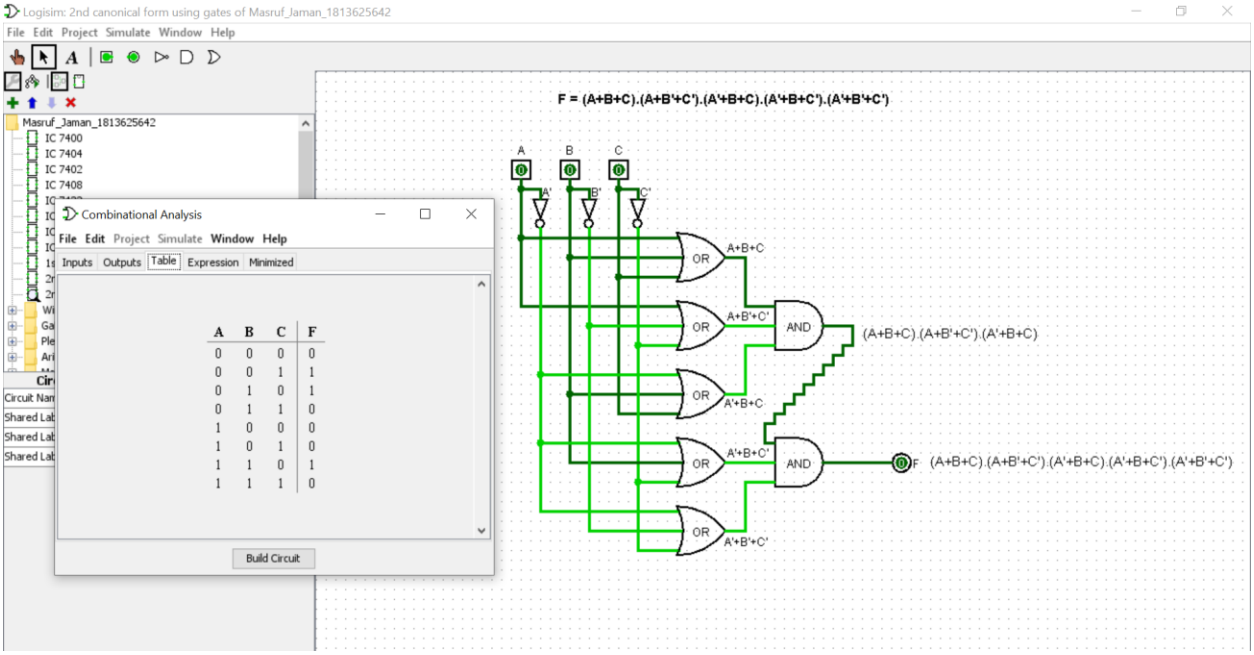
				Minterms		*Maxterms*
X	Y	Z		*Product Terms*		*Sum Terms*
0	0	0		$m_0 = \overline{X} \cdot \overline{Y} \cdot \overline{Z} = \min(\overline{X}, \overline{Y}, \overline{Z})$		$M_0 = X + Y + Z = \max(X, Y, Z)$
0	0	1		$m_1 = \overline{X} \cdot \overline{Y} \cdot Z = \min(\overline{X}, \overline{Y}, Z)$		$M_1 = X + Y + \overline{Z} = \max(X, Y, \overline{Z})$
0	1	0		$m_2 = \overline{X} \cdot Y \cdot \overline{Z} = \min(\overline{X}, Y, \overline{Z})$		$M_2 = X + \overline{Y} + Z = \max(X, \overline{Y}, Z)$
0	1	1		$m_3 = \overline{X} \cdot Y \cdot Z = \min(\overline{X}, Y, Z)$		$M_3 = X + \overline{Y} + \overline{Z} = \max(X, \overline{Y}, \overline{Z})$
1	0	0		$m_4 = X \cdot \overline{Y} \cdot \overline{Z} = \min(X, \overline{Y}, \overline{Z})$		$M_4 = \overline{X} + Y + Z = \max(\overline{X}, Y, Z)$
1	0	1		$m_5 = X \cdot \overline{Y} \cdot Z = \min(X, \overline{Y}, Z)$		$M_5 = \overline{X} + Y + \overline{Z} = \max(\overline{X}, Y, \overline{Z})$
1	1	0		$m_6 = X \cdot Y \cdot \overline{Z} = \min(X, Y, \overline{Z})$		$M_6 = \overline{X} + \overline{Y} + Z = \max(\overline{X}, \overline{Y}, Z)$
1	1	1		$m_7 = X \cdot Y \cdot Z = \min(X, Y, Z)$		$M_7 = \overline{X} + \overline{Y} + \overline{Z} = \max(\overline{X}, \overline{Y}, \overline{Z})$

Circuit Diagram:

IC diagram for the 1st canonical form of the circuit.



Simulation of the circuit for the 2nd canonical form.



Data Table:

Table 1: Truth table to a combinational circuit

Input Reference	A B C	F	Min term	Max term
0	0 0 0	0		A+B+C
1	0 0 1	1	A'.B'.C	
2	0 1 0	1	A'.B.C'	
3	0 1 1	0		A+B'+C'
4	1 0 0	0		A'+B+C
5	1 0 1	0		A'+B+C'
6	1 1 0	1	A.B.C'	
7	1 1 1	0		A'+B'+C'

Table 2: 1st and 2nd canonical forms of the combinational circuit of table 1.

	Shorthand Notation	Function
1st Canonical form	F=∑(1, 2, 6)	F = (A'.B'.C) + (A'.B.C') + (A.B.C')
2nd Canonical form	F=∏(0, 3, 4, 5, 7)	F = (A+B+C).(A+B'+C').(A'+B+C).(A'+B+C').(A'+B'+C')

Discussion: First of all, we discussed some basic theories of combinational logic design, **Canonical Form**, and **Min terms**, **Max terms**. We learn how to express the Min terms & Max terms.

Second, we fill up the minterm and max terms of the truth table of a combinational circuit that was given value in the lab manual. Then, we build **two** Canonical forms (1st on for Min term & 2nd on for Max term) according to the truth table. After made the truth table, we go to Logisim and build the two IC diagram (1st & 2nd Canonical forms) using IC 4073 Triple 3-input AND gates, IC 4075 Triple 3-input OR gates, and IC 7404 Hex Inverters (NOT gates).

At last, we implement the two canonical functions using gates. We match the truth table for all the functions.