

North South University
Department of Electrical & Computer Engineering

LAB REPORT

Course Name: **CSE231L**

Experiment No: 04

Experiment Name: **Combinational Logic Design**

Experiment Date: 01 December 2020

Report Submission Date: 08 December 2020

Section: 05

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Score

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Remarks:

LAB-04: Combinational Logic Design (BCD to Excess-3 Converter)

Objectives:

1. Design a complete minimal combinational logic system from specification to implementation.
2. Minimize combinational logic circuits using Karnaugh maps.
3. Learn various numerical representation systems.
4. Implement circuits using canonical minimal forms.

Equipment list:

- 1 x IC 4073 Triple 3-input AND gates
- 1 x IC 4075 Triple 3-input OR gates
- 1 x IC 7404 Hex Inverters (NOT gates)
- 1 x IC 7400 2-input NAND gates
- 2 x IC 7408 2-input AND gates

Theory:

K-Map: A K-map is a diagram made up of squares, with each square representing one minterm of the function that is to be minimized. In fact, the map presents a visual diagram of all possible ways a function may be expressed in standard form. By recognizing various patterns, it is possible to derive alternative algebraic expressions for the same function, from which the simplest can be selected.

BCD to Excess-3: Excess-3 is a decimal code in which each coded combination is obtained from the corresponding binary value plus 3. Excess-3 code can be derived from BCD code by adding 3 to each number.

For example, Decimal number 12 is represented as 0001 0010 in BCD. If we add 3 that is to add 0011 0011 then the corresponding Excess-3 code is 0100 0101

Circuit Diagrams:

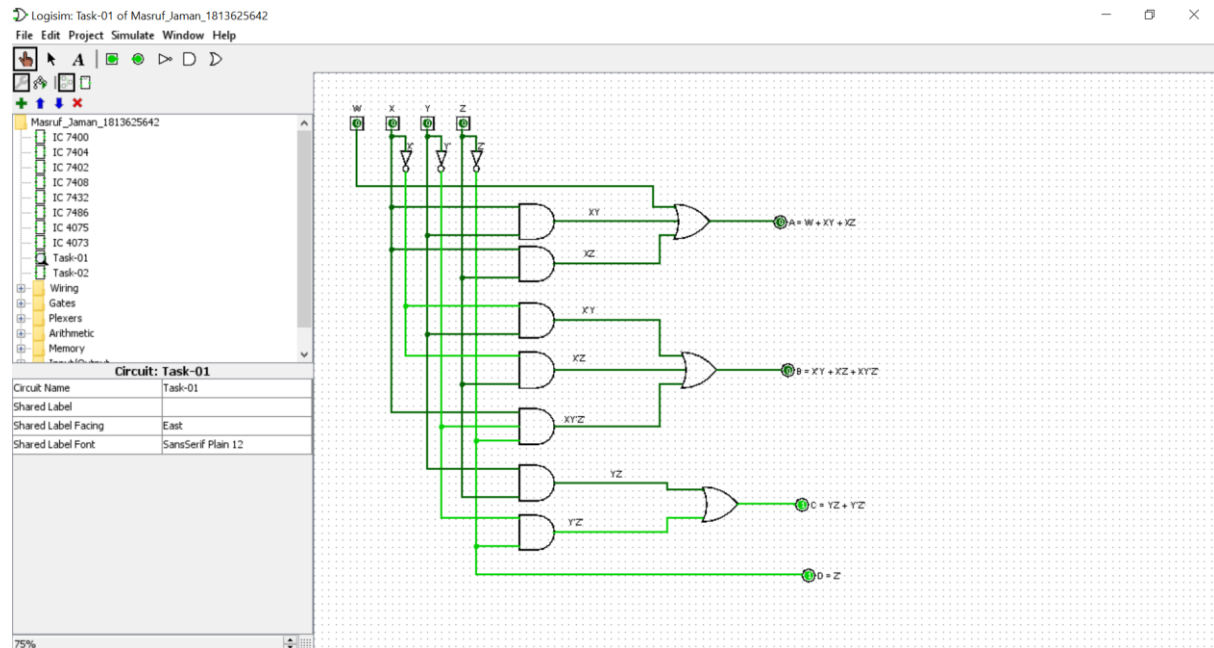


Figure F1: Minimal logic circuit of BCD to Excess-3 converter.

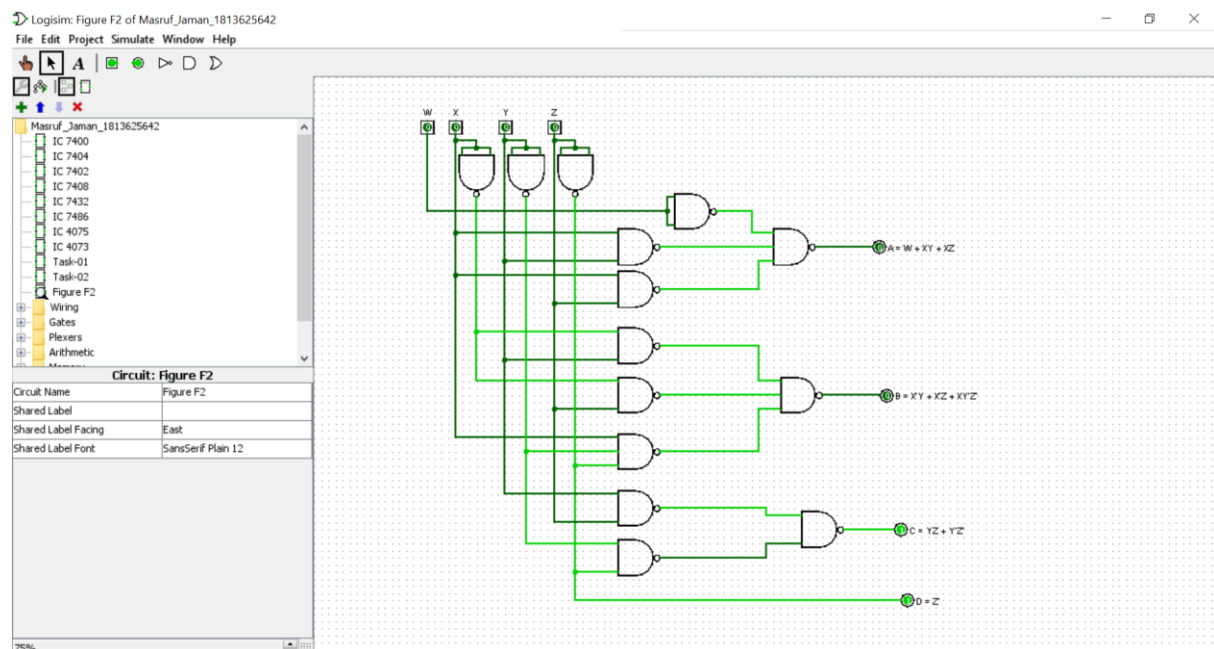


Figure F2: Minimal universal gate implementation of BCD to Excess-3 converter.

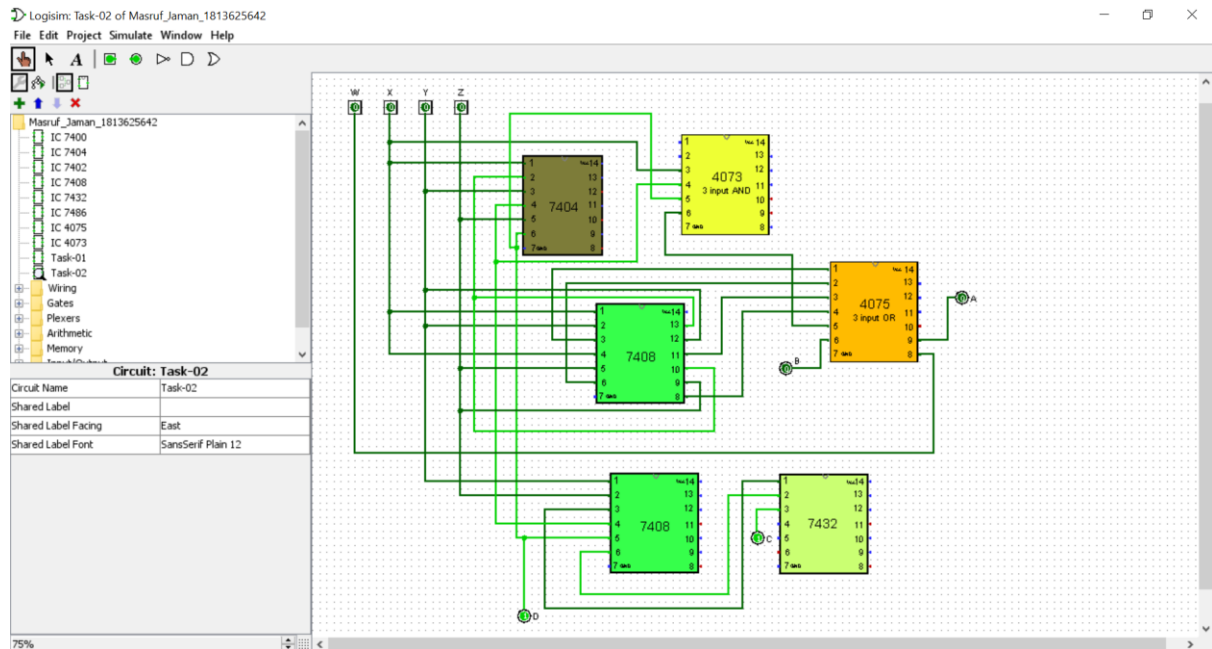


Figure F4: minimal IC implementation of BCD to Excess-3 converter.

Figure F3: K-Maps.

0	0	0	0
0	1	1	1
X	X	X	X
1	1	X	X

$$A = W + XY + XZ$$

0	1	1	1
1	0	0	0
X	X	X	X
0	1	X	X

$$B = X'Y + X'Z + XY'Z'$$

1	0	1	0
1	0	1	0
X	X	X	X
1	0	X	X

$$C = YZ + Y'Z'$$

1	0	0	1
1	0	0	1
X	X	X	X
1	0	X	X

$$D = Z'$$

Data Table:

Table 01: Truth table of the given circuit using universal gates

Decimal Digit	Binary Coded Decimal (BCD)				EXCESS-3			
	W	X	Y	Z	A	B	C	D
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

Discussion: First of all, we discussed about the K-Map, BCD to excess 3. The name of our experiment was Combinational Logic Design. Our experiment was to know about combinational logic designs and to implement them in circuit using minimal canonical form. Then I design the combinational logic circuit using k map. In this experiment I design a BCD to excess-3 converter. For this experiment, I have used Logic gates and universal gate NAND. I minimized and implemented a digital logic system where an input in binary coded decimal (BCD) is converted and displayed in Excess-3.