



North South University
Department of Electrical & Computer Engineering

LAB REPORT

Course Name: **CSE231L**

Experiment No: 06

Experiment Name: **Introduction to Multiplexers and Decoders**

Experiment Date: 15 December 2020

Report Submission Date: 28 December 2020

Section: 05

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Score

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Remarks:

LAB-06: Introduction to Multiplexers and Decoders

Objectives:

1. Understand the concept of multiplexing in the context of digital logic circuits.
2. Learn about the internal logic of digital multiplexers.
3. Implement digital logic functions using multiplexers.
4. Observe and analyze the operations of the 3 to 8 Line Decoder

Apparatus:

- 1 x IC 7404 Hex Inverter (NOT gates)
- 2 x IC 7411 3-input AND gates
- 1 x IC 7432 2-input OR gates

Theory:

Multiplexer: A multiplexer is a combinational circuit that chooses double data from one of many information lines and guides it to a solitary yield line. The determination of a specific info line is constrained by a bunch of choice lines. Typically, there are 2^n info lines and n choice lines whose bit mixes figure out which information is chosen.

Decoder: Decoder is a combinational circuit that has ' n ' input lines and maximum of 2^n output lines. One of these outputs will be active High based on the combination of inputs present, when the decoder is enabled. That means decoder detects a particular code.

Circuit Diagram:

Experiment-1:

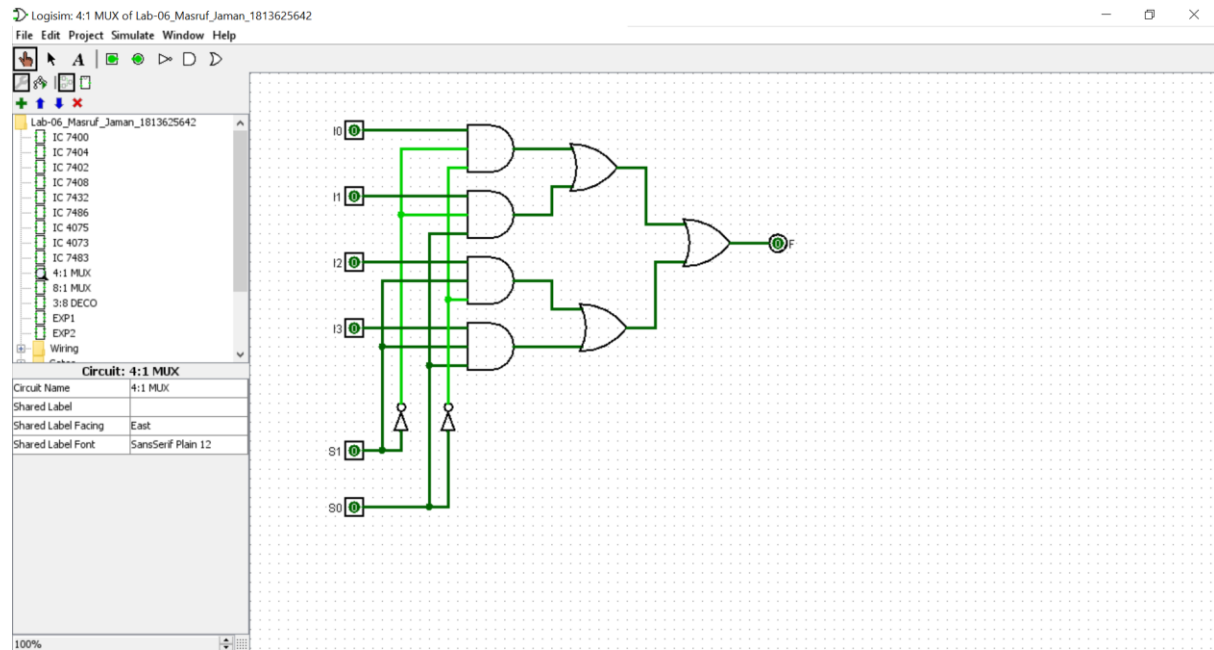


Figure 1: Constructing a 4:1 Multiplexer using basic logic gates.

Data Table:

Experiment-1:

Table 01: Truth table of the given circuit using universal gates.

A	B	C	F (Theoretical)	Data Inputs	F (Practical)
0	0	0	1	$I_0 = 1$	1
0	0	1	1		1
0	1	0	0	$I_1 = 0$	0
0	1	1	0		0
1	0	0	0	$I_2 = C$	0
1	0	1	1		1
1	1	0	0	$I_3 = C$	0
1	1	1	1		1

Table 02: Truth table for 8:1 MUX implementation for Function

$$F(A, B, C, D) = \Sigma(0, 1, 3, 5, 8, 9, 14, 15)$$

A	B	C	D	F (Theoretical)	Data Inputs	F (Practical)
0	0	0	0	1	$I_0 = 1$	1
0	0	0	1	1		1
0	0	1	0	0	$I_1 = D$	0
0	0	1	1	1		1
0	1	0	0	0	$I_2 = D$	0
0	1	0	1	1		1
0	1	1	0	0	$I_3 = 0$	0
0	1	1	1	0		0
1	0	0	0	1	$I_4 = 1$	1
1	0	0	1	1		1
1	0	1	0	0	$I_5 = 0$	0
1	0	1	1	0		0
1	1	0	0	0	$I_6 = 0$	0
1	1	0	1	0		0
1	1	1	0	1	$I_7 = 1$	1
1	1	1	1	1		1

Table 03: Truth table for 8:1 MUX implementation of report section.

For function $F(A, B, C, D) = \Sigma (1, 2, 4, 5, 10, 12, 13)$

A	B	C	D	F (Theoretical)	Data Inputs	F (Practical)
0	0	0	0	0	$I_0 = D$	0
0	0	0	1	1		1
0	0	1	0	1	$I_1 = D'$	1
0	0	1	1	0		0
0	1	0	0	1	$I_2 = 1$	1
0	1	0	1	1		1
0	1	1	0	0	$I_3 = 0$	0
0	1	1	1	0		0
1	0	0	0	0	$I_4 = 0$	0
1	0	0	1	0		0
1	0	1	0	1	$I_5 = D'$	1
1	0	1	1	0		0
1	1	0	0	1	$I_6 = 1$	1
1	1	0	1	1		1
1	1	1	0	0	$I_7 = 0$	0
1	1	1	1	0		0

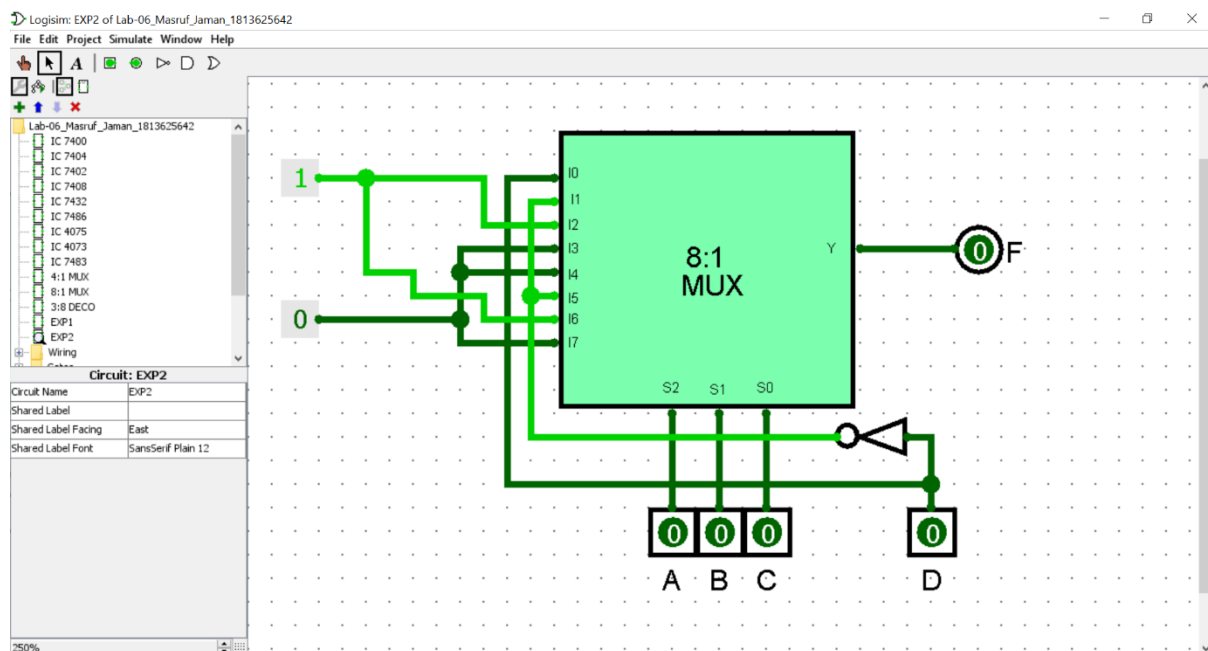
Table 04: Experimental Data of 3 to 8 Line Decoder.

Select Inputs			Outputs							
A	B	C	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Question and Answer:

Experiment-2:

Figure F2: IC Simulation diagram for the implementation of function $F(A, B, C, D) = \sum (1, 2, 4, 5, 10, 12, 13)$ using IC74151.



Experiment-3:

Ques: Difference between active-high and active-low device:

The line is used to represent NOT (also known as bar). When something is NOTTED, it changes to the opposite state. So if an active-high input is NOTTED, then it is now active-low.

Ans: *Active-High Device:* An active high device is a gadget that either yield a HIGH sign when set-off on or that acknowledges a high sign as a contribution to turning on. It truly relies upon whether the gadget is an information or a yield gadget.

Ans: *Active-Low Device:* An active low device is a gadget that either yield 0V, when set off on or that, acknowledges 0V as a contribution to turn on. It truly relies upon whether the gadget is info or a yield gadget

Discussion: The name of our experiment was Introduction to Multiplexers and Decoders. We covered the topic Multiplexers and Decoders in this experiment. we build 4:1mux, 8:1mux. In first experiment we constructed a 4:1 Multiplexer using basic logic gates. And in our second experiment we did IC Simulation diagram for the implementation of function $F(A, B, C, D) = \sum (1, 2, 4, 5, 10, 12, 13)$ using 8:1mux. And also, for this function $F(A, B, C, D) = \sum (0, 1, 3, 5, 8, 9, 14, 15)$. In our third or last experiment we know about active-high and active-low device.