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| G:\nsu-logo.png  **North South University**  Department of Electrical & Computer Engineering    **LAB REPORT**  Course Name: **CSE231L**  Experiment No: 04     |  | | --- | | Experiment Name: **Combinational Logic Design** |   Experiment Date: 24 November 2020  Report Submission Date: 28 November 2020  Section: 05 | |
| Student Name:Md. Masruf Jaman | Score |
| Student ID: **1813625642** |  |
| Remarks: |

**LAB-04: Combinational Logic Design (BCD to Excess-3 Converter)**

**Objectives:**

1. Design a complete minimal combinational logic system from specification to implementation.
2. Minimize combinational logic circuits using Karnaugh maps.
3. Learn various numerical representation systems.
4. Implement circuits using canonical minimal forms.

**Equipment list:**

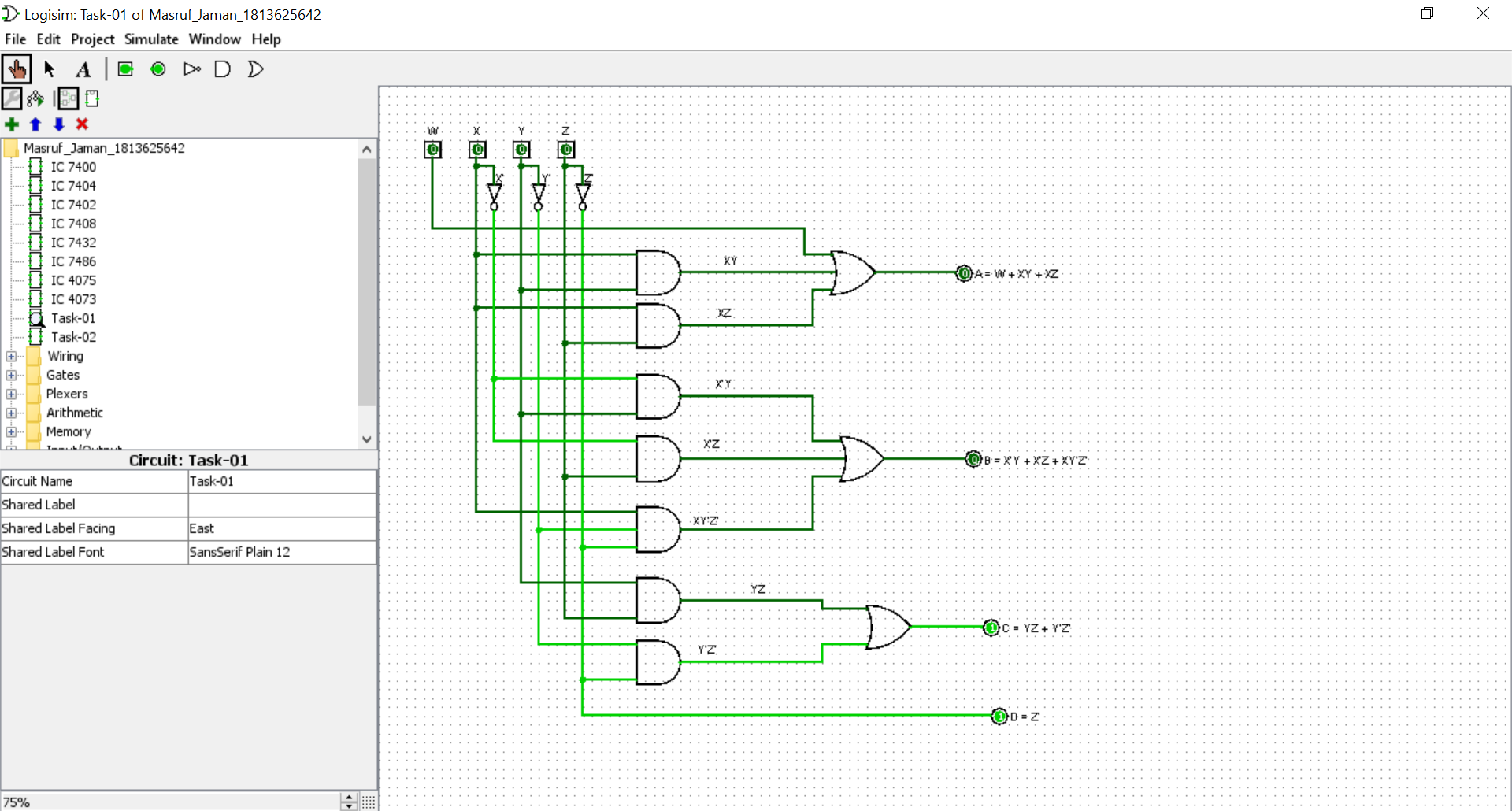
* 1 x IC 4073 Triple 3-input AND gates
* 1 x IC 4075 Triple 3-input OR gates
* 1 x IC 7404 Hex Inverters (NOT gates)
* 1 x IC 7400 2-input NAND gates
* 2 x IC 7408 2-input AND gates

**Theory:**

1. **Map:**

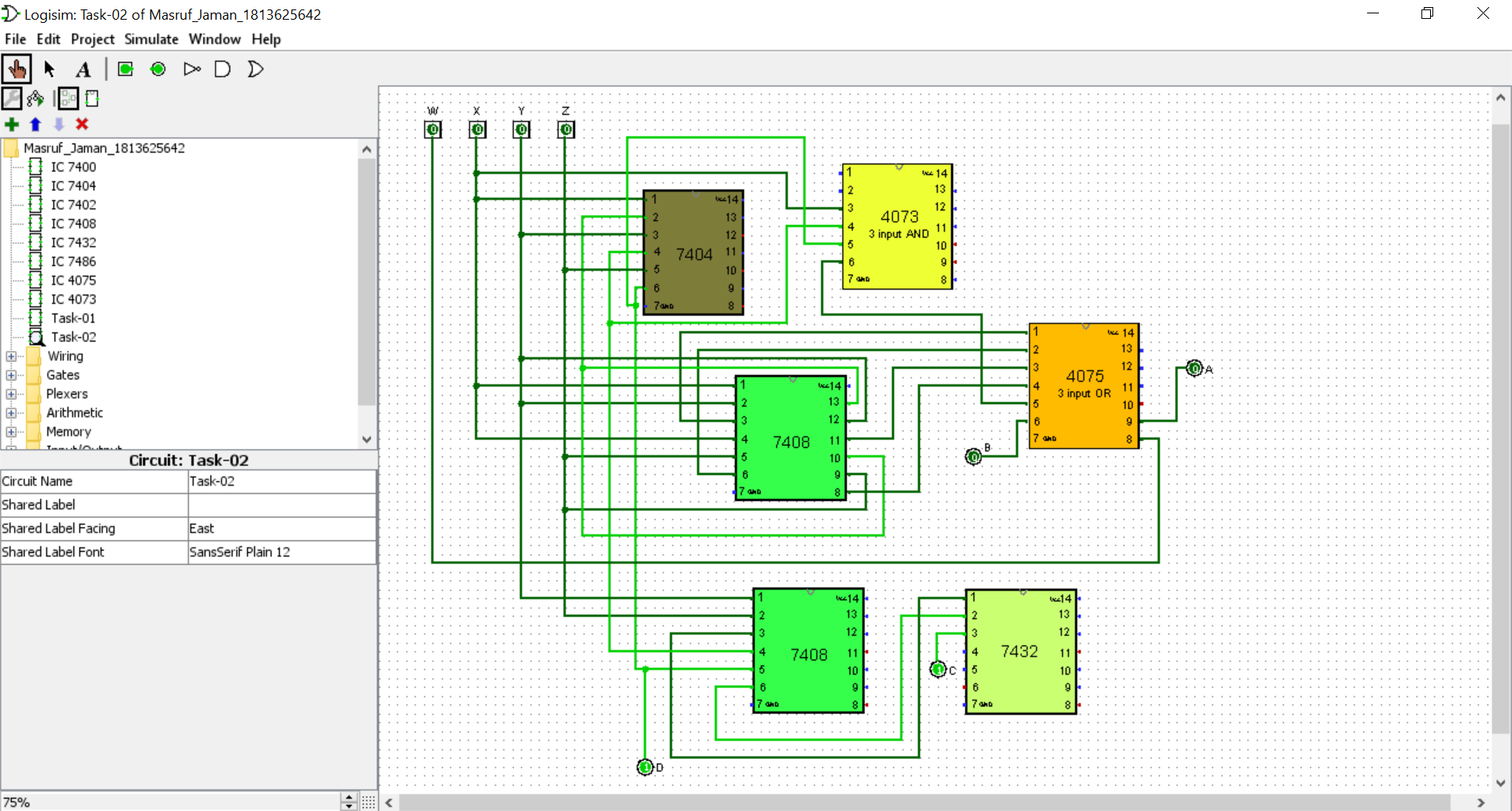
**BCD to Excess-3**

**Circuit Diagrams:**

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**Figure F1: Minimal logic circuit of BCD to Excess-3 converter.**

**Figure F2: Minimal universal gate implementation of BCD to Excess-3 converter.**

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**Figure F4: minimal IC implementation of BCD to Excess-3 converter.**

**Figure F3: K-Maps.**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **0** | **0** | **0** | **0** |  | **0** | **1** | **1** | **1** |
| **0** | **1** | **1** | **1** | **1** | **0** | **0** | **0** |
| **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** |
| **1** | **1** | **X** | **X** | **0** | **1** | **X** | **X** |

**A = W + XY +XZ B = X’Y + X’Z + XY’Z’**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **1** | **0** | **1** | **0** |  | **1** | **0** | **0** | **1** |
| **1** | **0** | **1** | **0** | **1** | **0** | **0** | **1** |
| **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** |
| **1** | **0** | **X** | **X** | **1** | **0** | **X** | **X** |

**C = YZ + Y’Z’ D = Z’**

**Data Table:**

**Table 01: Truth table of the given circuit using universal gates**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Decimal Digit** | **Binary Coded Decimal (BCD)** | | | | **EXCESS-3** | | | | |
| **W** | **X** | **Y** | **Z** | **A** | **B** | **C** | **D** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** |
| **1** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **0** |
| **2** | **0** | **0** | **1** | **0** | **0** | **1** | **0** | **1** |
| **3** | **0** | **0** | **1** | **1** | **0** | **1** | **1** | **0** |
| **4** | **0** | **1** | **0** | **0** | **0** | **1** | **1** | **1** |
| **5** | **0** | **1** | **0** | **1** | **1** | **0** | **0** | **0** |
| **6** | **0** | **1** | **1** | **0** | **1** | **0** | **0** | **1** |
| **7** | **0** | **1** | **1** | **1** | **1** | **0** | **1** | **0** |
| **8** | **1** | **0** | **0** | **0** | **1** | **0** | **1** | **1** |
| **9** | **1** | **0** | **0** | **1** | **1** | **1** | **0** | **0** |

**Discussion:**