



# **Utility Bus Split**

DS484 December 2, 2005

#### **Product Specification**

#### Introduction

The Utility Bus Split core is designed to be used with Platform Studio to split a bus into smaller buses.

The core takes one input bus and splits it into two output buses and serve as glue logic between peripherals.

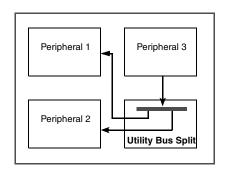


Figure 1: Utility Bus Split in a System

#### **Features**

The Split Operation has the following features:

Configurable size of the input and output vectors

LogiCORE™ Facts			
Core Specifics			
Supported Device Family	Virtex-II, S Spartan-IIE Spartan-3E, \	rtex™-II, QPro partan™-II, i, Spartan-3, /irtex, Virtex-II, irtex-4, Virtex-E	
Version of Core	util_bus_split v1.00a		
Re	esources Used		
	Min	Max	
Slices	0	0	
LUTs	0	0	
FFs	0	0	
Block RAMs	0	0	
Provided with Core			
Documentation	Product Specification		
Design File Formats	VHDL		
Constraints File	N	//A	
Verification	N	//A	
Instantiation Template	N/A		
Reference Designs	No	one	
Design Tool Requirements			
Xilinx Implementation Tools	5.1i or later		
Verification	N/A		
Simulation	ModelSim SE/	PE 5.7b or later	
Synthesis	Х	ST	
Support			
Support provided by Xilinx, Inc.			

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## **Utility Bus Split Parameters**

Table 1: Utility Bus Split Parameters

Parameter	Description	Default value	Туре
C_SIZE_IN	The vector size of input bus.	8	integer
C_LEFT_POS	The left bit position of the Out1 output bus. The maximum value of C_LEFT_POS is C_SPLIT-1.	0	integer
C_SPLIT	First bit of the Out2 output bus	4	integer
	The minimum value of C_SPLIT is 1. The maximum value of C_SPLIT is C_SIZE_IN-1.		

#### **Allowable Parameter Combinations**

The only restrictions between parameters is that C\_LEFT\_POS must be smaller than C\_SPLIT, and both of them must be smaller than C\_SIZE\_IN.

## **Utility Bus Split I/O Signals**

Table 2: Utility Bus Split I/O Signals

Signal	Interface	I/O	Description
Sig	None	I	Input bus
Out1	None	0	Output bus1 after split
Out2	None	0	Output bus2 after split

## **Parameter-Port Dependencies**

Table 3: Port and parameter dependencies

Name	Affects	Depends	Relationship Description			
Design Param	Design Parameters					
C_SIZE_IN	Sig	0 to C_SIZE_IN-1	Scale width of input bus			
C_SIZE_IN	Out2	C_SPLIT to C_SIZE_IN-1	Least <sup>1</sup> significant bit of Out2 bus			
C_LEFT_POS	Out1	C_LEFT_POS to C_SPLIT-1	Most <sup>1</sup> significant bit of Out1 bus			
C_SPLIT	Out1	C_LEFT_POS to C_SPLIT-1	Least <sup>1</sup> significant bit of Out1 bus			
C_SPLIT	Out2	C_SPLIT to C_SIZE_IN-1	Most <sup>1</sup> significant bit of Out2 bus			
Port Signals						
Sig		C_SIZE_IN	Scale width of input bus			
Out1		C_LEFT_POS	Most <sup>1</sup> significant bit of Out1 bus			
Out1		C_SPLIT	Least <sup>1</sup> significant bit of Out1 bus			
Out2		C_SPLIT	Most <sup>1</sup> significant bit of Out2 bus			
Out2		C_SIZE_IN	Least <sup>1</sup> significant bit of Out2 bus			

<sup>1.</sup> Assuming reverse big-endian bit ordering



## **Utility Bus Split Register Descriptions**

There are no registers in this core.

### **Utility Bus Split Interrupt Descriptions**

There are no interrupts associated with this core.

## **Utility Bus Split Block Diagram**

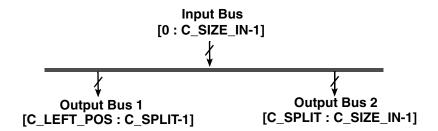


Figure 2: Utility Bus Split Block Diagram

## **Design Implementation**

#### **Design Tools**

The Utility Bus Split design is handwritten.

Xilinx XST is the synthesis tool used for synthesizing the Utility Bus Split.

### **Target Technology**

The intended target technology is an FPGA in one of the following families: QPro-R Virtex-II, QPro Virtex-II, Spartan-II, Spartan-IIE, Spartan-3, Virtex, Virtex-II, Virtex-II Pro, Virtex-4, or Virtex-E

#### **Device Utilization and Performance Benchmarks**

This core does not contain any logic. There are no performance benchmarks available.

## **Specification Exceptions**

Not applicable.

#### **Reference Documents**

None.

# **Revision History**

Date	Version	Revision
03/28/03	1.0	Revision History added to document.
12/19/03	1.1	Added LogiCORE Facts table. Reformatted to current Xilinx template.
7/15/04	1.2	Minor corrections and updates.
8/17/04	1.3	Updated for EDK 6.3. Updated trademarks and supported family device listing.
9/20/04	1.4	Corrected C_LEFT_POS description in parameter table. Updated to new data sheet template
12/2/05	1.5	Added Spartan-3E to supported device families listing.