

## Archit Gajjar

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CONTACT INFO	Address: Delta Annex (DA#32), 2700 Bay Area Blvd. Houston, Texas 77058 Email: architgajjar8464@gmail.com / GajjarA@uhcl.edu Web: www.architgajjar.com	
RESEARCH INTERESTS	<ul style="list-style-type: none"><li>• Approximate Design on Fog/Edge System</li><li>• Energy-Quality (E-Q) Tradeoff on ASIC/FPGA Design</li><li>• IoT Mesh Technology</li></ul>	
EDUCATION	<b>University of Houston - Clear Lake</b> , Houston, TX M.S., Computer Engineering	Expected: December 2018 <b>GPA: 3.94/4.00</b>
	<b>Dhirubhai Ambani Institute of Information and Communication Technology</b> , Gujarat, India B.Tech., Information and Communication Technology	2016 GPA: 5.62/10.00
WORK EXPERIENCE	<b>Research &amp; Teaching Assistant</b> CENG3316 Electronics & CENG3116 Lab for Electronics & CENG5534 ADSD Department of Engineering University of Houston Clear Lake ( <b>UHCL</b> )	August 2017 – Present
	<b>System Developer Intern</b> Inweon IT Innovations Pvt. Ltd. Greater Noida, India Using Visual Studio and OpenCV, a code was developed to find the length of rice from the provided image. Later, Raspberry pi micro-controller was set up to perform the code remotely.	May 2015 – October 2015
	<b>Intern</b> QX KPO Services Pvt. Ltd. Ahmedabad, India For one month, gained knowledge about OSI (Open Systems Interconnection) model in the field of network and communication along with practical implementation.	December 2014 – January 2015
SKILLS	<b>Programming Languages:</b> <ul style="list-style-type: none"><li>• Verilog, VHDL, Python, C, C++</li></ul> <b>Tools:</b> <ul style="list-style-type: none"><li>• Arduino, Keil, LTSpice, Raspberry Pi, Beagle Bone Black, OpenCV, Vim, Latex, FPGA, NI Multisim, ModelSim, MATLAB, Vivado</li></ul>	
PUBLICATIONS	<ul style="list-style-type: none"><li>• <b>A. Gajjar</b>, X. Yang, etc., "An FPGA Synthesis of Face Detection Algorithm using HAAR Classifiers," Intl. Conference on Algorithms, Computing and Systems (ICACS2018), Under Review, 2018.</li><li>• X. Yang, L. Wu, <b>A.Gajjar</b> etc., "A Vision of Fog Systems with Integrating FPGAs and BLE Mesh Network," Intl. Conference on Algorithms, Computing and Systems (ICACS2018), Under Review, 2018.</li><li>• Y. Zhang, X. Yang, <b>A. Gajjar</b>, etc., "Exploring Slice-Energy Saving on An Video Processing FPGA Platform with Approximate Computing," Journal of Image and Graphics (ISSN: 2301-3699) (JIG) , In Press, March, 2018.</li></ul>	

	<ul style="list-style-type: none"> <li>• Y. Zhang, X. Yang, <b>A. Gajjar</b>, etc., "Hierarchical Synthesis of Approximate Multiplier Design for Field-Programmable Gate Arrays (FPGA)-CSRmesh System," Intl. Journal of Compt. Applications (IJCA), Vol. 180, No. 17 PP. 1-7, Feb. 2018.</li> <li>• <b>A. Gajjar</b>, Y. Zhang, and X. Yang , "Demo Abstract: A Smart Building System Integrated with An Edge Computing Algorithm and IoT Mesh Networks," The Second ACM/IEEE Symposium on Edge Computing (SEC2017), Article No. 35, Oct. 2017. (doi&gt;10.1145/3132211.3132462).</li> </ul>
EVENT PRESENTATIONS	<ul style="list-style-type: none"> <li>• <b>A. Gajjar</b>, X. Yang, "Poster presentation – A Smart Home/Building System Integrated with An Edge Computing Algorithm and CSRmesh Networks," Houston Robotics and AI Day, July, 2017.</li> <li>• <b>A. Gajjar</b>, X. Yang, "Poster presentation – A Wide Area IoT Mesh Network With Edge Computing," IEEE Innovation and Automation Conference, Guilruth ctr., NASA., October, 2017.</li> </ul>
ACADEMIC PROJECTS	<ul style="list-style-type: none"> <li>• <b>Low Cost Security System Using Off the Shelf Components</b> January 2016 – April 2016 A security system capturing image of an intruder and informing to the designated person.</li> <li>• <b>Research Intern</b> May 2016 – July 2016 Gained knowledge of Cadence Encounter, tickle files, optimization.</li> <li>• <b>Surveillance Bot</b> January 2015 – April 2015 A live video stream from a manually controlled surveillance robot.</li> <li>• <b>5-Stage Pipeline processor</b> July 2014 – November 2014 Basic 5-stage pipelined processor development.</li> </ul>
HONORS AND AWARDS	<ul style="list-style-type: none"> <li>• Phi Kappa Phi Honor Society Invitation, UHCL, March, 2018</li> <li>• Research/Teaching Assistant Scholarship, UHCL, 2017-2018</li> <li>• NSF Student Travel Grant Award from SEC, 2017</li> <li>• Leadership Honor, Omicron Delta Kappa(ODK), Hilary Jo Karp Circle Honor Society, November 2017</li> </ul>
VOLUNTEER EXPERIENCE	<ul style="list-style-type: none"> <li>• Graduate Student Ambassador, College of Science &amp; Engineering, UHCL 2018</li> <li>• International Orientation Leader, UHCL 2017</li> <li>• IEEE Member 2013 – Present <ul style="list-style-type: none"> <li>– Leader of Special Interest Group on Microcontrollers, IEEE SB DA-IICT</li> <li>– I'Fest, Mentor, IEEE SB DAIICT</li> <li>– TENSYPMP'15 Volunteer, Region 10 IEEE International Conference, India</li> <li>– I'Fest, Event Coordinator</li> <li>– Teaching Assistant, Workshop on Embedded System and Arduino, PDPU, India</li> </ul> </li> <li>• Hostel Management Committee 2013 – 2015</li> <li>• Anti-Ragging Committee 2015 – 2016</li> </ul>