Archit Gajjar

CONTACT INFO
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RESEARCH INTERESTS
- Approximate Design on Fog/Edge System
- Energy-Quality (E-Q) Tradeoff on ASIC/FPGA Design
- VLSI, ASIC/FPGA, IoT, Embedded Systems hardware design

EDUCATION

University of Houston - Clear Lake, Houston, TX — Expected: December 2018
M.S., Computer Engineering — **GPA: 3.9/4.0**
- Thesis: Towards a Novel Edge Computing Platform Integrated with FPGA and IoT mesh Network: A Case Study of a Smart System
- Advisor: Xiaokun Yang, Ph.D.

Dhirubhai Ambani Institute of Information and Communication Technology, Gujarat, India — 2016
B.Tech., Information and Communication Technology — GPA: 5.6/10.0
- Project: Low-Cost Security System Using Off the Shelf Components
- Advisor: Biswajit Mishra, Ph.D.

WORK EXPERIENCE

Research & Teaching Assistant — August 2017 – Present
Electronics, Lab for Electronics, Advanced Digital System Design, Computer Architecture & Lab for Computer Architecture
Department of Engineering
University of Houston Clear Lake **(UHCL)**

System Developer Intern — May 2015 – October 2015
Inweon IT Innovations Pvt. Ltd. Greater Noida, India
Using Visual Studio and OpenCV, a code was developed to find the length of rice from the provided image. Later, Raspberry pi micro-controller was set up to perform the code remotely.

Intern — December 2014 – January 2015
QX KPO Services Pvt. Ltd. Ahmedabad, India
For one month, gained knowledge about OSI (Open Systems Interconnection) model in the field of network and communication along with practical implementation.

SKILLS

Programming Languages:
- Verilog, VHDL, Python, C, C++

Tools:
- Arduino, Keil, LTSpice, Raspberry Pi, Beagle Bone Black, OpenCV, Vim, Latex, FPGA, NI Multisim, ModelSim, MATLAB, Xilinx ISE, Vivado

PUBLICATIONS
- **A. Gajjar**, X. Yang , et al., "Mesh-IoT Based System For Large-Scale Environment," 5th Annual Conf. on Computational Science & Computational Intelligence (CSCI2018), Under Review, 2018.

- X. Yang, L. Wu, **A. Gajjar**, et al., "A Vision of Fog Systems with Integrating FPGAs and BLE Mesh Network," Journal of Communications (ISSN: 1796-2021), Accepted, In Press, 2018.
- **A. Gajjar**, X. Yang, et al., "An FPGA Synthesis of Face Detection Algorithm using HAAR Classifiers," Intl. Conference on Algorithms, Computing, and Systems (ICACS2018), PP.133-137, July 27-29, Beijing China, 2018.
- Y. Zhang, X. Yang, **A. Gajjar**, et al., "Exploring Slice-Energy Saving on An Video Processing FPGA Platform with Approximate Computing," Intl. Conference on Algorithms, Computing, and Systems (ICACS2018), PP.138-143, July 27-29, Beijing China, 2018.
- Y. Zhang, X. Yang, **A. Gajjar**, et al., "Hierarchical Synthesis of Approximate Multiplier Design for Field-Programmable Gate Arrays (FPGA)-CSRmesh System, Intl. Journal of Compt. Applications (IJCA), Vol. 180, No. 17 PP. 1-7, Feb. 2018.
- **A. Gajjar**, Y. Zhang, and X. Yang, Demo Abstract: A Smart Building System Integrated with An Edge Computing Algorithm and IoT Mesh Networks, The Second ACM/IEEE Symposium on Edge Computing (SEC2017), Article No. 35, Oct. 2017.

Event Presentations

- X. Yang, Y. Zhang, **A. Gajjar**, H. Schmoyer, and N. Ly, "Learning-on-Chip: Facial Detection with Approximations of FPGA Computing," 2018 Robotics & AI Day, UHCL, August 2018.
- **A. Gajjar**, X. Yang, Poster presentation A Wide Area IoT Mesh Network With Edge Computing, IEEE Innovation and Automation Conference, Gilruth ctr., NASA., October 2017.
- **A. Gajjar**, X. Yang, Poster presentation A Smart Home/Building System Integrated with An Edge Computing Algorithm and CSRmesh Networks, Houston Robotics and AI Day, July 2017.

Academic Projects

- **Low Cost Security System Using Off the Shelf Components** January 2016 – April 2016
  A security system capturing image of an intruder and informing to the designated person.
- **Research Intern** May 2016 – July 2016
  Gained knowledge of Cadence Encounter, tickle files, optimization.
- **Surveillance Bot** January 2015 – April 2015
  A live video stream from a manually controlled surveillance robot.
- **5-Stage Pipeline processor** July 2014 – November 2014
  Basic 5-stage pipelined processor development.

Honors and Awards

- Member, The National Society of Leadership and Success, August 2018 (Invited)
- Research Scholarship Award ($1300), Dr. Ted Leibfried Legacy, UHCL, July 2018 (2/100 Students)
- Graduate Student Ambassador, College of Science & Engineering, UHCL (2 Students out of CENG Program) 2018
- Member, Phi Kappa Phi Honor Society, UHCL, April 2018 (Invited)
- Research/Teaching Assistant Scholarship, UHCL, 2017-2018
- NSF Student Travel Grant Award ($800), SEC, 2017
- Leadership Honor, Omicron Delta Kappa(ODK), Hilary Jo Karp Circle Honor Society, November 2017

Volunteer Experience

- Secretary, Executive Officer, IEEE SB UHCL — 2018
- International Student Orientation Leader, UHCL — 2017 & 2018
- IEEE Member — 2013 – Present
  - Leader of Special Interest Group on Microcontrollers, IEEE SB DA-IICT
  - I'Fest, Mentor, IEEE SB DAIICT
  - TENSYMP'15 Volunteer, Region 10 IEEE International Conference, India
  - I'Fest, Event Coordinator
  - Teaching Assistant, Workshop on Embedded System and Arduino, PDPU, India

References

- References are available on request.