Archit **Gajjar**

Ph.D. Student · Computer Engineering

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Education

North Carolina State University (NCSU) — *Raleigh, NC*

Ph.D. - Computer Engineering — *Aug. 2019 - May 2024*

Advisor: Paul Franzon, Ph.D.

University of Houston - Clear Lake (UHCL) — *Houston, TX*

M.S. - Computer Engineering — *Jan. 2017 - May 2019*

Advisor: Xiaokun Yang, Ph.D.

Dhirubhai Ambani Institute of Information and Communication Technology (DAIICT) — *Gujarat, India*

B.Tech. - Information and Communication Technology — *July 2012 - Dec. 2016*

Advisor: Biswajit Mishra, Ph.D.

Research Experience

Research Assistant — *Raleigh, NC*

NC State University & CAEML — *Aug. 2019 - Present*

- Explore the feasibility of FPGA based accelerator for advanced decision tree based ML algorithms
- Tackle real time high workloads with low latency for a specific problem
- PI: Dr. Paul Franzon, Co-PI: Dr. Aydin Aysu

Teaching Assistant, Teaching Fellow & Research Assistant — *Houston, TX*

UHCL — *May. 2017 - May 2019*

- Instructed a course Lab of Computer Architecture consisting 40 undergraduate students
- Designed labs in Xilinx Vivado Design Suite using VHDL
- Handled Lab for Electronics & Lab for Computer Architecture consisting 50 undergraduate students
- Assisted graduate students in Advanced Digital System Design course utilizing ModelSim, Verilog and Xilinx ISE

Summer Research Intern — *Gujarat, India*

DAIICT — *May 2015 - July 2015*

- Explored optimization techniques for performance, area, and power consumption using Cadence Encounter and tickle files on a couple of micro-controllers' open-source RTL (MSP430 & OR1200)

Industry Experience

Machine Learning Intern — *Raleigh, NC*

Hewlett Packard Enterprise (HPE) — *May 2020 - Aug. 2020*

- Performed Random Forest benchmarking on CPU, GPU, and FPGA

System Developer Intern — *Gujarat, India*

Inweon IT Innovations Pvt. Ltd. — *May 2015 - Oct. 2015*

- Formulated a program to find the length of rice grains from provided image using C++ and OpenCV
- Integrated the same environment on Raspberry pi micro-controller to perform the code remotely

Skills

Programming	Python, Verilog, VHDL, Matlab, LaTeX, Bash Scripting, Tcl Scripting, Make
Tools	Xilinx (Vitis, Vitis HLS, Vivado, ISE), Synopsys (Design Compiler, IC Compiler 2, Custom Compiler), Cadence (Encounter), SciKit Learn, XGBoost, Xelera, LTSpice, OpenCV, Vim, NI Multisim, ModelSim
Hardware	FPGAs (Basys 3, Nexys 4, Xilinx Virtex Ulrascale+ VU9P, Alveo U200), Arduino, Raspberry Pi, Beagle Bone Black
Familiar	C, C++, HTML, SystemVerilog, Assembly, WaveForms, SystemC

Publications

- **A. Gajjar**, S. Dave, X. Yang, et al.,"An IoT-Edge-Server System with BLE Mesh Network, LBPH, and Deep Metric Learning," The 22nd International Conference on Artificial Intelligence **(ICAI2020)**, Accepted, March 2020
- H. Koc, **A. Gajjar**, S. Graham, "Static Charging Scheduling of Electric Vehicles at Private Station," 10th IEEE Annual Information Technology, Electronics and Mobile Communication Conference **(IEMCON)**, pp. 0237-0240, Vancouver, BC, Canada, 2019
- K. Vaca, **A. Gajjar**, X. Yang, "Real-Time Automatic Music Transcription (AMT) with Zync FPGA," IEEE Computer Society Annual Symposium on VLSI **(ISVLSI)**, Student Forum, pp. 378-384, Miami, FL, USA, 2019 (Acceptance Rate: 17%)
- **A. Gajjar**, X. Yang, H. Koc, et al., "Mesh-IoT Based System For Large-Scale Environment," 5th Annual Conf. on Computational Science & Computational Intelligence **(CSCI2018)**, pp. 1019-1023, Las Vegas, NV, USA, 2018 (Acceptance Rate: 23%)
- X. Yang, L. Wu, **A. Gajjar**, et al., "A Vision of Fog Systems with Integrating FPGAs and BLE Mesh Network," Journal of Communications **(JCM)**, (ISSN: 1796-2021), Vol. 14, No. 3, pp. 210-215, 2019
- **A. Gajjar**, X. Yang, et al., "An FPGA Synthesis of Face Detection Algorithm using HAAR Classifiers," Intl. Conference on Algorithms, Computing, and Systems **(ICACS2018)**, PP.133-137, Beijing, China, 2018
- Y. Zhang, X. Yang, **A. Gajjar**, et al., "Exploring Slice-Energy Saving on An Video Processing FPGA Platform with Approximate Computing," Intl. Conference on Algorithms, Computing, and Systems **(ICACS2018)**, PP.138-143, Beijing, China, 2018
- Y. Zhang, X. Yang, **A. Gajjar**, et al., "Hierarchical Synthesis of Approximate Multiplier Design for Field-Programmable Gate Arrays (FPGA)-CSRmesh System," Intl. Journal of Compt. Applications **(IJCA)**, Vol. 180, No. 17 PP. 1-7, Feb. 2018
- **A. Gajjar**, Y. Zhang, X. Yang, "Demo Abstract: A Smart Building System Integrated with An Edge Computing Algorithm and IoT Mesh Networks," The Second ACM/IEEE Symposium on Edge Computing **(SEC2017)**, Article No. 35, Oct. 2017

Presentation

- **A. Gajjar**, "IoT-Edge-Server Based Embedded System For Wide-Range Habitats," Student's Day, IEEE Student Branch, UHCL, April 2019
- **A. Gajjar**, X. Yang, et al., "Mesh-IoT Based Smart and Secure Monitoring System for Wide-Range Territory," IEEE Innovation and Automation Conference, Gilruth Center, NASA, Houston, November 2018
- X. Yang, **A. Gajjar**, Y. Zhang, et al., "Learning-on-Chip: Facial Detection with Approximations of FPGA Computing," Houston Robotics and AI Day, UHCL, August 2018
- **A. Gajjar**, X. Yang, "Poster presentation – A Wide Area IoT Mesh Network With Edge Computing," IEEE Innovation and Automation Conference, Gilruth Center, NASA, Houston, October 2018
- **A. Gajjar**, X. Yang, "Poster presentation – A Smart Home/Building System Integrated with An Edge Computing Algorithm and CSRmesh Networks," Houston Robotics and AI Day, UHCL, July 2017

Reviewer

Conference

- Journal of Real-Time Image Processing (JRTIP)
- 22nd International Conference on Artificial Intelligence (ICAI 2020)
- Proceedings of the 3rd International Conference on Computer Science and Application Engineering (CSAE 2019)
- 7th International Conference on Computer and Communications Management (ICCCM 2019)
- 9th International Workshop on Computer Science and Engineering (WCSE 2019)

Service To Profession

- Secretary, Executive Officer, IEEE SB UHCL, 2018-2019
- Orientation Leader, International Student Orientation, UHCL, 2017-2018
- Mentor, I'Fest, IEEE SB DAIICT, 2015-2016
- Volunteer, TENSYMP'15, Region 10 IEEE International Conference, India, 2015
- Event Coordinator, I'Fest, IEEE SB DAIICT, 2015
- Leader, Special Interest Group on Microcontrollers, IEEE SB DA-IICT, 2014

- Teaching Assistant, Workshop on Embedded System and Arduino, PDPU, India, 2013

Academic Projects

8T Based 16-bit (4x4) 2-Port SRAM

NCSU

Course Project | VLSI Design Systems

Mar. 2021 - Apr. 2021

- Designed architecture for a 16-bit (4x4) SRAM employing 15nm FinFet technology at NCSU with Synopsys Custom Compiler
- Created transistor level schematics and layouts for the SRAM and its peripherals such as Flip-Flops, Row decoders, and Bit-line conditioning
- Created transistor level schematics for the SRAM and its peripherals like TSPC, Row and Column decoders, Multiplexer, Precharge and inverter
- Verified functionality using DRC and LVS and optimized the design for the given objective: $Energy \times Delay \times Area$

Physical Design Optimization

NCSU

Course Project | Electronic System Level & Physical Design

Sep. 2020 - Oct. 2020

- Performed the complete Physical design flow (RTL Synthesis, Placement, CTS, Routing, STA) for s38584-ISCAS89 sequential benchmark circuits employing Synopsys DC and ICC2 with FreePDK15: 15nm FinFet technology at NCSU
- Optimized the design for the given objective: $Area \times Delay^2$
- Met the setup and hold timing constraints with low critical path delay and core area of the design

Input Gate g(t) of LSTM

NCSU

Course Project | ASIC & FPGA Design With Verilog

Aug. 2019 - Dec. 2019

- Designed and synthesized hardware for input gate g(t) of LSTM employing Verilog HDL
- Simulated the design using ModelSim as well as verification for the design's functionality
- Improved the design by exploiting a parallelized pipelining architecture in order to minimize timing and area
- Optimized design with Synopsys' Design Compiler

RGB to Gray Scale Converter

UHCL

Course Project | Advanced Digital System Design

Aug. 2017 - Dec. 2017

- Designed 8-bit (each) RBG to gray scale converter finite state machine design (FSMD)
- Transferred FSMD into RTL utilizing Verilog and ModelSim, and analyzed accuracy and power on Xilinx ISE
- Researched approximate design trade-off techniques on the design

Low Cost Security System using Off the Shelf Components

DAIICT

Final Year Project | DAIICT

Jan. 2016 - Apr. 2016

- Devised a security system capturing motion sensor-triggered image of an intruder and informing to the designated person using SMTP protocol on a Beagle Bone Black
- Engineered product was almost 50% cost-effective compared to indistinguishable products in the commercial market

Surveillance Bot

DAIICT

Course Project | Embedded Hardware Design

Jan. 2015 - Apr. 2015

- Developed a manually controlled surveillance robot on Beagle Bone Black transmitting a live video stream

Honors & Awards

- Outstanding Computer Engineering Graduate Student Award, UHCL, 2019
- Research Scholarship Award ($1300), Dr. Ted Leibfried Legacy, UHCL, July 2018 **(2/100 Students)**
- Graduate Student Ambassador, College of Science & Engineering, UHCL, 2018 **(2 Students out of CENG Program)**
- Member, Phi Kappa Phi Honor Society, UHCL, April 2018 (Invited)
- Research/Teaching Assistant Scholarship, UHCL, 2017-2018
- Student Travel Grant Aware ($800), National Science Foundation, SEC2017, October 2017
- Leadership Honor, Omicron Delta Kappa (ODK), Hilary Jo Karp Circle Honor Society, November 2017