Overview of Computers

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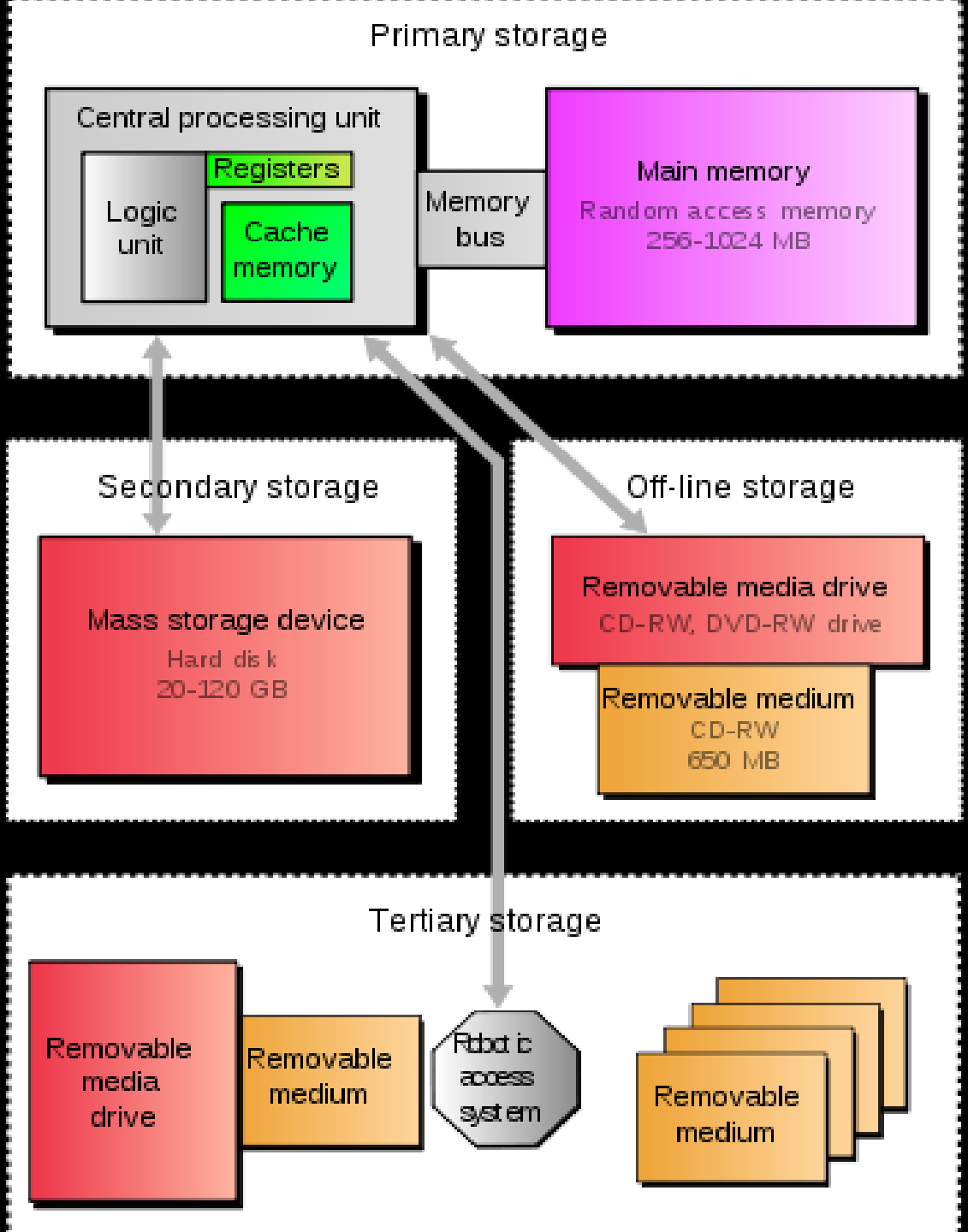
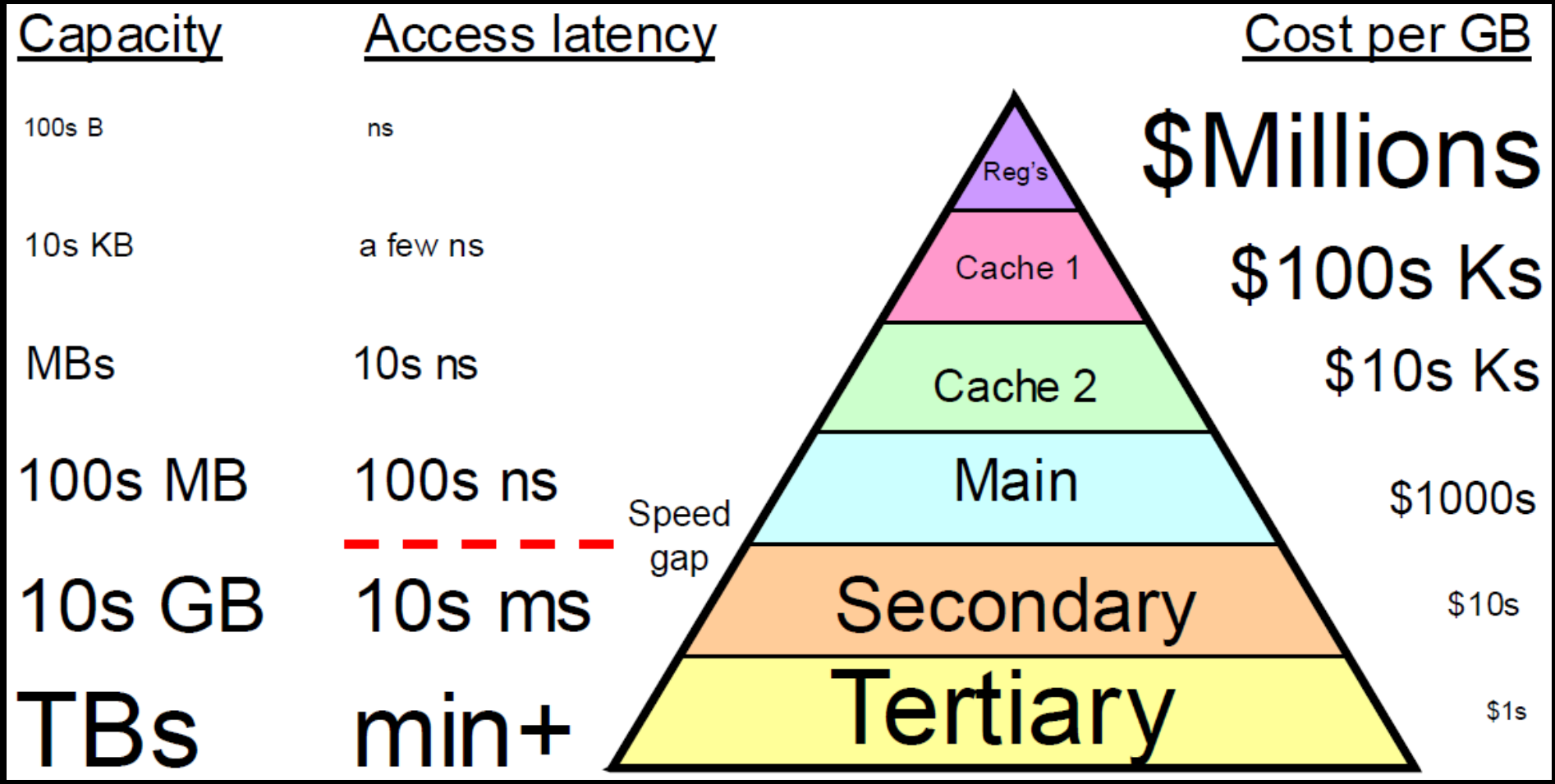
Memory

Storage/Memory

- What ?
- Why ?


Primary storage
Central processing unit
Logic unit
Registers
Cache memory
Memory bus
Main memory
Random access memory
256-1024 MB
Secondary storage
Mass storage device
Hard disk
20-120 GB
Off-line storage
Removable media drive
CD-RW, DVD-RW drive
Removable medium
CD-RW
650 MB
Tertiary storage
Removable media drive
Removable medium
Robotic access system
Removable medium

Typical Levels in a Hierarchical Memory



RAM (Random Access Memory)

- DRAM – Dynamic RAM
- SRAM – Static RAM

DRAM

DRAM

- Main Memory (generally called as RAM)

DRAM / Main Memory

- Type of random access semiconductor memory
- Stores each bit of data in a separate tiny capacitor within an integrated circuit
- The capacitor can
  - either be charged (representing 1)
  - or discharged (representing 0)

DRAM / Main Memory

- The electric charge on the capacitors slowly leaks off
- DRAM requires an external memory refresh circuit (i.e., dynamic)
- DRAM consumes relatively more power

DRAM / Main Memory

- A DRAM cell consists of one capacitor and one transistor
- The transistor is used to access the capacitance
- DRAM is volatile memory

SRAM

SRAM

- Cache Memory (inside CPU)

SRAM / Cache Memory

- Type of random access semiconductor memory
- Uses bistable latching circuitry (flip-flop) to store each bit
- Requires 4-6 transistors in each SRAM cell
- No need of periodically refresh like DRAM

SRAM / Cache Memory

- SRAM is faster and more expensive than DRAM
- Volatile memory
- Low power consumption
- Less storage

L1 Cache Memory

- The L1 cache is built using larger transistors and wider metal tracks.
- Thus, trading off space and power for speed.
- The higher level caches (L2 and L3) are more tightly packed and use smaller transistors.

L1, L2 and L3 Cache Memory

- Speed L1>L2>L3
- Transistor size L1>L2>L3
- Metal area L1>L2>L3
- Cost per bit L1>L2>L3
- Memory size L1<L2<L3

Why Random Access?

Why Random Access?

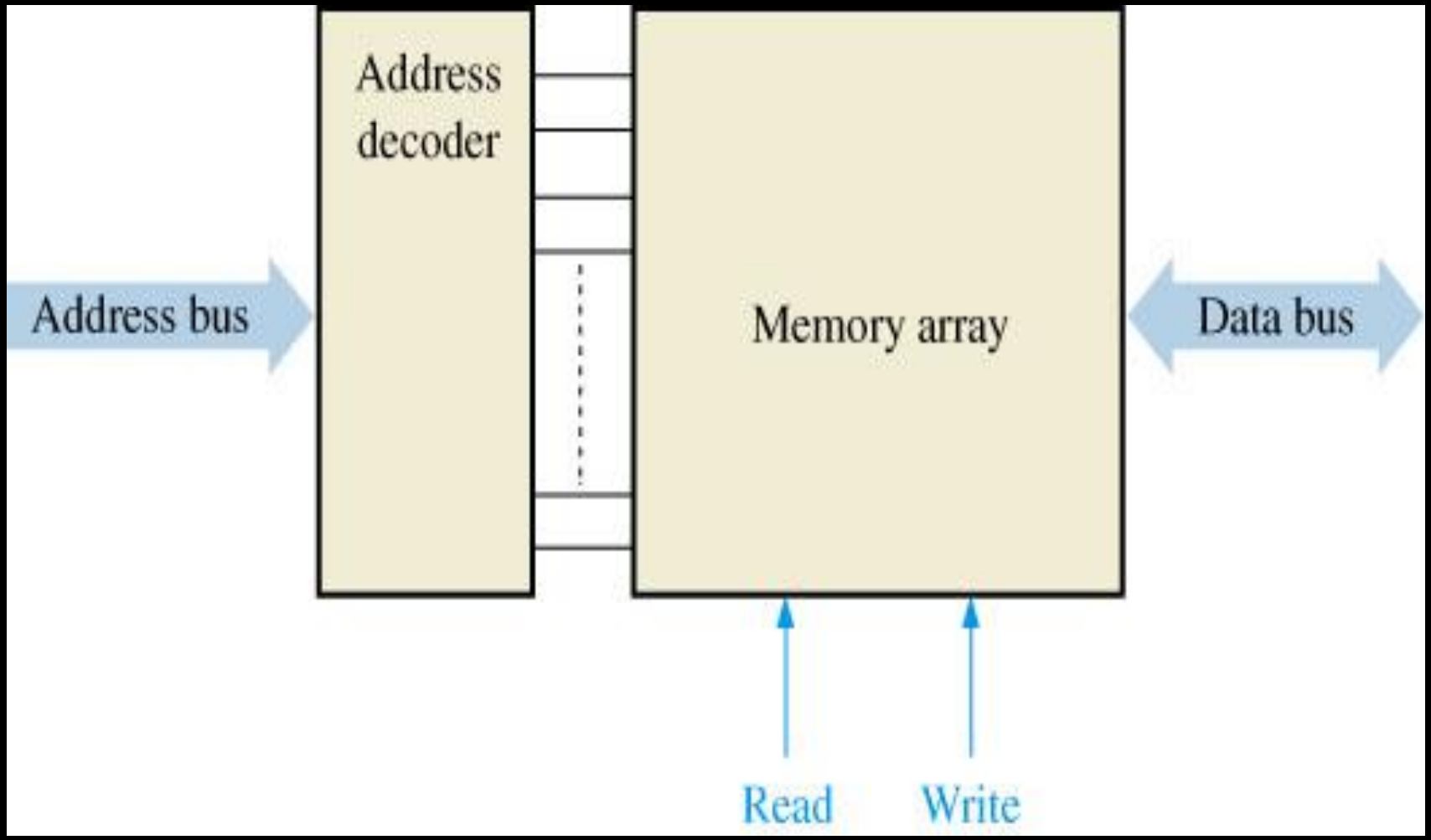
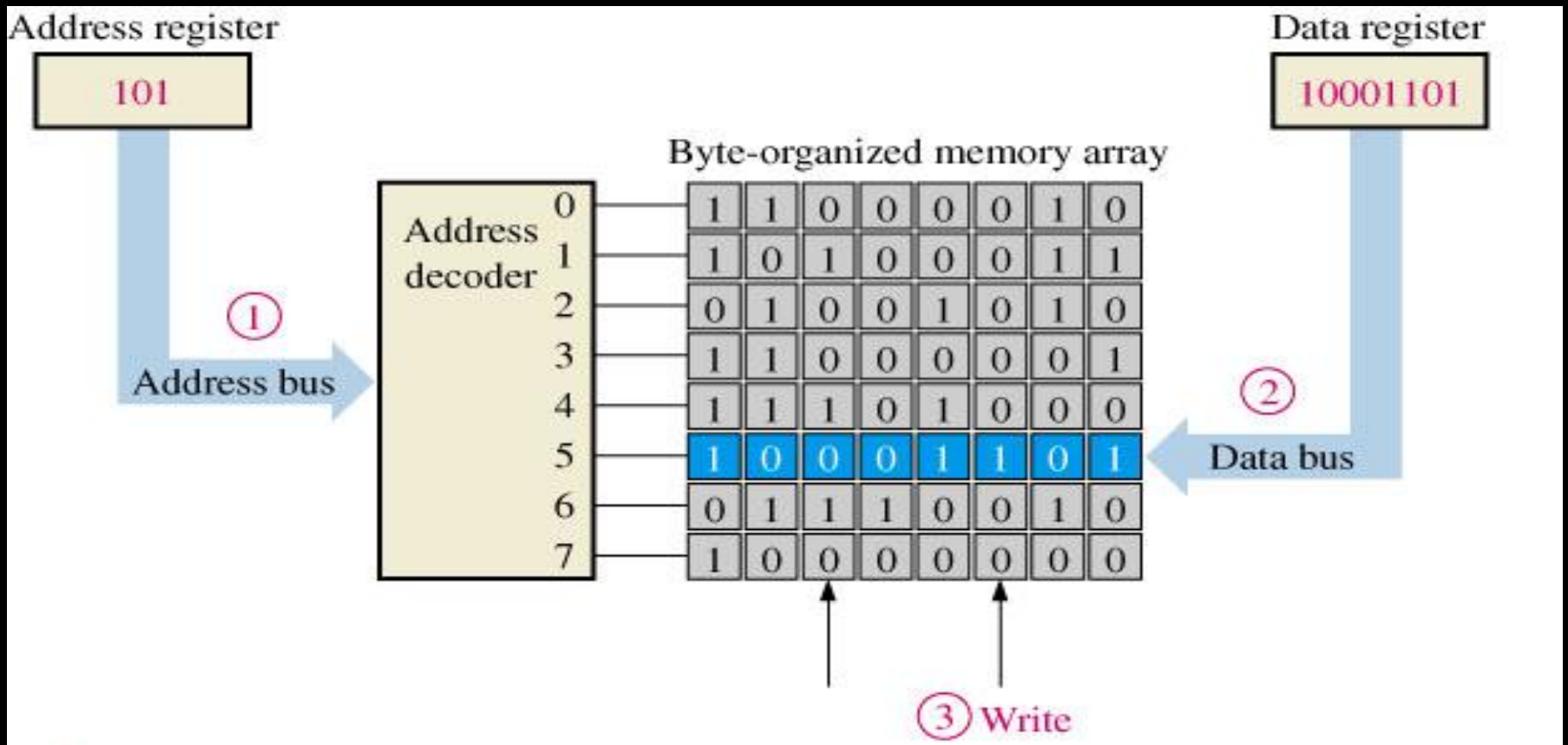
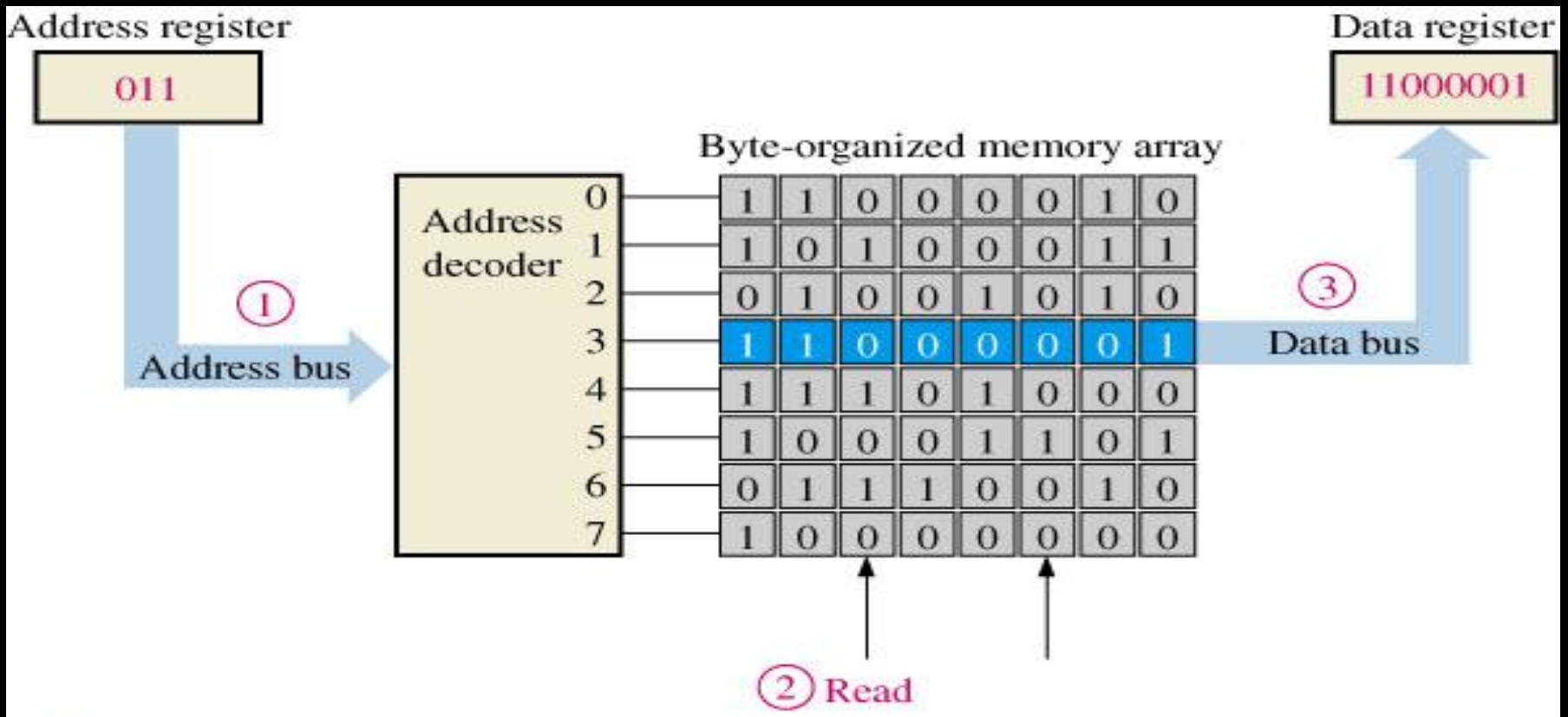


Illustration of the write operation



1. Address code 101 is placed on the address bus and address 5 is selected.
2. Data byte is placed on the data bus.
3. Write command causes the data byte to be stored in address 5, replacing previous data.

Illustration of the read operation



1. Address code 011 is placed on the address bus and address 3 is selected.
2. Read command is applied.
3. The contents of address 3 is placed on the data bus and shifted into data register. The contents of address 3 is not destroyed by the read operation.

ROM (Read Only Memory)

ROM (Read Only Memory)

- A type of memory where data can be stored permanently or semi permanently.
- Data can be read form a ROM, but there is no write operation as in RAM.
- The ROM is also a random access memory.
- Used for hardcoding the program such as BIOS, etc.

CPU Registers

CPU Registers

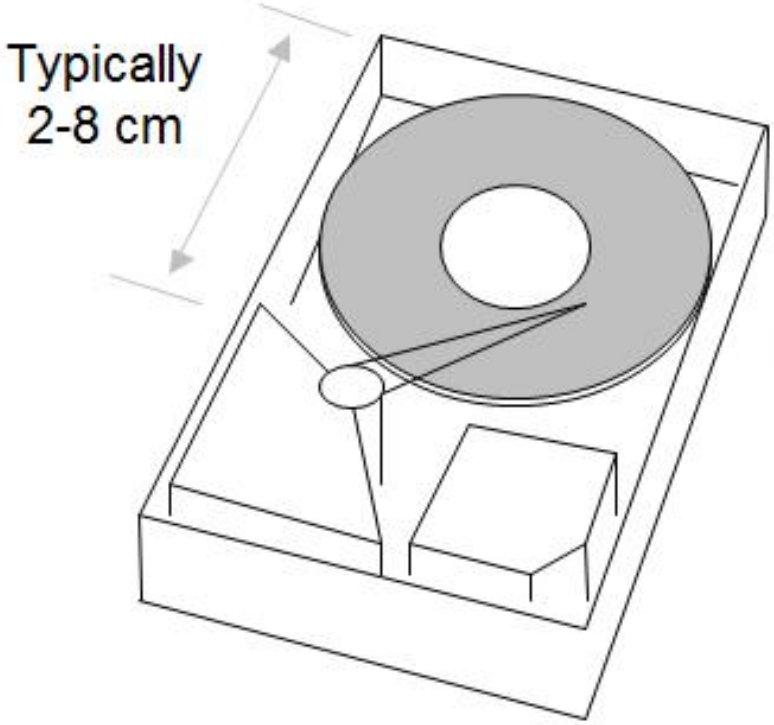
- Usually implemented as flip-flops
- Very fast and versatile
- Much larger and more expensive per bit than main memory
- Usually, the register cell is a 4-transistor SRAM cell

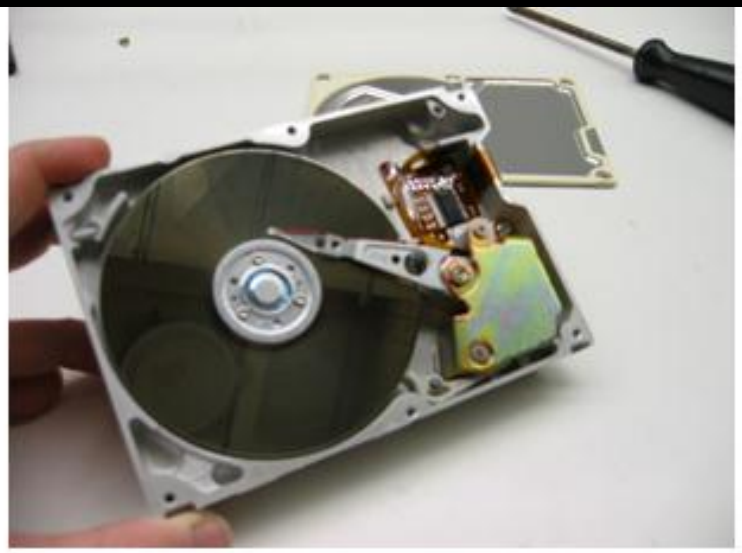
Hard Drives


IBM WARRANTY VOID IF AUTHENTICITY LABEL REMOVED OR DAMAGED.
DO NOT COVER THIS HOLE
Product of China

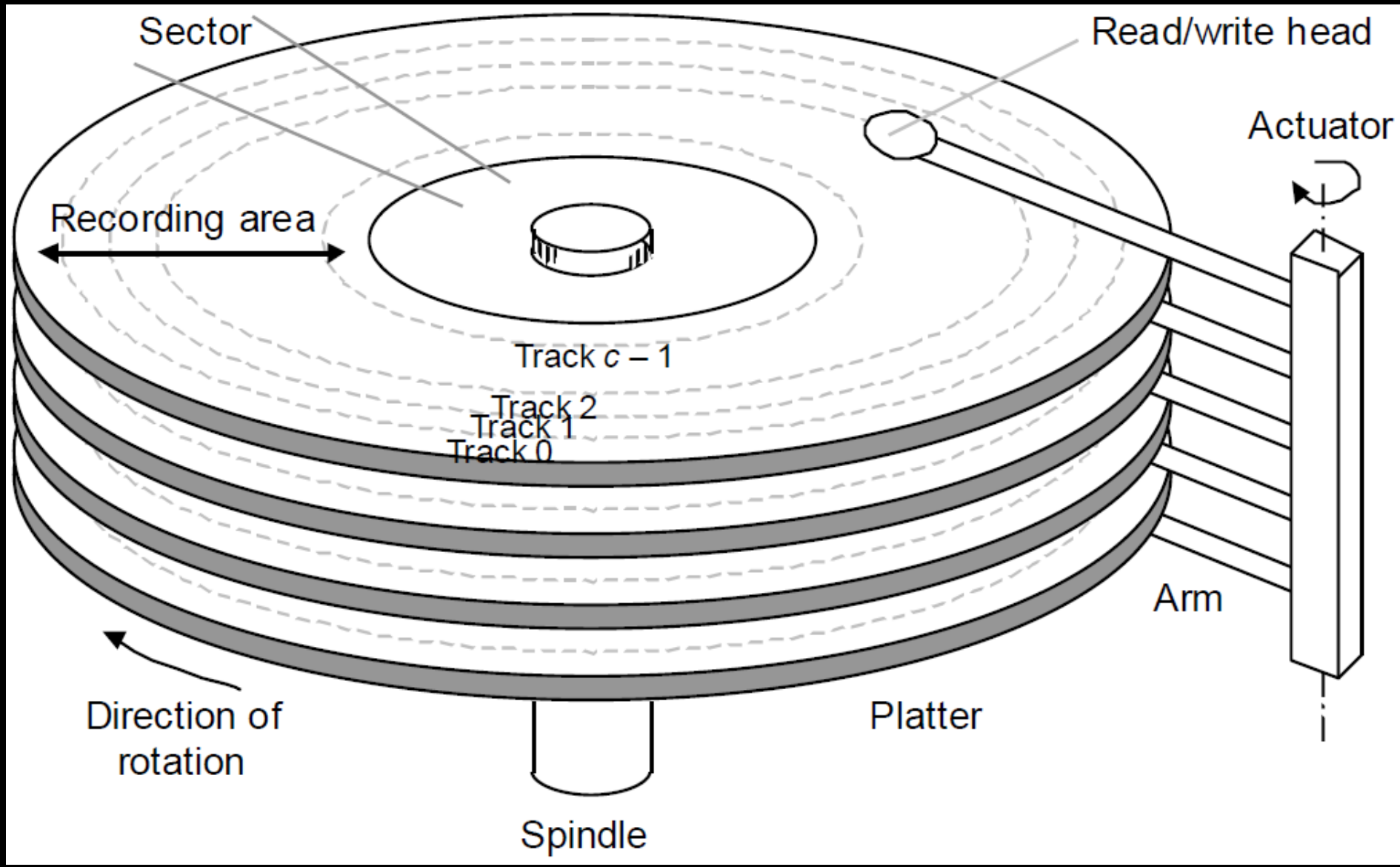
Hard Drives

Hard Drives





Hard Drives


Sector
Read/write head
Actuator
Recording area
Track c – 1
Track 2
Track 1
Track 0
Arm
Direction of rotation
Platter
Spindle

Hard Drives

- Consists of circular "plate" of magnetic material called a platter

- The platters are
  - disks made from a hard material such as glass, ceramic, or aluminum
  - coated with a thin layer of metal that can be magnetized or demagnetized

Hard Drives

- The platter is divided into billions of tiny areas

- Each one of those areas can be independently
  - magnetized (to store a 1) or
  - demagnetized (to store a 0).

Access Time for a Disk