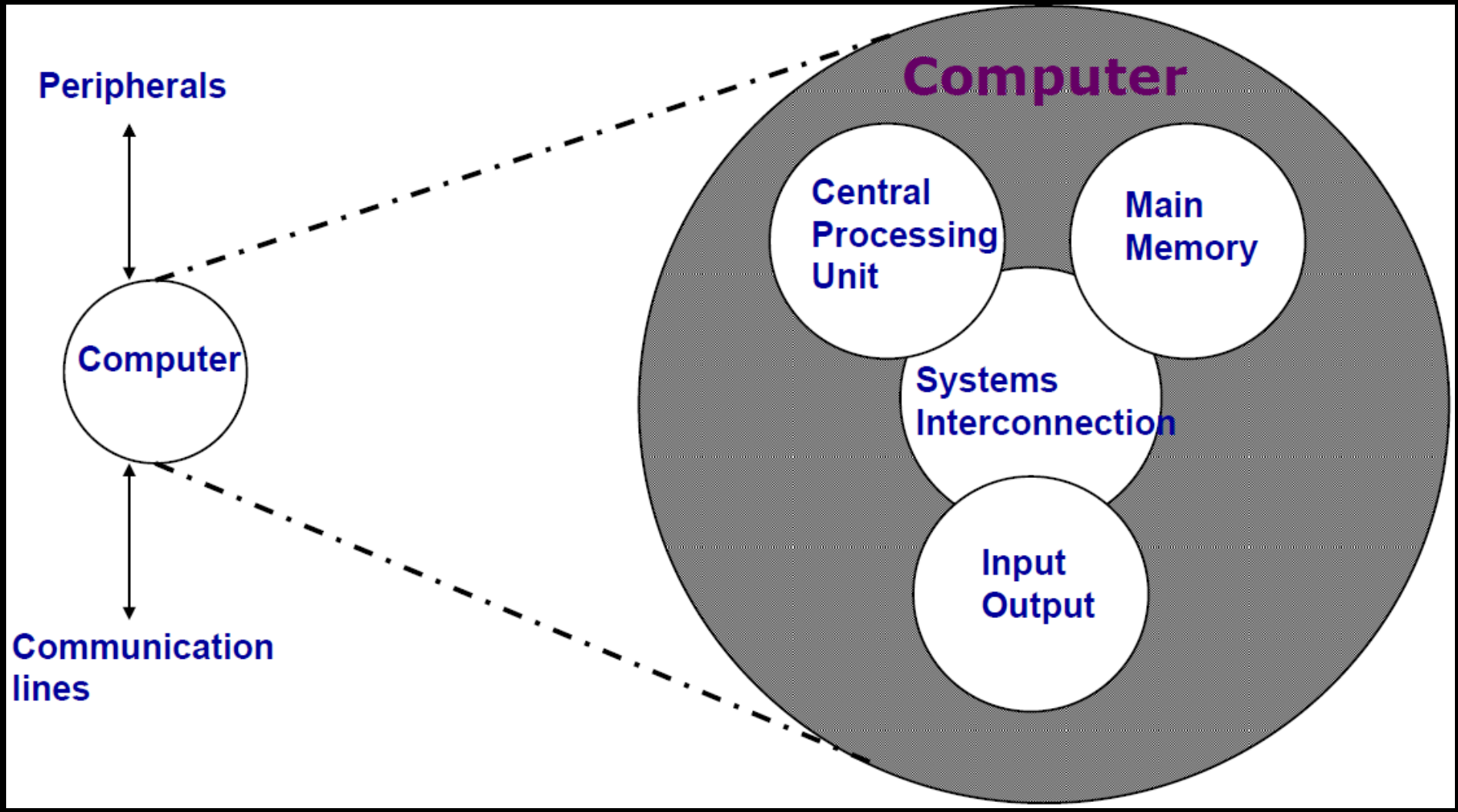
Overview of Computers

Instructor – Dr. Shiv Ram Dubey

Central Processing Unit

Structure – Top Level



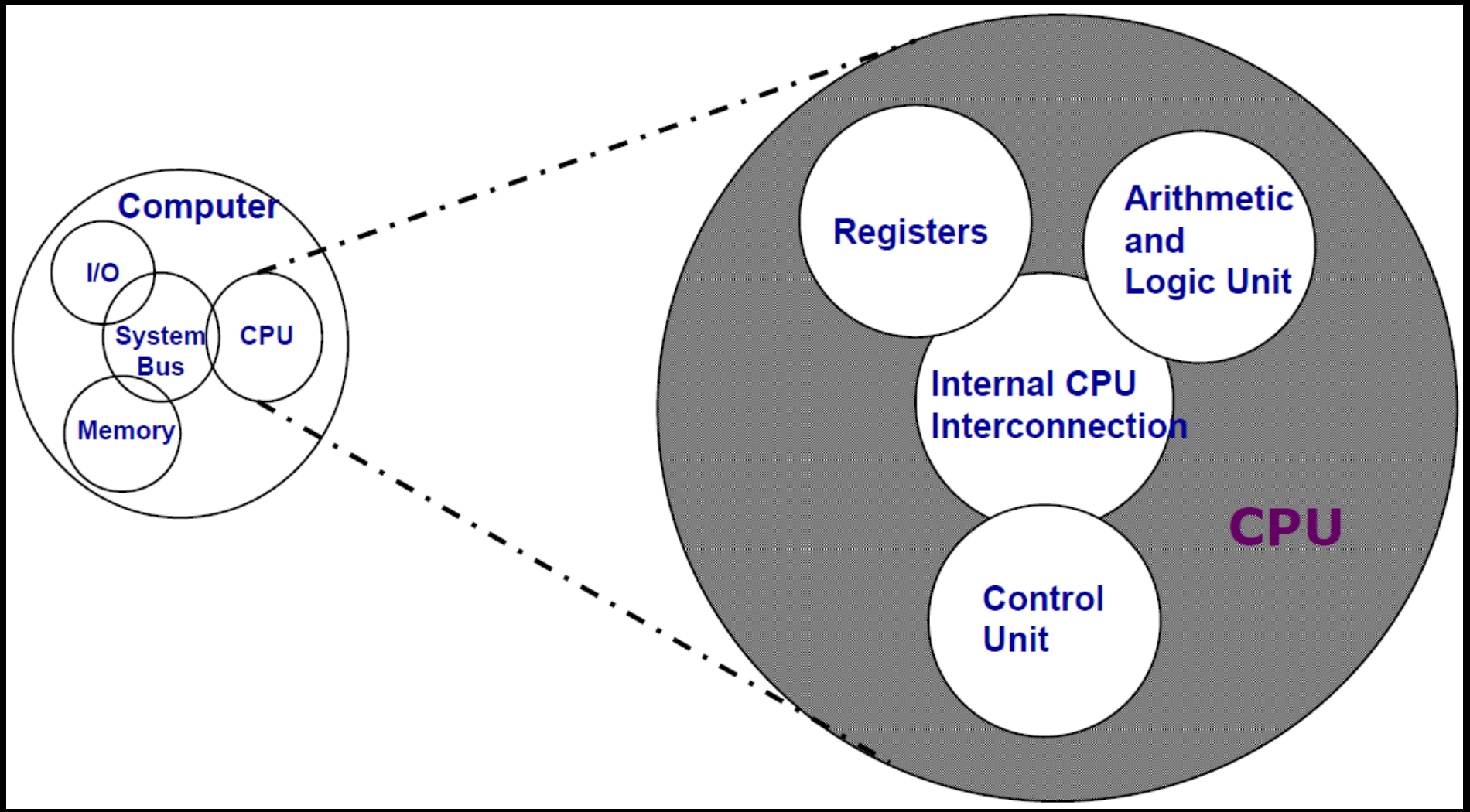
Central Processing Unit (CPU)


intel
Xeon®
processor

CPU

- The **CPU** (***C****entral* ***P****rocessing* ***U****nit)* is the ‘brains’ of the computer.
- The **purpose** of the CPU is to carry out program instructions *(each CPU type is designed to understand a specific group of instructions, the* ***instruction set****).*
- On personal computers and small workstations, the CPU is housed in a single chip called a *microprocessor*.

Structure – The CPU



Major Components of Processor

Storage Components:

- Flip-flops
- Registers
- Cache memory

Execution (Processing) Components:

- Arithmetic Logic Unit (ALU):
  - Arithmetic calculations, Logical computations, Shifts/Rotates

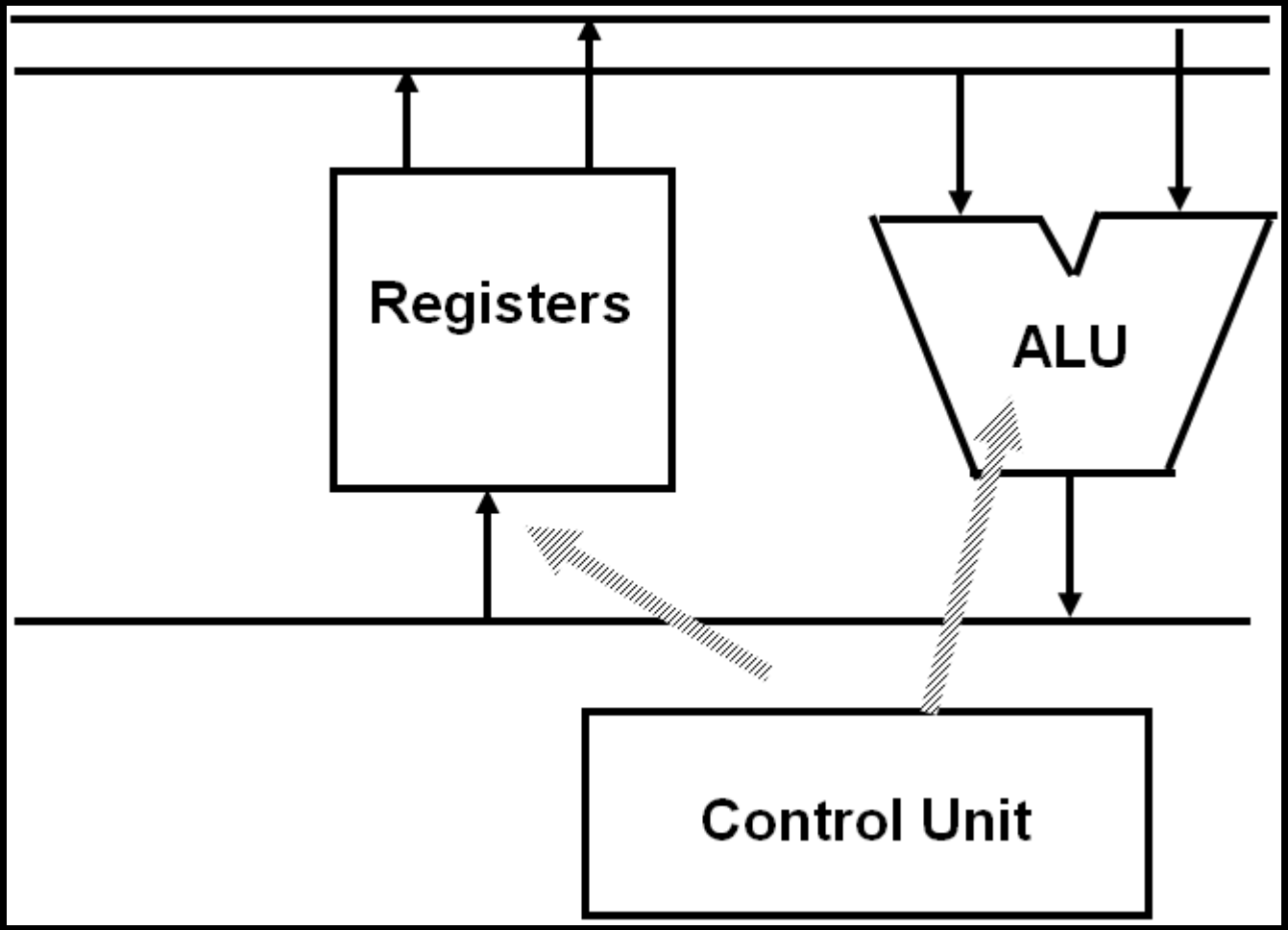
Transfer Components:

- Bus

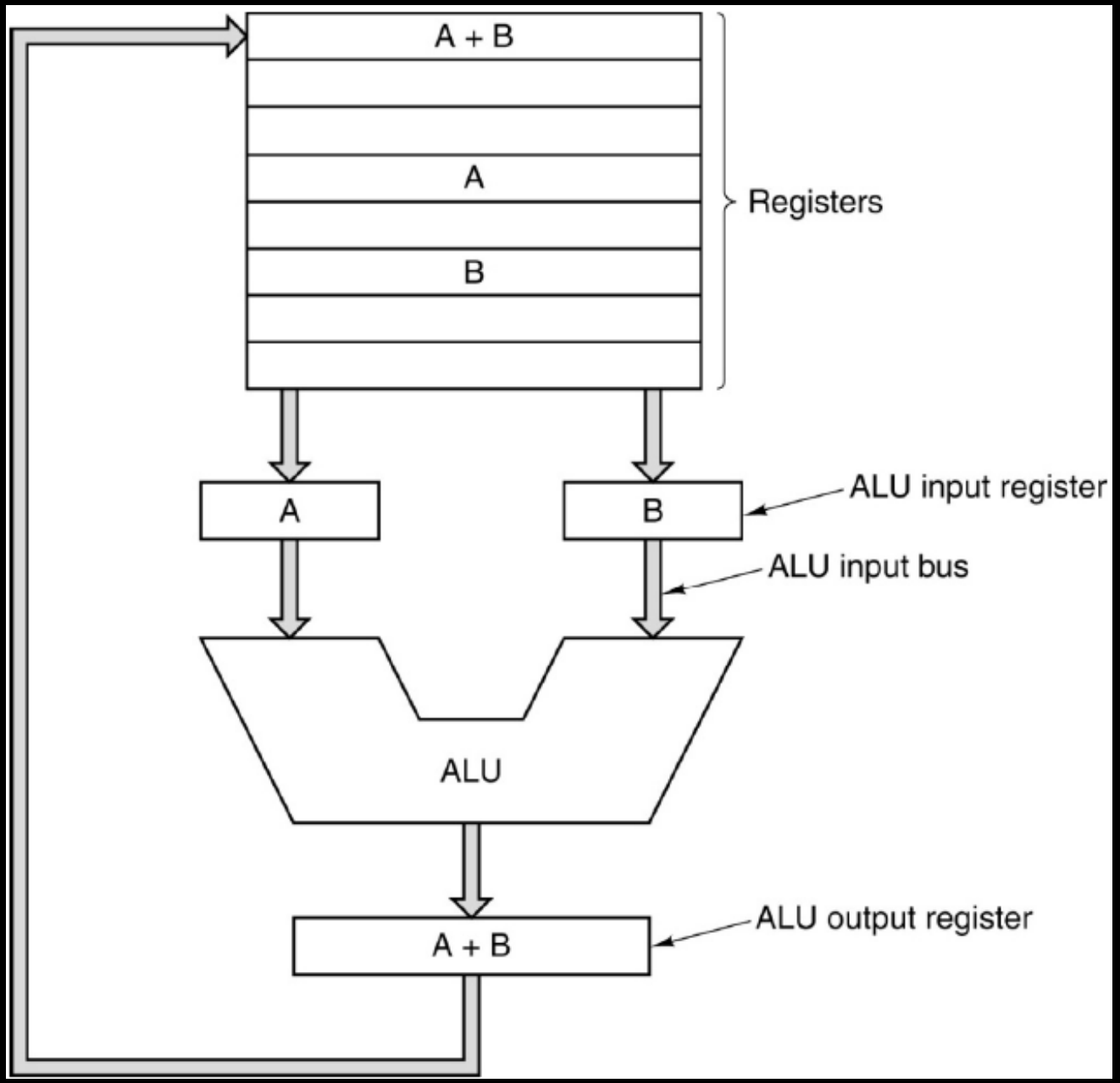
Control Components:

- Control Unit

Processor Organization



Processor Organization

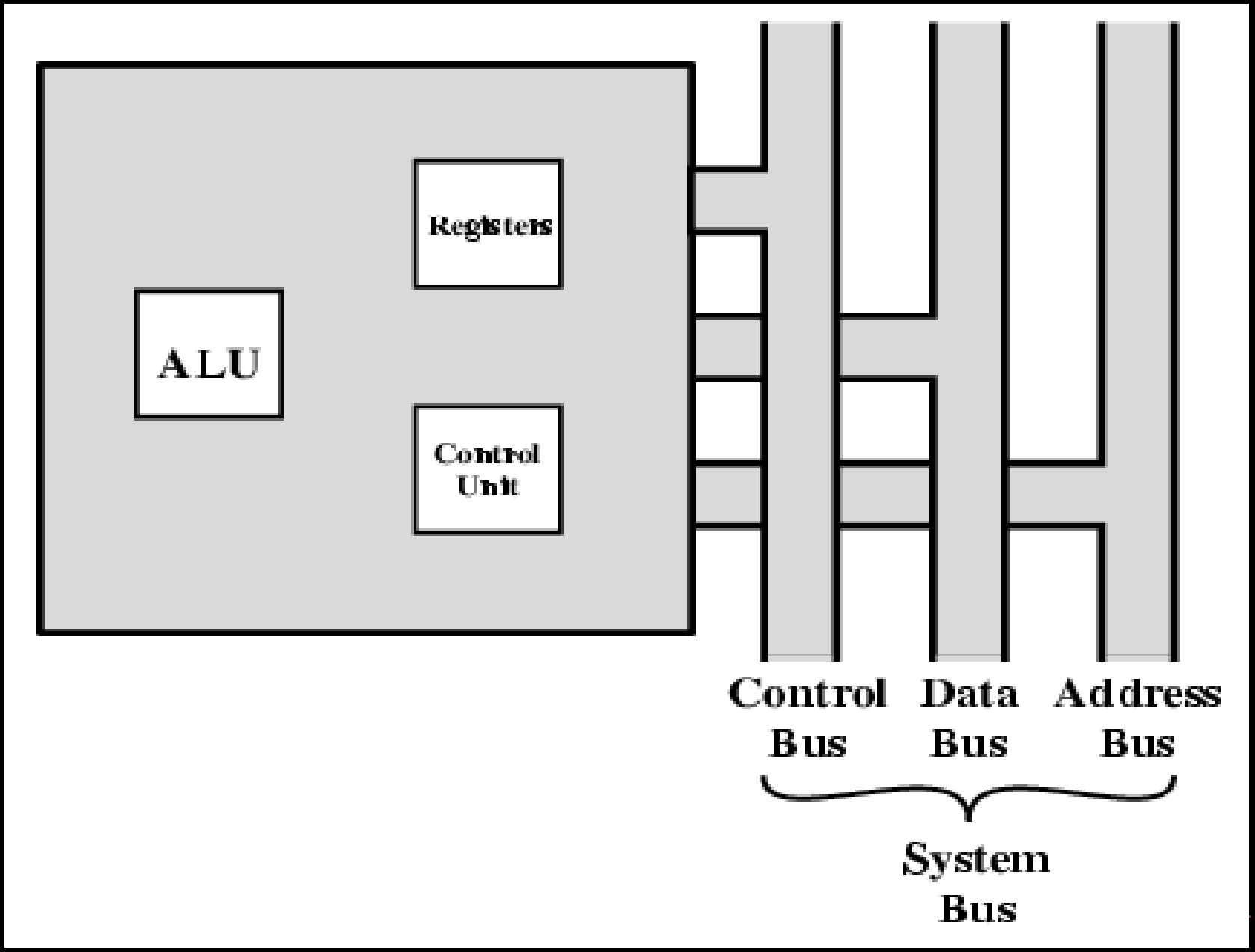


CPU Function

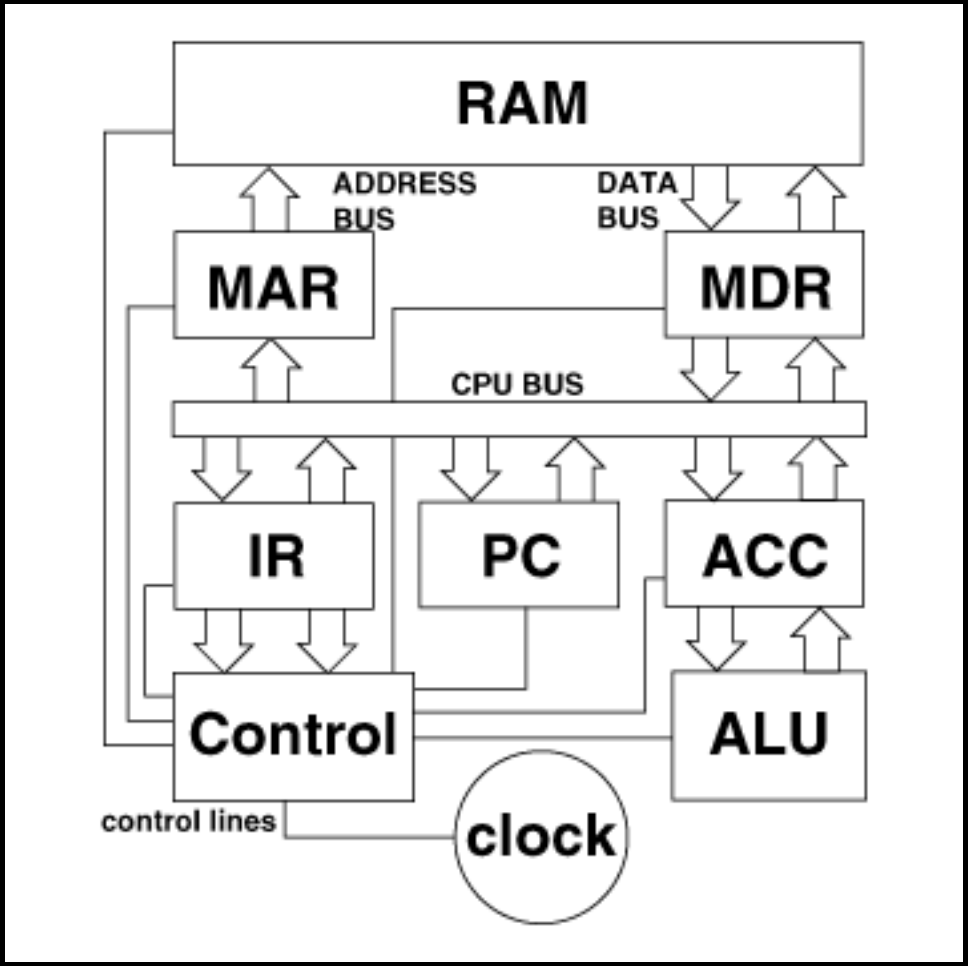
CPU must:

- —Fetch instructions
- —Interpret/Decode instructions
- —Fetch data
- —Process data
- —Write data

CPU With Systems Bus

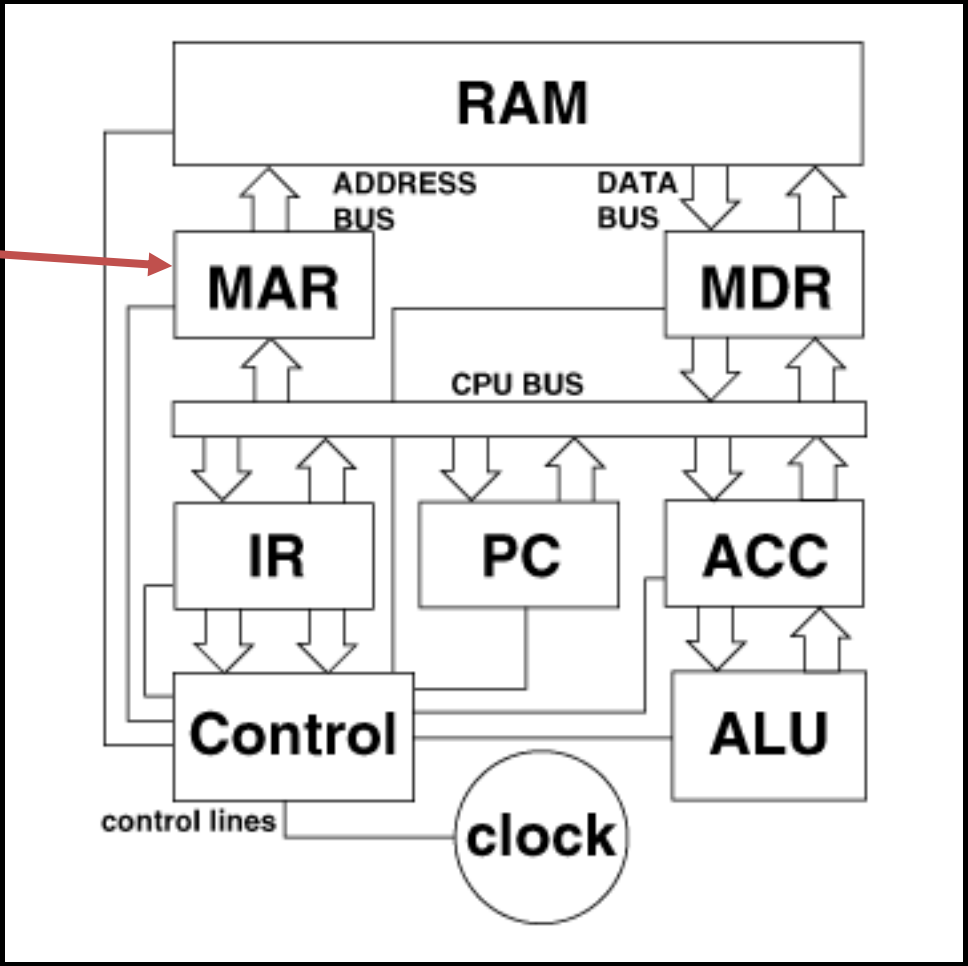


CPU Function



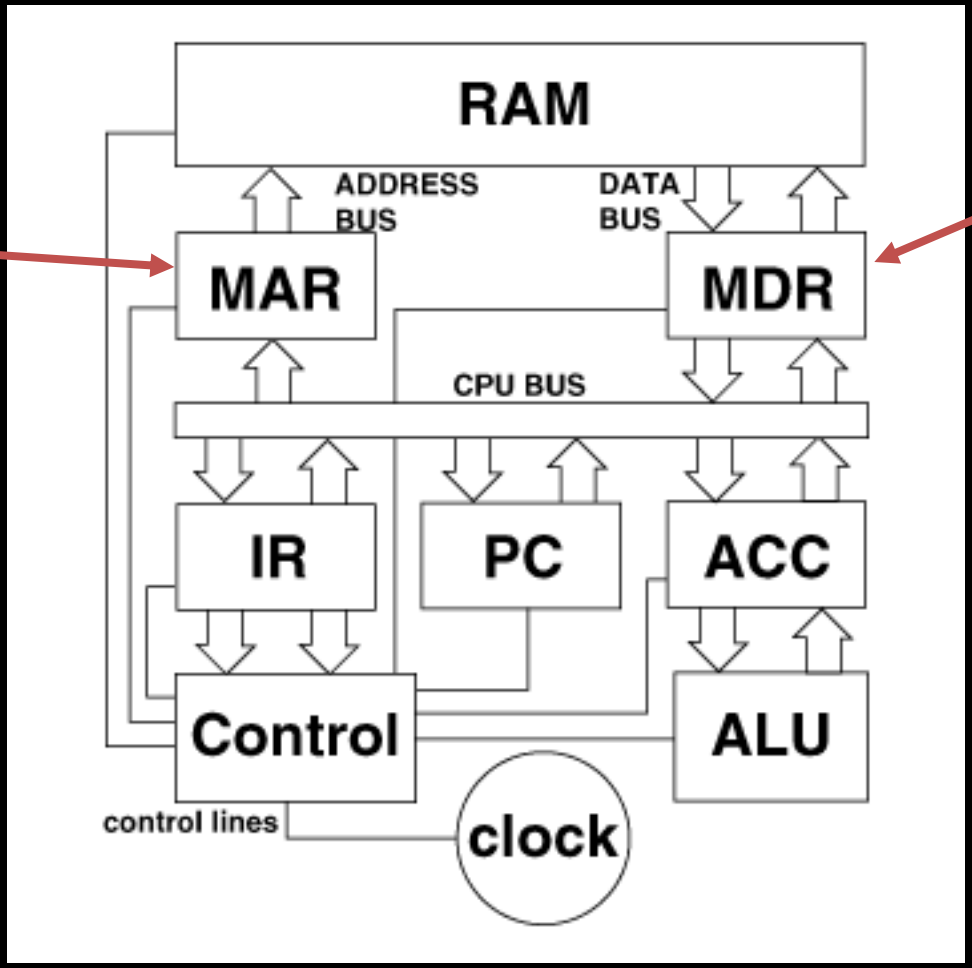
CPU Function

memory address register



CPU Function

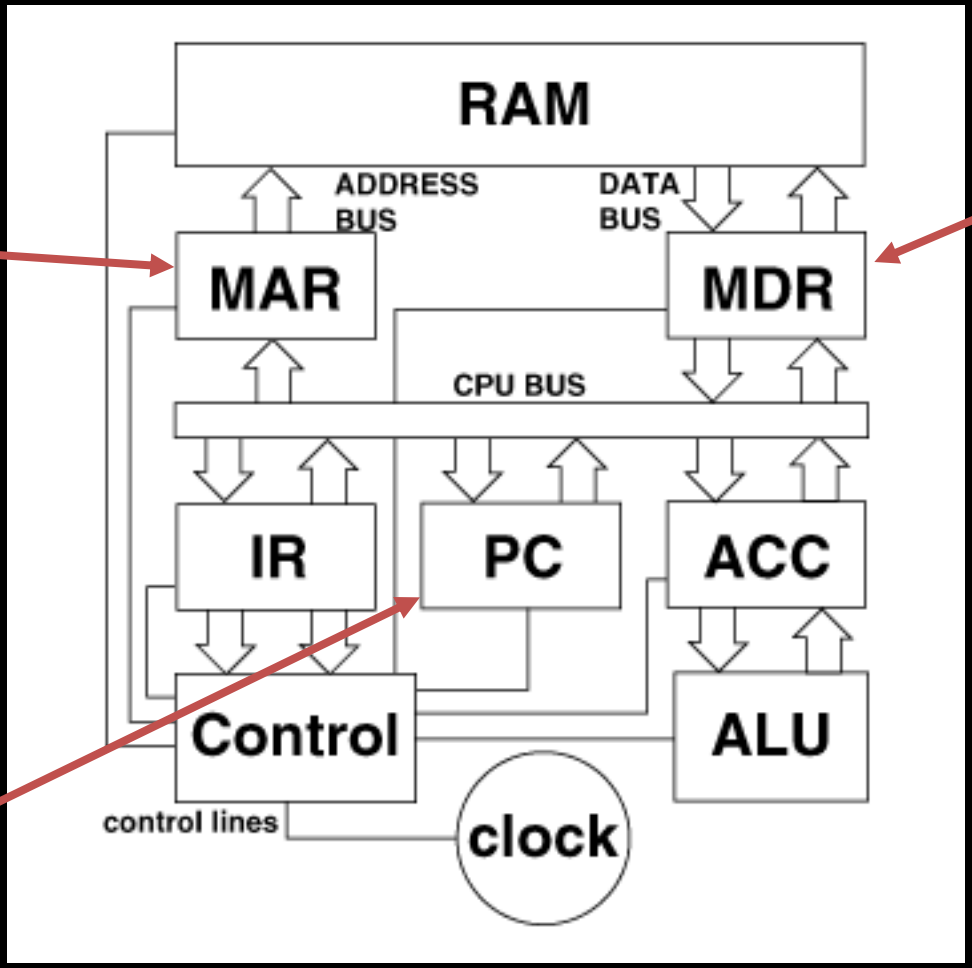
memory address register



memory data register

CPU Function

memory address register



memory data register

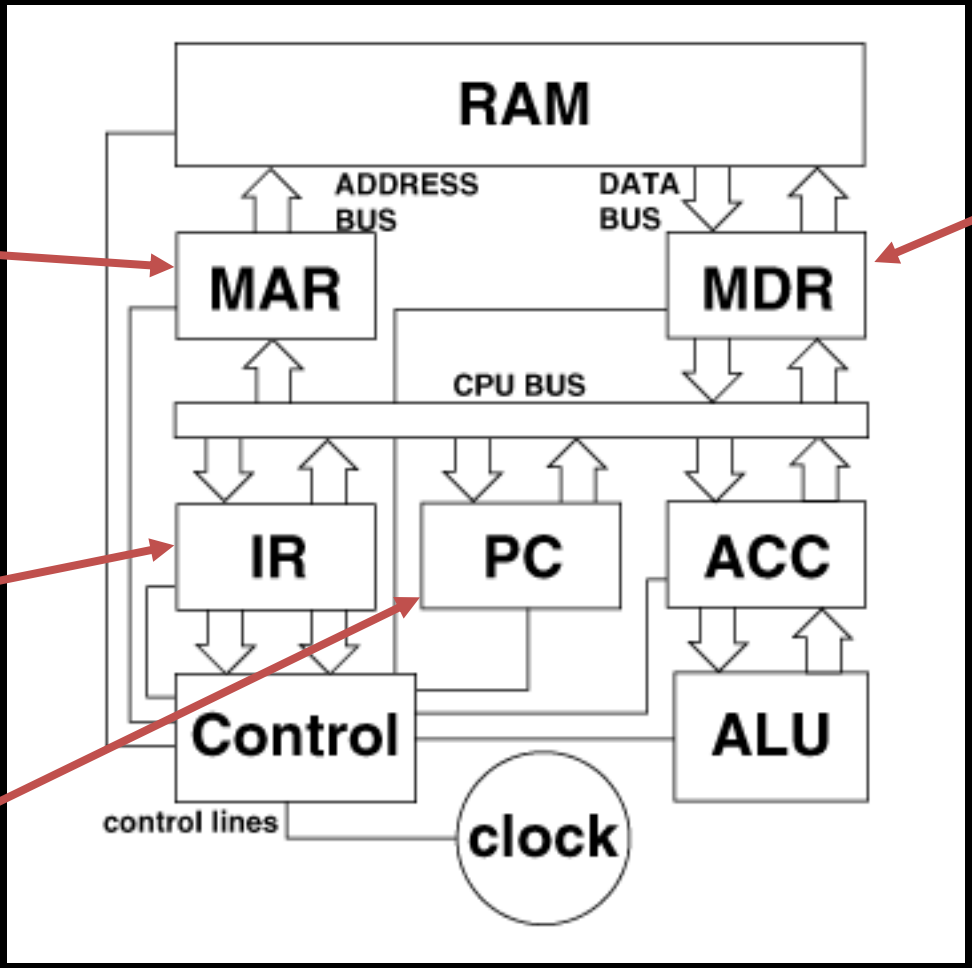
program counter

CPU Function

memory address register

instruction register

program counter



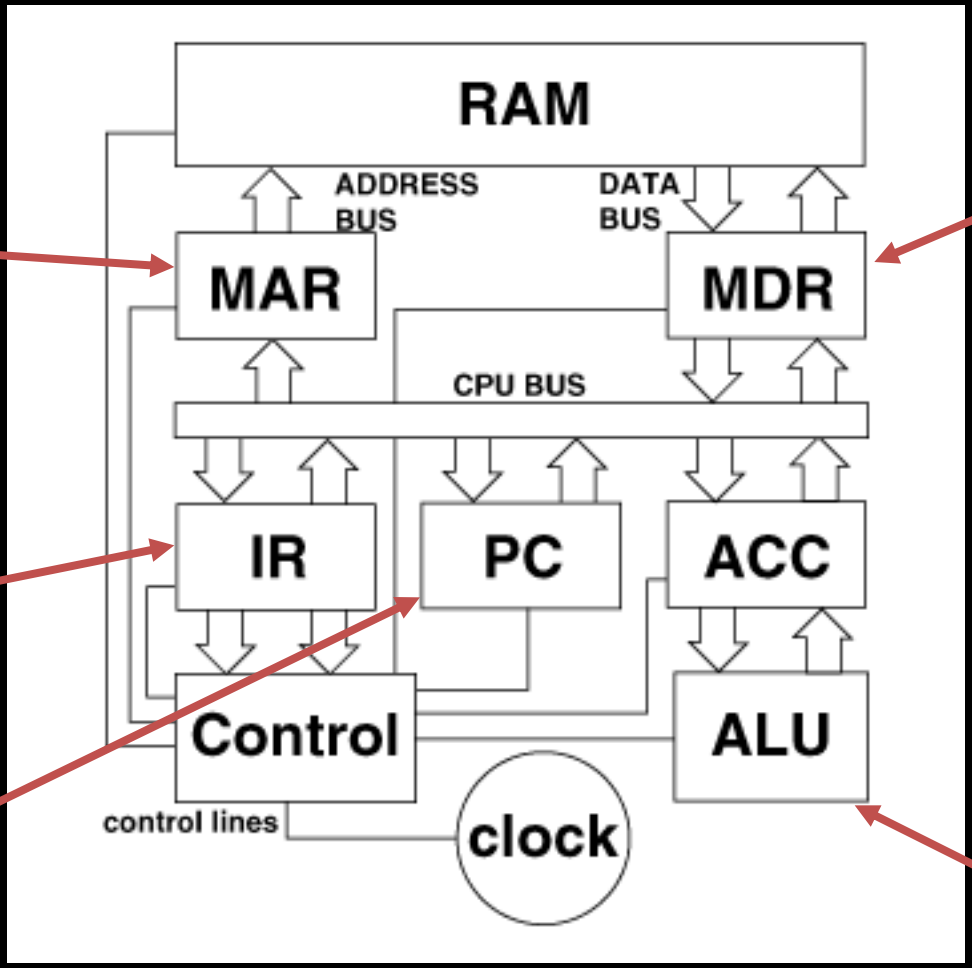
memory data register

CPU Function

memory address register

instruction register

program counter



memory data register

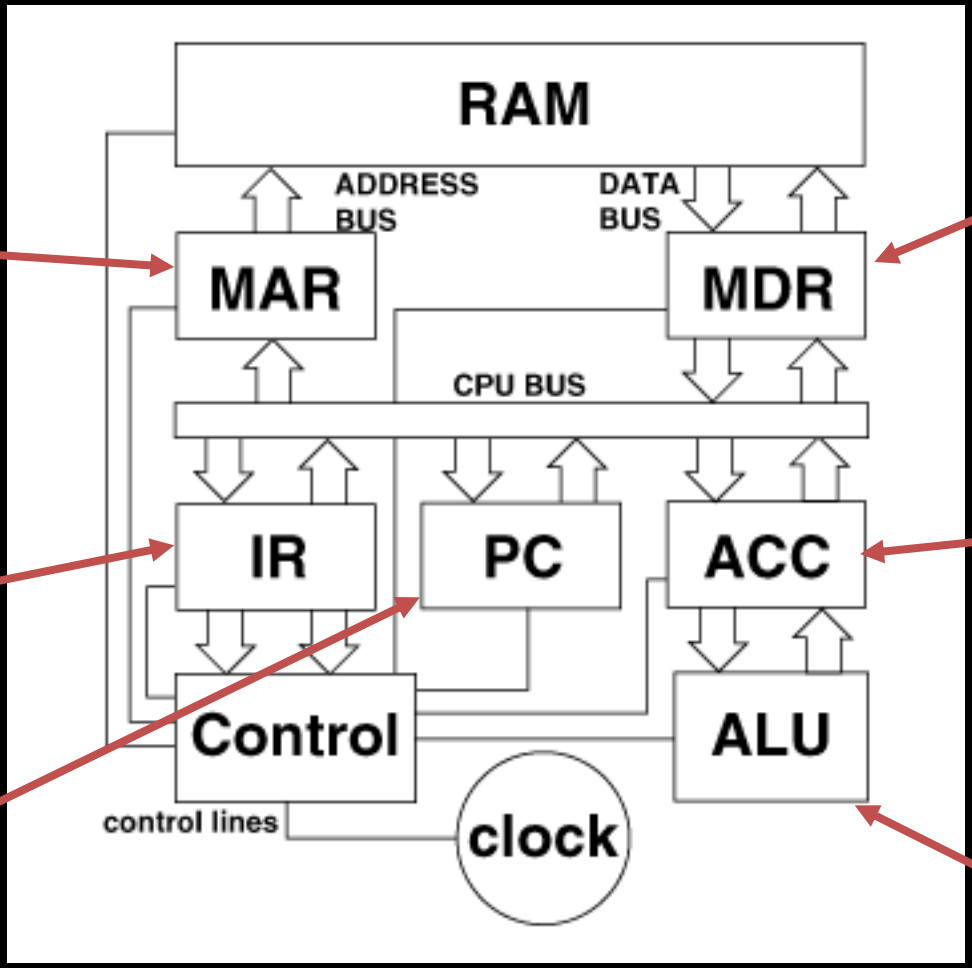
arithmetic logic unit

CPU Function

memory address register

instruction register

program counter

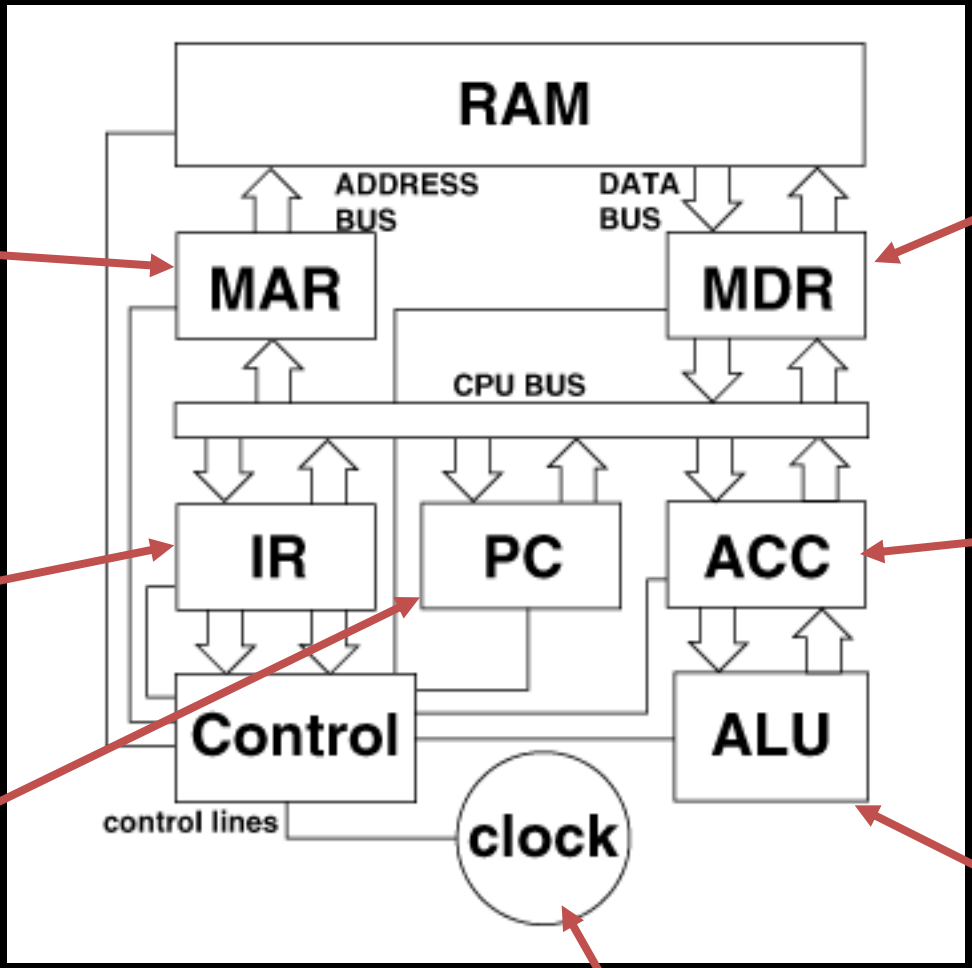


memory data register

accumulator (work register)

arithmetic logic unit

CPU Function



memory address register

memory data register

instruction register

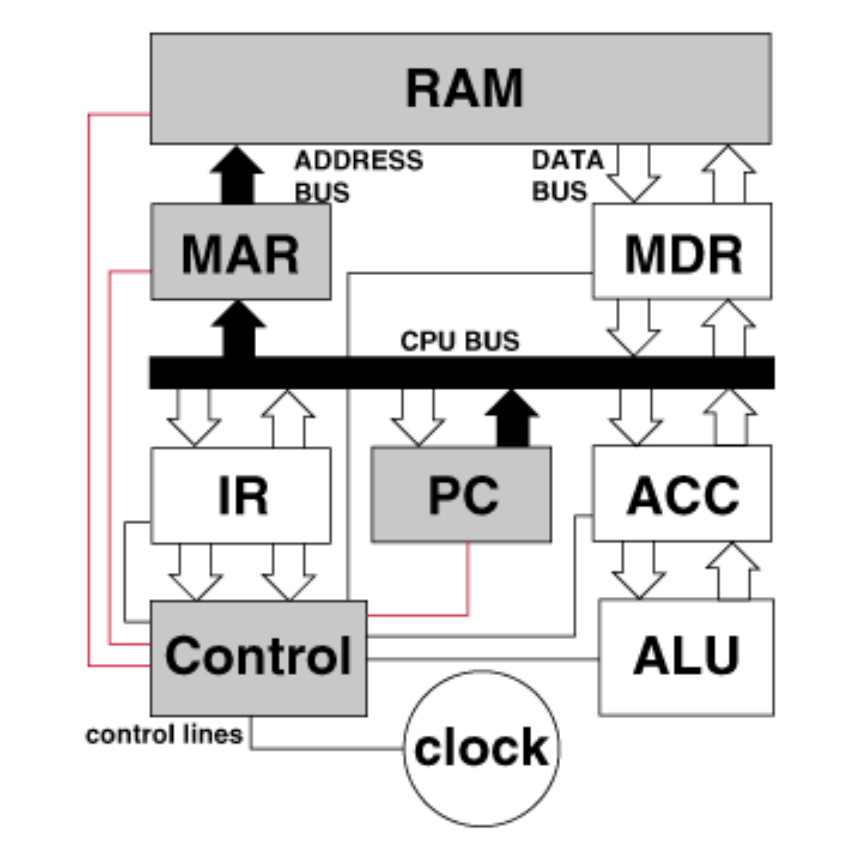
accumulator (work register)

program counter

arithmetic logic unit

system clock

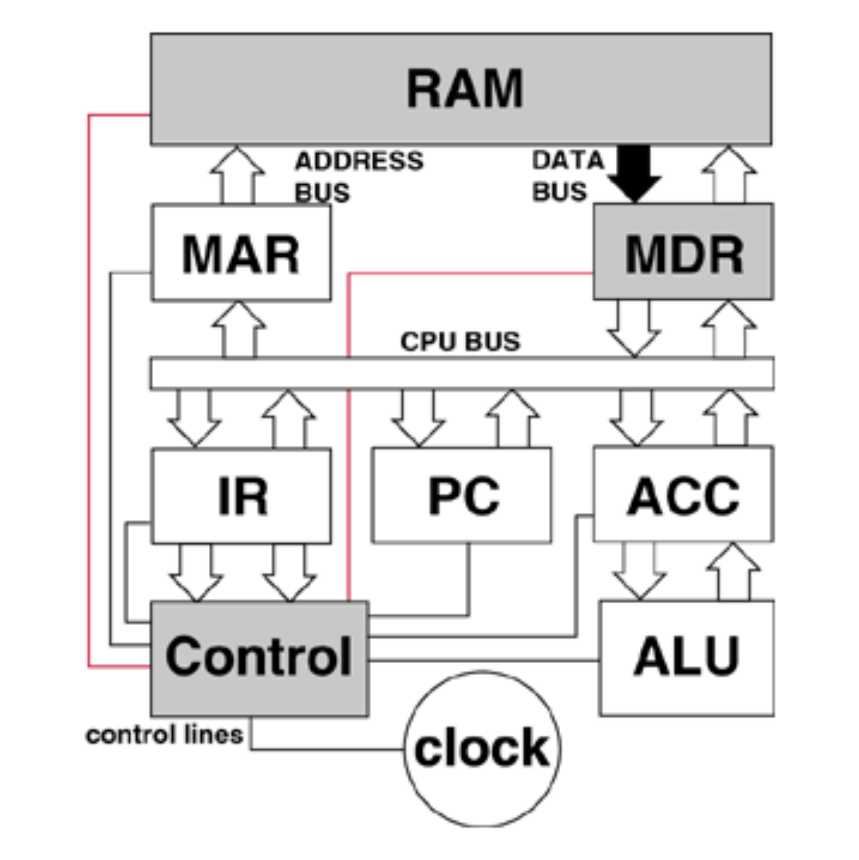
FETCH the Instruction



1. address of the next instruction is transferred from PC to MAR

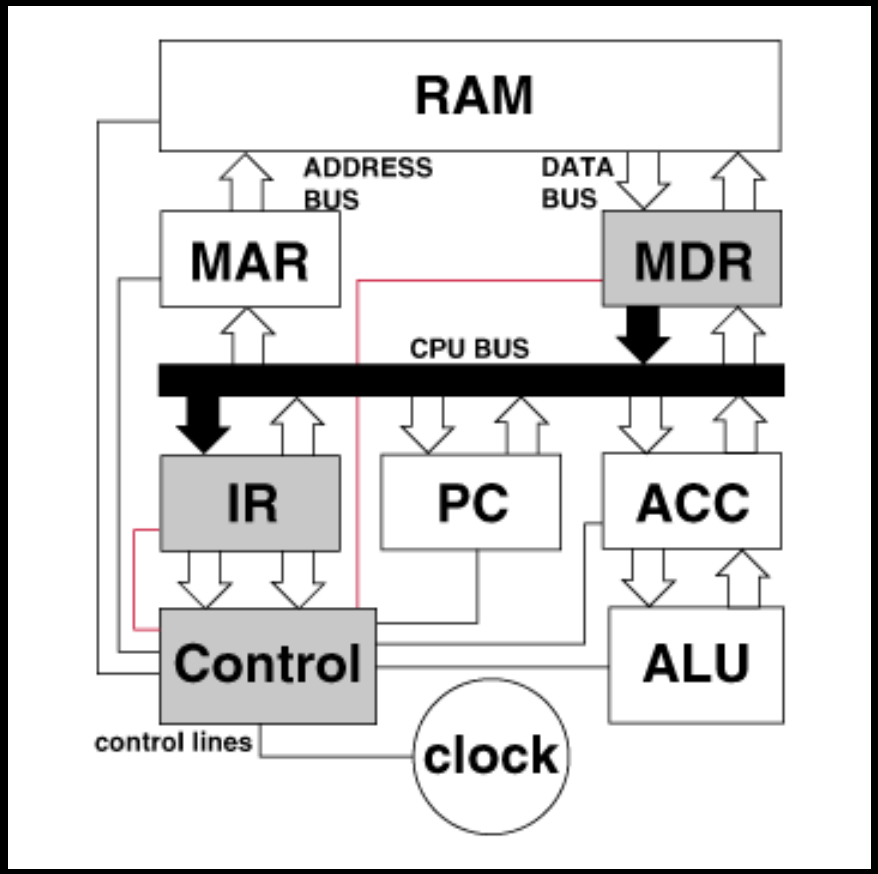
2. the instruction is located in memory

FETCH the Instruction



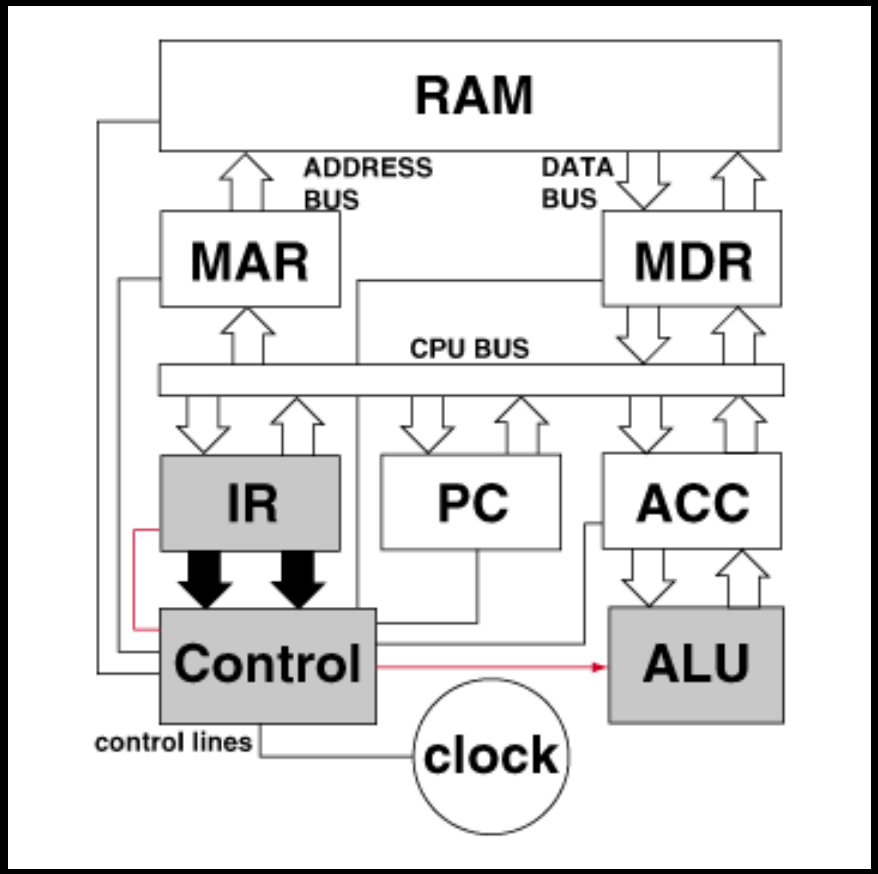
3. instruction is copied from memory to MDR

DECODE the Instruction



instruction is transferred to and decoded in the IR

EXECUTE the Instruction



control unit sends signals to appropriate devices to cause execution of the instruction

General Register Organization