Assignment-10
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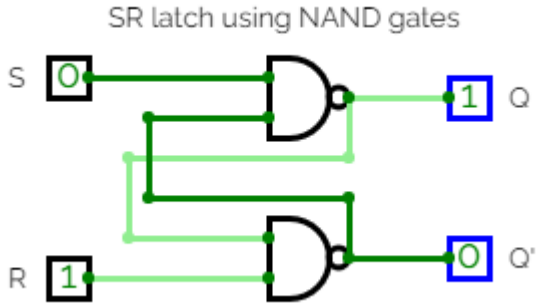
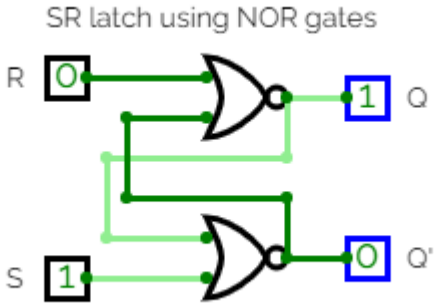
- **Problem 1:** Design a SR latch using NAND gates.



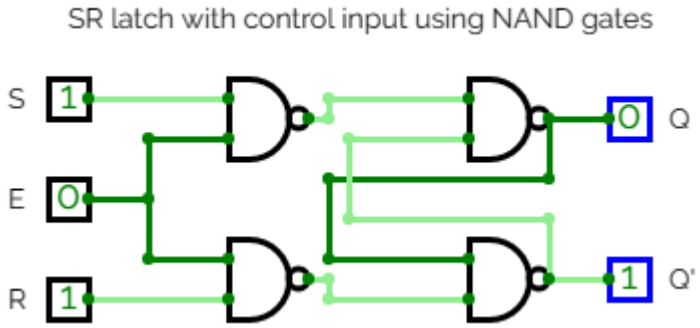
S	R	Q(n)	Q(n+1)
0	0	0	INVALID
0	0	1	INVALID
0	1	0	1 (Reset)
0	1	1	1 (Reset)
1	0	0	0 (Set)
1	0	1	0 (Set)
1	1	0	0 (Memory)
1	1	1	1 (Memory)

- **Problem 2:** Design SR latch using NOR gates.



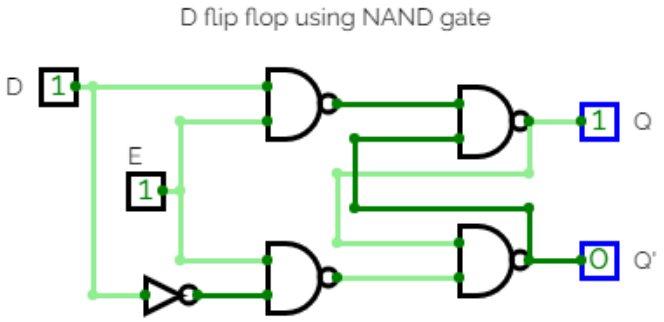
S	R	Q(n)	Q(n+1)
0	0	0	0 (Memory)
0	0	1	1 (Memory)
0	1	0	0 (Reset)
0	1	1	0 (Reset)
1	0	0	1 (Set)
1	0	1	1 (Set)
1	1	0	INVALID
1	1	1	INVALID

- **problem 3:** Design SR latch with control input using NAND gates.



Clog	S	R	Q(n)	Q(n+1)
Untriggered	X	X	0	0 (Memory)
Untriggered	X	X	1	1 (Memory)
Triggered	0	0	0	0 (Memory)
Triggered	0	0	1	1 (Memory)
Triggered	0	1	0	0 (Reset)
Triggered	0	1	1	0 (Reset)
Triggered	1	0	0	1 (Set)
Triggered	1	0	1	1 (Set)
Triggered	1	1	0	INVALID
Triggered	1	1	1	INVALID

- **problem 4:** Design D flip flop using NAND gate.



Clock	D	Q(n)	Q(n+1
Untriggered	X	0	0
Untriggered	X	1	1
Triggered	0	0	0
Triggered	0	1	0
Triggered	1	0	1
Triggered	1	1	1