ECE335 Introduction to Electronic Devices

Project 2

Design a Deep Submicron NMOS

12/06/2023

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1 Introduction

The 65nm CMOS transistor is a state-of-the-art technology that transformed semiconductor manufacturing. The 65nm CMOS transistor device is categorized as Low Power (LP), High Speed (HS), and General Purpose (G) in order to cover the entire foundry application space with diverse performance and power requirements [1]. Compared to 90nm CMOS transistors, this technology offers 1.3 times faster speed, two times higher density, and 0.6 times lower power [4]. The transistor's intrinsic CViI index and gate length (Lg) are decreased by 20 percent compared to the 90nm node so as to satisfy the AC performance requirement in all three application segments of this 65nm CMOS transistor [1]. The 65nm node transcends its size, making it appropriate for various applications, from consumer electronics to telecommunications [5].

2 Background Reading and Getting Started

Extension doping is a method used to finely control the doping levels in a transistor's drain and source extension areas. The extension sides are found near the channel of transistors. Extension doping modulates the threshold voltage of a transistor, which is vital in controlling its ON/OFF behaviour [6]. Doping the extension areas of a transistor enables precise tuning of its performance, especially its threshold voltage. In the case of the 65nm-node CMOS transistor, extension doping helps the device achieve optimal short-channel control and mitigate problems like drain-induced barrier lowering (DIBL) [1]. Halo doping entails introducing dopant ions into the substrate near the drain and source regions but deeper than the extension regions [6]. The purpose of this technique is to control the charge distribution in the channel region. As a result, halo doping controls the threshold voltage of the transistor and improves its short-channel behaviour. This technique assists in addressing issues associated with sub-threshold swing and threshold voltage roll-off, which results in improved transistor performance. A spacer contains dielectric material and is incorporated in transistor fabrication to regulate the lateral diffusion of dopants during the ion implantation process [6]. In a CMOS transistor, spacers are installed on the sidewalls of the gate structure. Their function is to define the channel length and inhibit excessive lateral diffusion of dopants into the channel region [7].

(i) extension doping: The function of extension doping is to push out N-wells to form source and drain regions.

(ii) halo doping: The halo doping is to suppress the short channel effect, and the shallow junction formed helps to reduce the channel leakage current effect between the source and the drain.

(iii) spacer: In order to prevent a large dose of source-drain injection from being too close to the channel and resulting in the channel being too short or even source-drain connection, side walls (spacers) are formed on both sides of the polysilicon gate after CMOS LDD injection forms pocket doping.

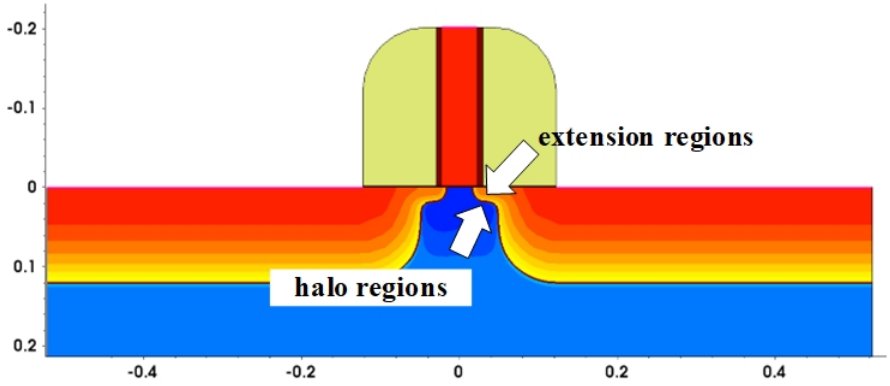

Fig. 1 2D doping concentration of the default transistor

Table 1 Acronyms Definition

Acronyms	LP	G	HS	IO	LVT/HVT
meaning	Low Power	General Purpose	High Speed	Input/Output	Low/High-voltage Threshold

A low Ioff means that the leakage current is low when the device is turned off, indicating that the device can be turned off quickly, so the device can be suitable for high-speed applications. High Ion means that the on-resistance is small when turned on, indicating low heat, and this transistor is suitable for desktop applications such as cpus and Gpus. According to Table 2, it is the case for both nMos and pMos that the Ioff is low and Ion is very high.

Table 2 Device Option for 65nm Technology [1]

TSMC Process W=1um		LP		G		HS		IO	
Device		STD	HVT	STD	HVT	LVT	STD		
Vdd (V)		1.2		1.0		1.0		1.8	2.5
EOT (nm)		1.95		1.4		1.2		28	~53
Lpoly (nm)		55		45		<40		145	265
nMOS	Ioff (nA/um)	0.2	0.01	26	4	400	80	< 5p	< 1f
	Ion (uA/um)	570	445	795	665	1130	1010	660	580
pMOS	Ioff (nA/um)	0.2	0.01	26	4	400	80	< 5p	< 1f
	Ion (uA/um)	263	190	340	282	>540	>475	300	290
Ring Target (ps)		<11.5	<14.5	<6.7	<8	<5	<5.5	<23	<32

3 Design and Results

Ioff is Id at Vds = Vdd and Vgs = 0V. Ion is Id,sat at Vds = Vgs = Vdd. In the requirement Vdd=1v, we revise Vgmin to 0v and Vgmax to 1v so it is 2 different voltage values. The original structure has a Ion of around 500 uA/μm and the Ioff is greater than 35 nA/μm, achieving around 200 nA/μm. Therefore we want to increase the Ion current and decrease the Ioff current.

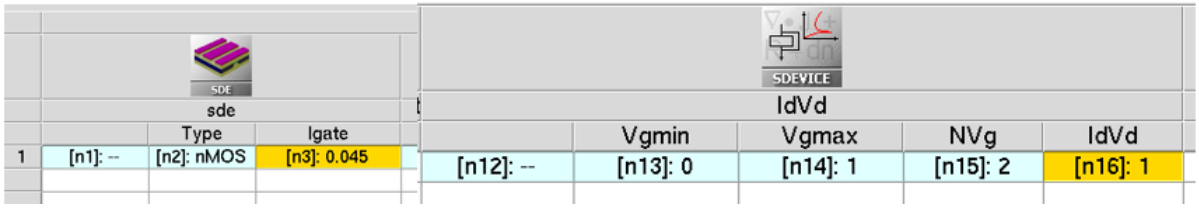

Fig. 2 SWB capture

Table 3 Sde structural modification and summarized transistor specifications

Item	Xjext	Tox	halo doping	sub doping	extension doping
Before	0.026 μm	1.4 nm	$1.5\times1018\ cm^{-3}$	$1\times1017\ cm^{-3}$	$1\times1019\ cm^{-3}$
After	0.036 μm	1nm	$3\times1018\ cm^{-3}$	$1\times1016\ cm^{-3}$	$3\times1019\ cm^{-3}$

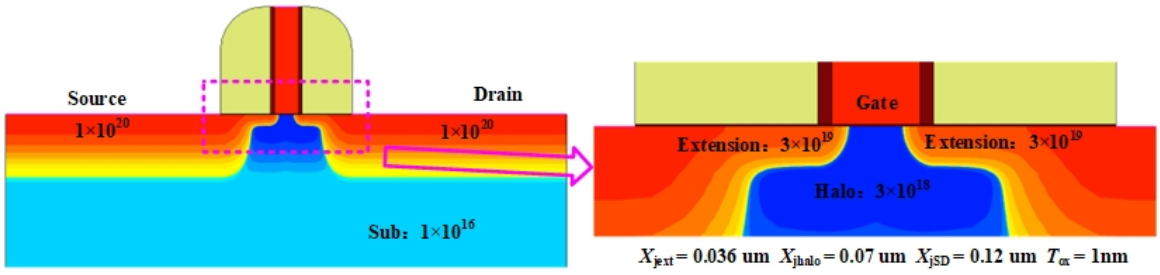

Fig. 3 2D doping density profile with parameter labeling and enlarged channel region

First, decreasing the substrate doping concentration and increasing the halo concentration can effectively reduce Ioff, but at the same time decreasing the substrate doping concentration and increasing the halo concentration can reduce Ion. Therefore, let Ioff reach a reasonable value, and then take external measures to make Ion meet the conditions. Therefore, the halo concentration was increased from 1.5×1018 cm-3 to 3×1018 cm-3, so that the Ioff reached the target value of 25 nA/um. In addition, the sub concentration can not be too high, too high will lead to the PN junction formed by the leak-substrate is prone to Zener breakdown in the reverse bias, which will lead to an increase in Ioff, so it is necessary to reduce a little substrate concentration, sub doping from 1×1017 cm-3 to 1×1016 cm-3.

Second, in order to increase the saturation current (Ion), the following measures can be taken to increase the saturation current. Increasing the extension depth and concentration can shorten the channel length. Reducing the channel length can make the channel easier to invert, so a higher channel electron concentration can be obtained, and eventually an Ion can be increased. Or reducing the thickness of the oxide layer can also make the channel easier to invert, and ultimately increase the saturation current. In short, making the channel easier to invert can increase the saturation current. Therefore, the measures taken are as follows: Xjext changed from 0.026m to 0.036m, Tox changed from 1.4nm to 1nm, extension doping changed from 1×1019 cm-3 to 3×1019 cm-3.

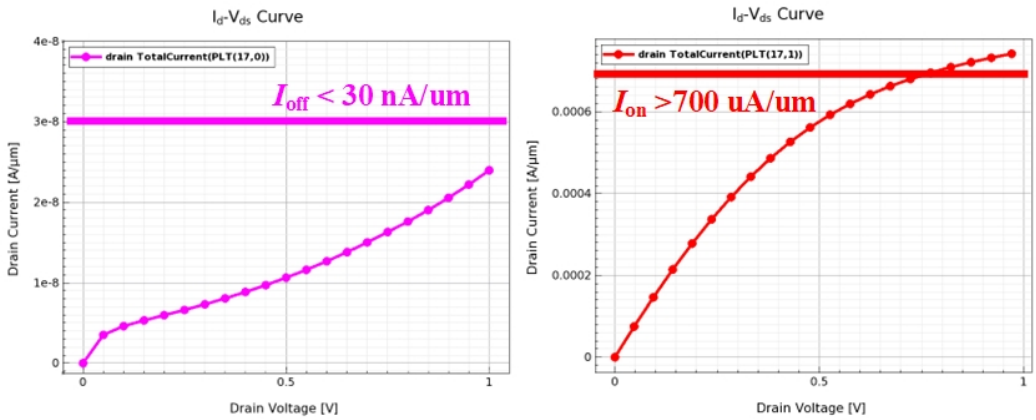

Fig. 4 Achieved Id-Vds characteristic curve for the nMOs structure

In addition, the plot for Id vs. Vgs where 0 < Vgs < Vdd (Vdd is the supply voltage) for Vds = 50 mV (low drain voltage, linear regime) & Vds = Vdd (saturation regime) are given and after running the simulation, the result is shown below.

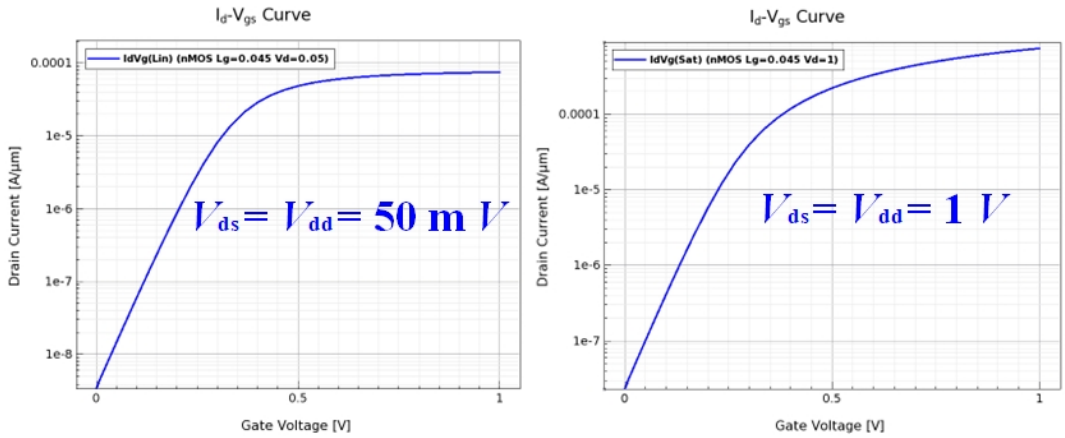

Fig. 5 Transfer characteristic curve when Vds = 50 mV, transfer characteristic curve when Vds = Vdd

The subthreshold swing (SSsat) after running the simulation is 79.349 mV/dec, which corresponds to a subthreshold swing below 100 mV/dec mentioned in the paper. The linear threshold voltage and saturation threshold voltage for our design are shown below, which also aligns with the values in the TSMC paper with a 45nm gate length.

Table 4 Linear threshold voltage and saturation threshold voltage

		Variable Values								
	PlotIdVd									
d		Vtgm	VtiLin	IdLin	SSlin	gmLin	IdSat	Ioff	VtiSat	SSsat
1	[n17]: --	0.275	0.238	7.490e-05	80.379	2.313e-04	7.422e-04	2.403e-08	0.162	79.349

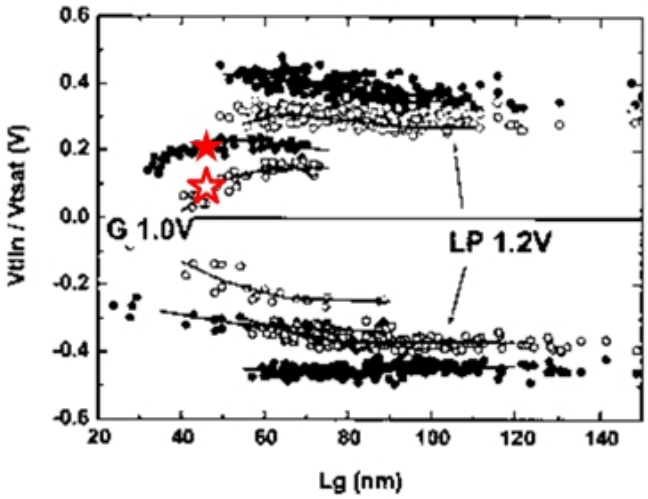

Fig. 6 Vt roll-off of G and LP technology (Vtln is solid red star)

Regarding DIBL, taking an n-channel MOSFET as an example, two back-to-back diodes are formed in the N-source region and the N-drain region. Vds is inversely biased to drain PN. For long channel MOSFETs, the Vds falls almost entirely to the drain PN junction and does not affect the source PN junction. However, in a short-channel MOSFET, because the channel length is very short, part of the power line originating in the drain zone will end in the source zone through the channel, thus reducing the barrier height between the source and drain zone. This phenomenon is called the drain-induced barrier lowering, or DIBL effect. The shorter the channel length L, the greater the drain-source voltage V, and the more the barrier height is lowered. When the barrier height between the source and drain is reduced, it is equivalent to the positive bias of the source PN junction, and electrons are injected into the channel from the source zone, thus increasing the drain current.

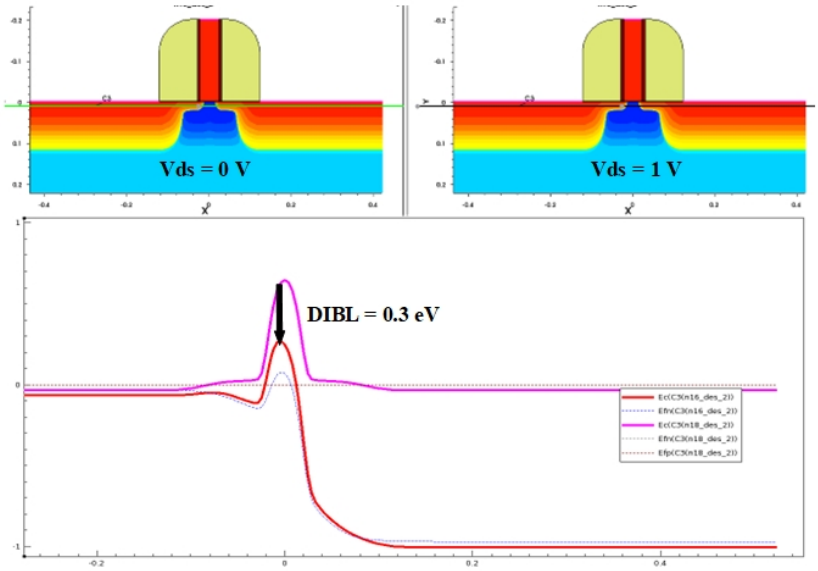

Fig. 7 DIBL=0.3eV in simulation

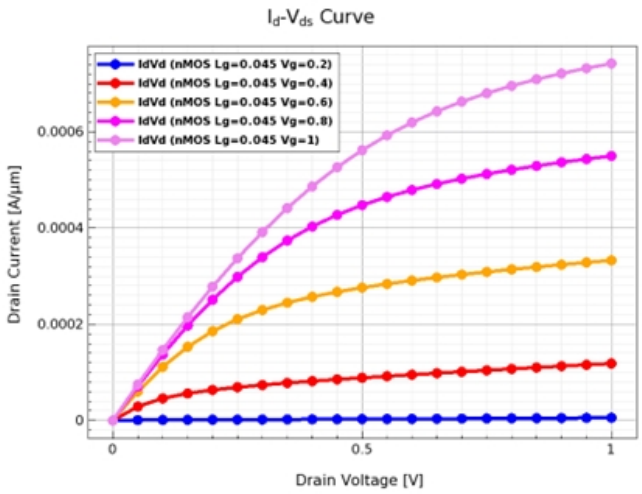

Fig. 8 Id vs Vds for Vgs = 0.2, 0.4, 0.6, 0.8, and 1.0V for $0 \leq$ Vds $\leq$ Vdd forward output characteristic curve

The ideal square law dependence of the ideal MOSFET states that the drain-source current (Ids) is proportional to the square of the effective gate voltage (Vgs – Vth).

$$I_{ds} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 \tag{1}$$

In an ideal square law model, for a given Vgs above the threshold voltage, the drain current Ids would increase quadratically with Vgs in the saturation region. The plot we got from the simulation ideally shows this quadratic relationship in the saturation region.

From the saturation region onwards, ideally, the current would remain constant as Vds increases, indicating that the device has entered the saturation region and the current is now only a function of Vgs. However, in real MOSFETs, the drain current continues to increase slightly due to channel length modulation, which is not accounted for in the basic square law model.

In the plot we generated, as Vgs increases, the drain current also increases, which is different from what the ideal square law expected. The onset of saturation can be observed when the curves start to flatten, indicating the transition from the triode to the saturation region.

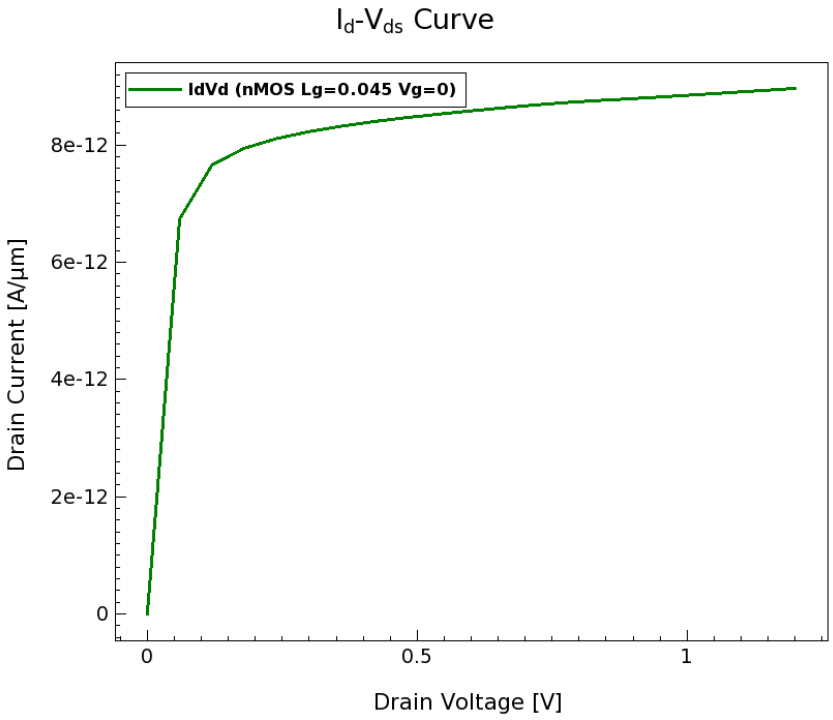

Fig. 9 Ioff

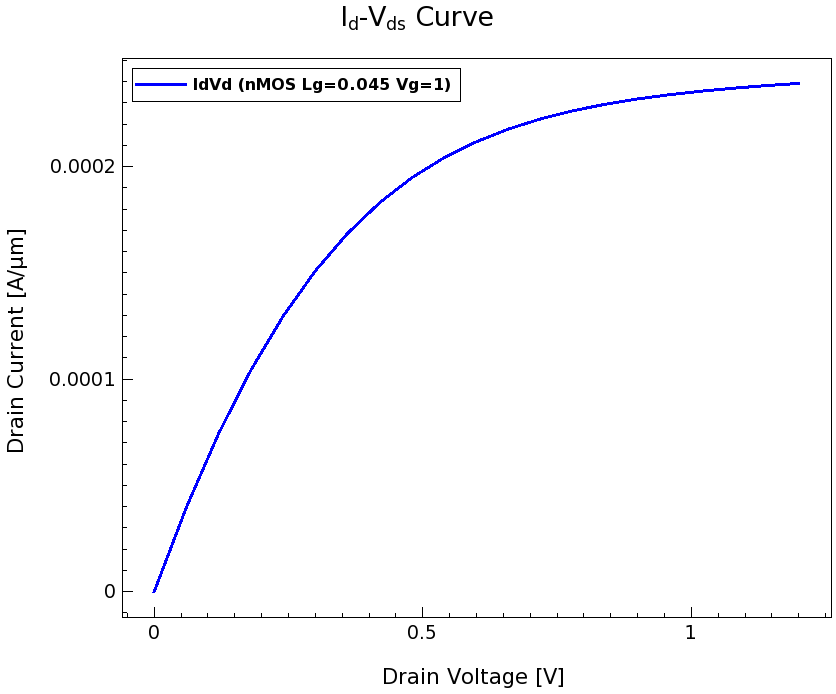

Fig. 10 Ion

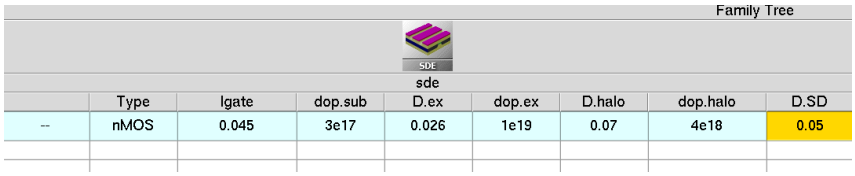

Fig. 11 SWB Capture

In terms of a LP HVT nMos design, the substrate doping was increased to set at 3e17, a level that helps in managing threshold voltage and suppressing leakage currents. The extension doping concentration of 1e19 and the extension depth was both maintained at 0.026 μm. Additionally, the halo doping profile with a depth of 0.07 μm and a concentration of 4e18. Overall, the design achieves the target Ioff of $\leq$ 0.01 nA/μm and Ion of $\geq$ 250 μA/μm at a Vdd of 1.2V, not meeting the goal of Ion of $\geq$ 445 μA/μm .

References

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