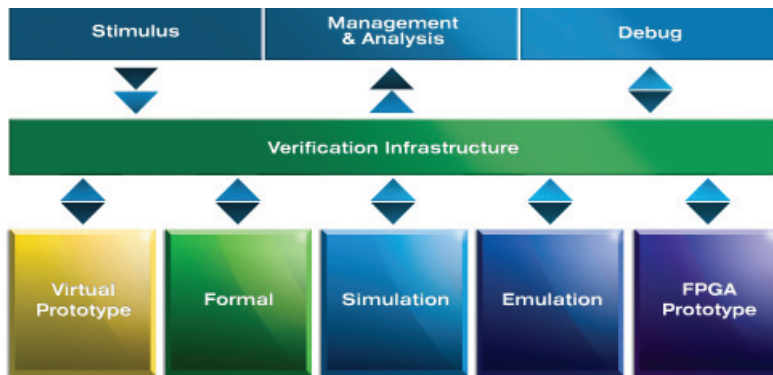# The Questa Verification Solution

The Mentor Graphics Enterprise Verification Platform (EVP) is transforming verification by bringing powerful engines and platforms together to deliver high performance verification from prototype to silicon.

Uniting Simulation, Formal, and Emulation

The Mentor Graphics® Enterprise Verification Platform™ is transforming verification by bringing powerful engines and platforms together to provide a unified user experience from architectural exploration and virtual prototyping to full-system modeling and execution on the desktop and in the lab. Built on our best-in-class engines, the solution starts at the architecture level with Vista, a complete TLM 2.0 based solution for architecture design, analysis, verification and virtual prototyping that enables system architects and SoC designers to make viable architecture decisions while allowing hardware and software engineers to validate their work.

As an implementation is refined, the focus shifts to Questa®, where formal and simulation engines provide a comprehensive platform to verify complex SoC designs. Providing the industry's most complete native support for SystemVerilog, Verilog, VHDL, SystemC, PSL and UPF, as well as automated formal applications, Questa quickly and accurately verifies your design as you go from block-level to assembling your system. Questa eliminates the barriers to hardware acceleration, combining the functionality and observability of simulation-based verification with the speed of emulation.

Enterprise Verification Platform: Unified Verification from Simulation to Emulation

- Simulation acceleration with Veloce TBX for up to 1000X performance gain
- Common coverage database and flows
- Unified verification IP for acceleration and reuse

Industry-Leading Solutions

- Intelligent stimulus generation and coverage closure
- Integrated verification management and analysis
- High performance/capacity unified debug
- Power-aware verification

Best-in-Class Technology

- High-performance multi-language simulator
- Formal-based apps and verification
- HW/SW co-verification
- UVM methodology

The Veloce® emulation system provides the speed and capacity you need to verify software running on your hardware, with up to 2 billion gates to support full SoC RTL simulations running with signal-level and transaction-based testbenches. The powerful Veloce OS3 Enterprise Server turns what used to be a project-bound engineering lab instrument into a datacenter-hosted global resource while enabling advanced verification features, including PSL/SystemVerilog assertions, functional coverage, and UPF for low-power verification. Unification comes from a common infrastructure layer and VIP that abstract the verification process from the underlying engines. Mentor Verification IP, built using standard UVM/RTL, is designed for both simulation and acceleration modes, providing a smooth transition from simulation to emulation.

Debug takes up the largest percentage of verification time, and the new Mentor Visualizer™ debug environment provides a single integrated solution for both simulation and emulation with the capacity and performance to handle the largest SoC designs. Visualizer handles RTL, gate-level and transaction-level debug, including a complete set of native UVM and SystemVerilog class-based debugging capabilities as well as protocol and low-power UPF debug, and automatic tracing to quickly pinpoint the cause of errors. Veloce OS3 enables off-line software debug via Codelink™, freeing up the emulator to support hundreds of engineers at speeds of up to 100 MHz, enabling maximum debug productivity and speeding up the process of OS bring-up.

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Questa Verification Platform

Functional verification continues to evolve in response to the growing complexity of SoC designs. Besides the sheer size of designs, the inclusion of multiple embedded processors and advanced interconnect systems, increasing software content and the configurability required by multi-platform based designs require a functional verification platform that unifies a broad arsenal of verification solutions. The key to verification success is to decompose the problem and use the best solution for each aspect of the system. This places tremendous importance on the verification plan and the ability to collect metrics throughout the process and across all verification tasks to track progress against the plan, allocate and manage resources efficiently, and identify trends as the project progresses against schedule.

Software has become a major component of SoC system functionality, creating new requirements for block-to-system verification reuse and the need for system verification and debug. While software testing of SoC integration and basic functionality as well as the verification of low level driver software can be accomplished in simulation, long, complex sequences that exercise system functionality demand acceleration with full debug visibility. To avoid wasting cycles at the system level, it is critical to identify bugs as early as possible in the process. Questa lets you apply CDC verification, formal verification, mixed-signal verification, intelligent automation and other powerful technologies to maximize the effectiveness of your verification at the block- and subsystem-level so your system-level verification can focus on system-level functionality, including software, without having to worry about lower-level bugs taking away from your productivity. No one wants to compromise product quality. However, time-to-market pressures dominate SoC projects. To deliver quality within schedule requires improving the time to achieve coverage and quality goals and improving debug productivity.

The platform is composed of several technologies, each powerful on its own. Applied together, along with a comprehensive database and best-in-class verification management tools, these technologies deliver a powerful answer to the spectrum of verification problems.

Unified Simulation, Coverage, and Debug Technology built on a best-in-class simulator. The Questa Advanced Simulator achieves industry-leading performance and capacity through very aggressive, global compile and simulation optimization algorithms for SystemVerilog and VHDL. Questa also supports very fast turnaround time flows and effective library management while maintaining high performance with unique capabilities to pre-optimize and reuse, enabling dramatic regression throughput improvements of up to 3X when running a large suite of tests. The Visualizer debug environment provides high-performance, high-capacity debugging for both Questa and Veloce, enabling the use of the same debug environment from simulation to emulation and other engines.

Intelligent Testbench Automation automatically generates verification stimulus and can be applied at the block, subsystem and SoC levels. The technology avoids redundancy and can achieve target coverage more than 10X faster than is possible with constrained random testing. The technology can be applied to shorten time to coverage or to achieve more comprehensive verification by enabling more tests to run in the same amount of time.

Verification IP consists of reusable testbench building blocks. Questa Verification IP (QVIP) is a performance-optimized library of standard SV UVM components for simulation with support for ARM® AMBA®, Ethernet, MIPI®, PCIe® and USB and many other protocols. Using QVIP frees up engineers to focus on design-specific verification and enables tests to be reused in acceleration with Veloce. QVIP includes advanced transaction-level debug, comprehensive protocol assertions, functional coverage, test plans and test sequences that together can be used to validate protocol compliance and accelerate time-to-RTL-signoff.

The Questa Memory Library comprises an extensive range of fast and accurate DRAM and Flash memory models. These can be dropped into any testbench to verify any memory subsystem. For speed, we provide backdoor access and on-the-fly reconfiguration. For correctness and completeness, we provide extensive assertions and coverage. For debugging, we provide powerful transaction-to-pins debug capabilities.
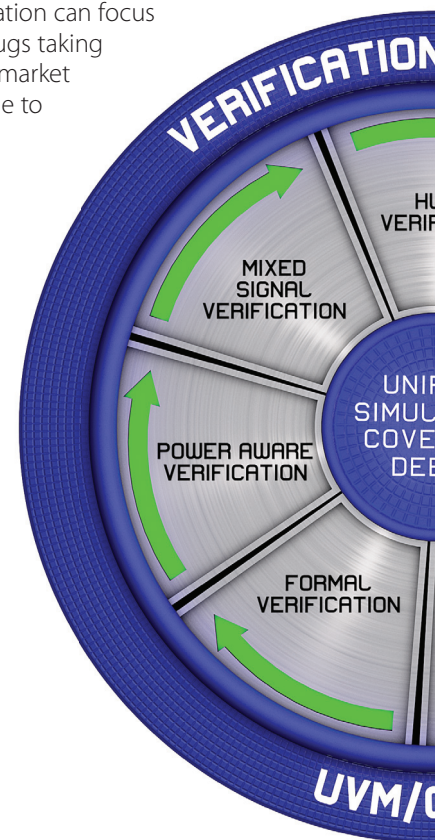
Questa CDC Solutions identify errors that have to do with clock domain crossings – signals (or groups of signals) that are generated in one clock domain and consumed in another. It does so with structural analysis and recognition of clock domains, synchronizers, and low power structures (via UPF); and with generation of metastability models for reconvergence verification. The technology checks all potential failure modes and presents to the user familiar schematic and waveform displays. Additionally, in concert with simulation this technology can be used to inject metastability into functional simulation to verify the DUT correctly processes async clocks. Finally, with Questa ResetCheck this technology has been extended to cover structural checking for reset domain crossings, reset trees, gated reset signals, etc.

Questa Formal Verification solutions complement simulation with a full spectrum of formal tools ranging from fully automatic formal solutions to formal apps and property checking. At the core of the platform is a set of high performance property checking engines that offer exhaustive verification early in their design cycle with custom coded SVA/PSL/OVL assertions. Building on this foundation are a wide range of automated formal apps for verification tasks well suited to exhaustive formal analysis such as RTL design checks, X-Checking, coverage closure, property generation, connectivity checking, control and status register verification, interface protocol validation, and post-silicon debug.

Questa Low Power Verification enables early (RTL) verification of active power management applied to a complex design, to ensure that the power management architecture and behavior are correct and that the design will operate correctly under active power management. Questa PowerAware simplifies the verification process through a comprehensive suite of static checkers for checking the consistency of the power management architecture and dynamic checks for automated error detection. Questa PowerAware also provides visualization of power management architecture and behavior, coverage data collection, and test plan generation for power states and state transitions. Based on the latest industry-standard IEEE 1801-2015 UPF for specification of active power management, Questa PowerAware integrates well with other UPF-based tools to support multi-tool and multi-vendor low power design and verification flows.

Questa® ADMS™ verifies complex analog/mixed-signal designs. The technology integrates four high performance engines: Eldo® for general purpose analog, ADiT™ for fast transistor-level, Eldo RF for modular steady state and Questa Sim for digital. Its combination of languages and algorithms allows for both top-down design and bottom-up verification supporting multiple levels of abstraction and performance from Spice netlists to Real Number Models.

Questa HW/SW Verification provides processor-based system-level verification, using software tests to verify RTL and hardware/software integration. The technology comes with a host of advantages such as ensuring chip power management, loading and booting operating systems, and running software applications. It accelerates simulation, enables instant replay, and offers virtual emulation — all of which serve to trim debugging time.

Questa Verification Management manages the data complexity, guides the process and provides automation across all verification engines to improve verification productivity. It offers analysis and optimization features built upon the Unified Coverage Interoperability Standard database (UCISDB), with results and trend analysis, test plan tracking and run management. Questa Verification Management efficiently ties all verification-related tasks together and gives all parties — system architects, software engineers, designers and verification specialists — real-time visibility into the project. This visibility helps to hit market windows on schedule, manage risk and improve throughput and debug turnaround times.

UVM provides a "methodology platform" so you can build your verification environment to take advantage of Questa technologies targeted to your specific application. The UVM library provides the infrastructure that enables you to assemble configurable VIP components and environments that can be reused from block-to-system and from project- to-project. For stimulus generation, Questa's Intelligent Testbench Automation can be seamlessly integrated into your UVM environment. The modularity of UVM lets you reuse your transaction-level testbench, using both the Questa and Veloce platforms, while also letting you gather coverage data that you can later analyze using Questa Verification Management. The UVM framework provides a quick start to creating a UVM testbench and adopting UVM for the first time. The Visualizer debug environment has unique UVM and SystemVerilog debug capabilities that make it easy to debug your testbench alongside your design, too.

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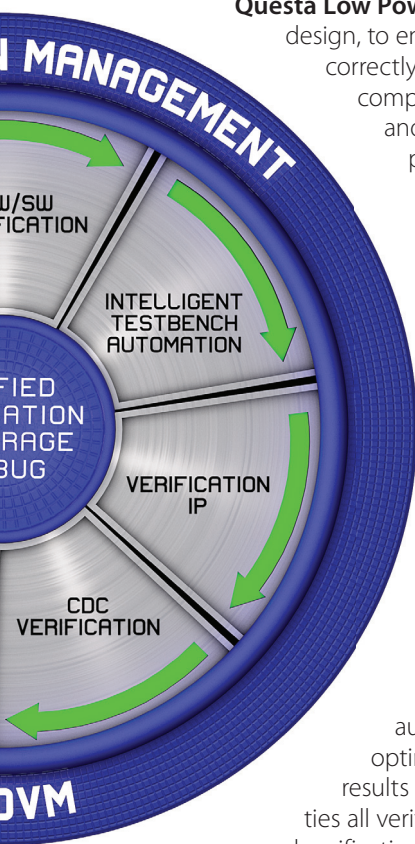
Verification Expertise

Mentor Graphics provides ample resources to help you get started adopting advanced verification techniques.

Verification Academy

The Verification Academy is organized into a collection of free online courses and resources, focusing on key aspects of advanced functional verification designed to mature an organization's verification process. Course topics include assertion-based verification, FPGA verification, clock-domain-crossing verification, Intelligent Testbench Automation, power aware simulation, and many more. Each course consists of multiple sessions allowing the viewer to pick and choose topics of interest as well as revisit topics for future reference.

The Verification Academy is the most complete UVM online resource collection. You'll find everything you need to get up to speed on UVM, whether it's downloading the kit(s) or participating in online or in-person training. The UVM courses provide a great overview of methodology concepts, introductory to advanced, with videos that walk through useful code examples. The UVM Online Methodology Cookbook is an online textbook to show you in more detail how to use the various features of the methodologies to create reusable verification components and environments. (www.verificationacademy.org)

Consulting and Training

Mentor Consulting Verification Services offers solution-driven consultants who will dramatically reduce your verification process times while improving quality. Unlike other EDA consulting services or third party consultants, Mentor Consulting's highly experienced Verification Services team offers customized solutions and proven, structured processes to ensure projects are delivered on time and to specification, and with greater probability of first-pass success. Mentor Graphics Education Services offers a full range of learning solutions developed specifically for electronics designers and engineers engaged in advanced verification. Users can choose the type of training that best suits their needs and schedule. These choices include unique Live Online Training, training and seminars given in Mentor Graphics training centers around the world, and on-site training and mentoring specifically designed for your company.