Computer Organization Lab5

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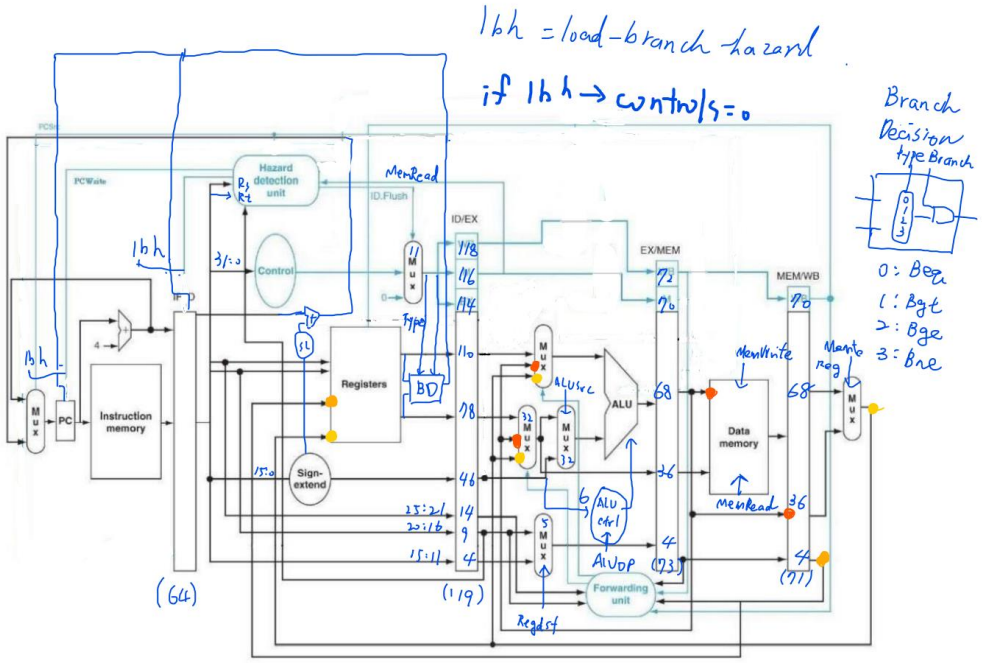
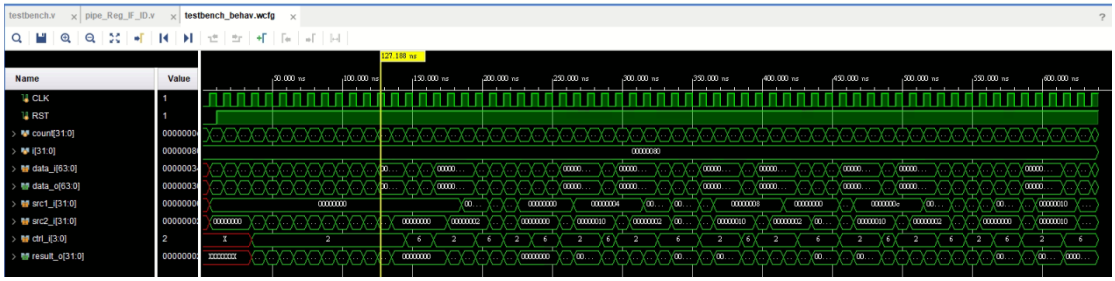
Architecture diagrams:



Hardware module analysis:

The module contains hazard detection unit as well as forwarding unit, the strength is it can boost more efficiency and reduce more clock cycles than the previous designs; however, it is complicate and prone to design errors, especially with data hazards and control hazards. Another thing that has to be careful is that when facing load branch and reg_write branch, as we move the branch comparison from MEM stage to ID stage, we cannot use forwarding technique to send signal toward the branch, so we have to stall 2 cycles to have it saved in the memory then retrieve the data.

Finished part:



We can observe that sometimes the program counter (the data I/O column) will stall for either 1 cycle or 2 cycles, depending on the hazard it detects.

Problems you met and solutions:

In this lab I met 2 major problems. The first one is that I found the architecture on the slides need to be integrated and some wires need to be trimmed to fit the design. For example, I realized that improper design may cause infinite loop interruption so I delete the wire from branch decision to the hazard detection unit as it may cause infinite loop when BD affect HDU and flush the control, then again affect BD. The other obstacle is that I in the beginning didn't discover that except for the general load-use hazard and control hazard, we need to handle reg_write-branch and load-branch instructions, as we move the branch to ID stage, we have to stall 2 cycles to wait for the data written into the register. This cost me the whole night to realize the problem then fix it.

Summary:

I think this lab is the most difficult one then the previous ones. However, I've learned a lot from scratch to a pipeline CPU with HDU and forwarding unit. Although I often had a hard time debugging every time with some trivial errors or big mistakes, I still enjoy these labs and eventually gained sense of achievement finishing them.