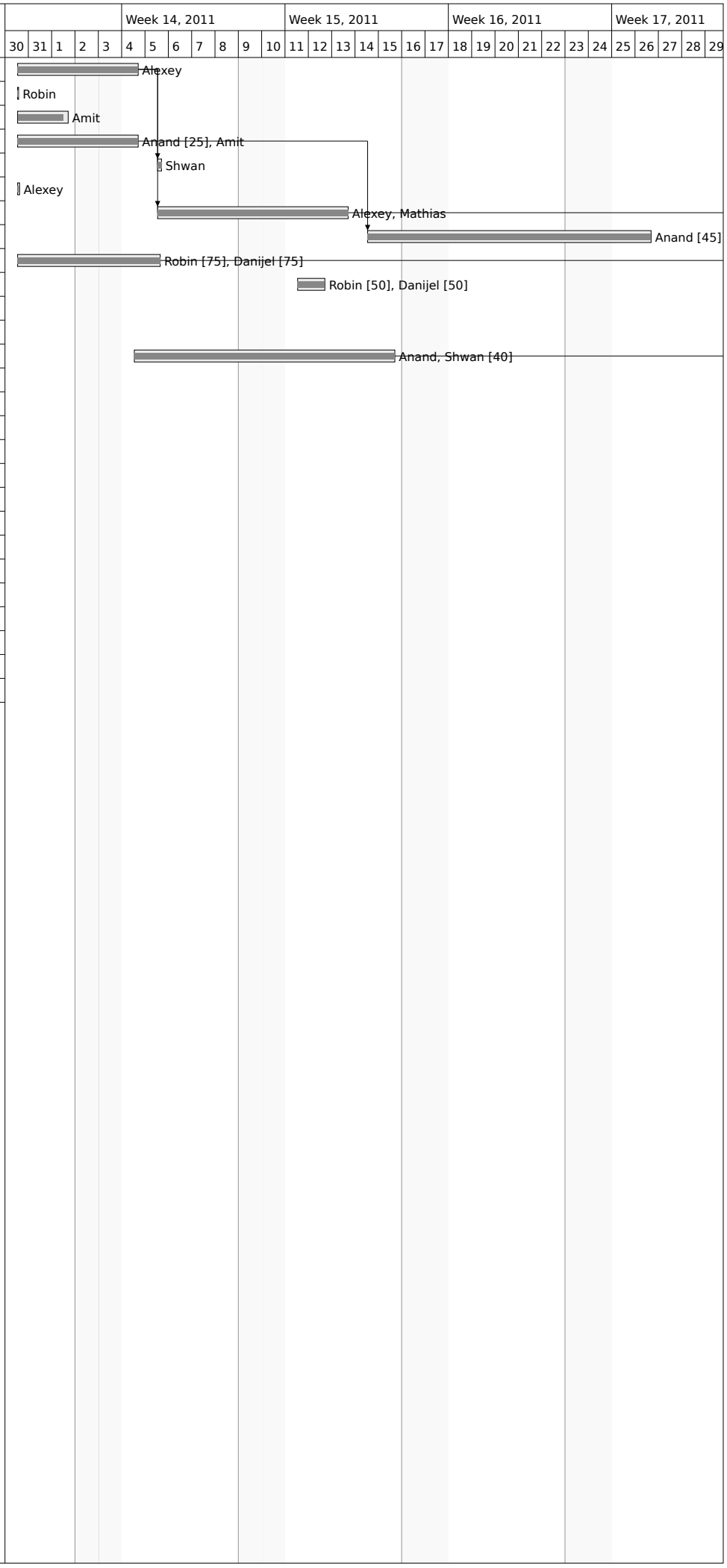
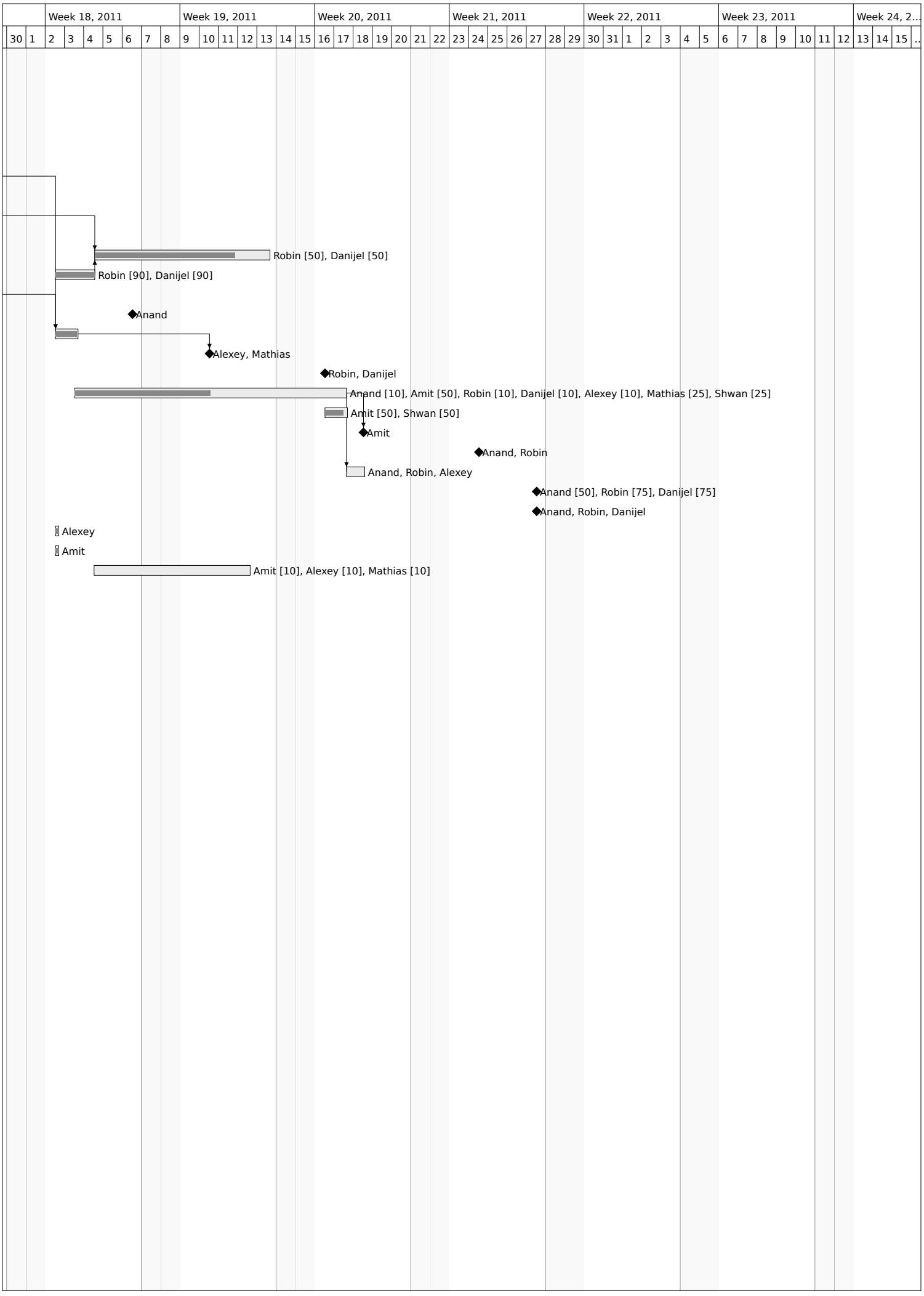
Name	Work
Verify Serialfilter.vhd	4d
Avarerage can satuaret ?	1h
Interface VB.net	3d
interface vhdl	5d
clean up the data types	1d
databuffer	2h
Verify EQ main	14d
Testbench the rx tc vhdl parts	4d
Verify Driver Stage	7d
Calculate Transistor Dimensioning	2d
Creat Full custom Layout (Analog)	7d 2h
Creat Mixed Signal Verification models	4d
Complete the FPGA code	14d
Milstone: Verify the FPGA code	
verification of the system	2d
Milstone: Submit Formal verification of the system	
Milstone: Submit the Final VAMS results	
Write The Final Report	15d
Write The Final Report - project	2d
Tolgate : Submit Final Report	
Milstone: Final Presentation	
Final Presentation	2d
Milstone: Exctract Pre Final Layout	
Milstone: Exctract Final Layout	
Debug the GainAmplifier	1d
Debug the RX TX vhdl part	1d
Try out the RotatingBuffer again	2d




Week 18, 2011
Week 19, 2011
Week 20, 2011
Week 21, 2011
Week 22, 2011
Week 23, 2011
Week 24, 2...
30 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 ..
Robin [50], Danijel [50]
Robin [90], Danijel [90]
Anand
Alexey, Mathias
Robin, Danijel
Anand [10], Amit [50], Robin [10], Danijel [10], Alexey [10], Mathias [25], Shwan [25]
Amit [50], Shwan [50]
Amit
Anand, Robin
Anand, Robin, Alexey
Anand [50], Robin [75], Danijel [75]
Anand, Robin, Danijel
Alexey
Amit
Amit [10], Alexey [10], Mathias [10]

WBS	Name	Start	Finish	Work	Duration	Slack	Cost	Assigned to
1	Verify Serialfilter.vhd	mar 30	apr 4	4d	4d	29d	0	Alexey
2	Avarerage can satuaret ?	mar 30	mar 30	1h	1h	41d 3h	0	Robin
3	Interface VB.net	mar 30	apr 1	3d	3d	39d	0	Amit
4	interface vhdl	mar 30	apr 4	5d	4d	29d	0	Amit, Anand
5	clean up the data types	apr 5	apr 5	1d	1d	37d	0	Shwan
6	databuffer	mar 30	mar 30	2h	2h	41d 2h	0	Alexey
7	Verify EQ main	apr 5	apr 13	14d	7d	29d	0	Alexey, Mathias
8	Testbench the rx tc vhdl parts	apr 14	apr 26	4d	8d 3h	22d	0	Anand
9	Verify Driver Stage	mar 30	apr 5	7d	4d 2h	30d 1h	0	Danijel, Robin
10	Calculate Transistor Dimensioning	apr 11	apr 12	2d	2d	32d	0	Danijel, Robin
11	Creat Full custom Layout (Analog)	maj 4	maj 13	7d 2h	7d 2h	9d	0	Danijel, Robin
12	Creat Mixed Signal Verification models	maj 2	maj 4	4d	2d	9d 3h	0	Danijel, Robin
13	Complete the FPGA code	apr 4	apr 15	14d	10d	27d	0	Anand, Shwan
14	Milstone: Verify the FPGA code	maj 6	maj 6	N/A	N/A	15d	0	Anand
15	verification of the system	maj 2	maj 3	2d	2d	17d	0	
16	Milstone: Submit Formal verification of the system	maj 10	maj 10	N/A	N/A	13d	0	Alexey, Mathias
17	Milstone: Submit the Final VAMS results	maj 16	maj 15	N/A	N/A	9d	0	Danijel, Robin
18	Write The Final Report	maj 3	maj 17	15d	10d 2h	6d 1h	0	Alexey, Amit, Anand, Danijel, Mathias, Robin, Shwan
19	Write The Final Report - project	maj 16	maj 17	2d	2d	7d	0	Amit, Shwan
20	Tolgate : Submit Final Report	maj 18	maj 18	N/A	N/A	7d	0	Amit
21	Milstone: Final Presentation	maj 24	maj 24	N/A	N/A	3d	0	Anand, Robin
22	Final Presentation	maj 17	maj 18	2d	2h 40min	6d 2h	0	Alexey, Anand, Robin
23	Milstone: Exctract Pre Final Layout	maj 27	maj 27	N/A	N/A		0	Anand, Danijel, Robin
24	Milstone: Exctract Final Layout	maj 27	maj 27	N/A	N/A		0	Anand, Danijel, Robin
25	Debug the GainAmplifier	maj 2	maj 2	1d	1d	18d	0	Alexey
26	Debug the RX TX vhdl part	maj 2	maj 2	1d	1d	18d	0	Amit
27	Try out the RotatingBuffer again	maj 4	maj 12	2d	6d 2h	10d 1h	0	Alexey, Amit, Mathias

% Complete
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Name	Short name	Type	Group	Email	Cost
Shwan Ciyako	Shwan	Work			0
Mathias Lundell	Mathias	Work			0
Alexey	Alexey	Work			0
Danijel R	Danijel	Work			0
Robin Andersson	Robin	Work			0
Amit Kulkani	Amit	Work			0
Anandhavel S	Anand	Work			0