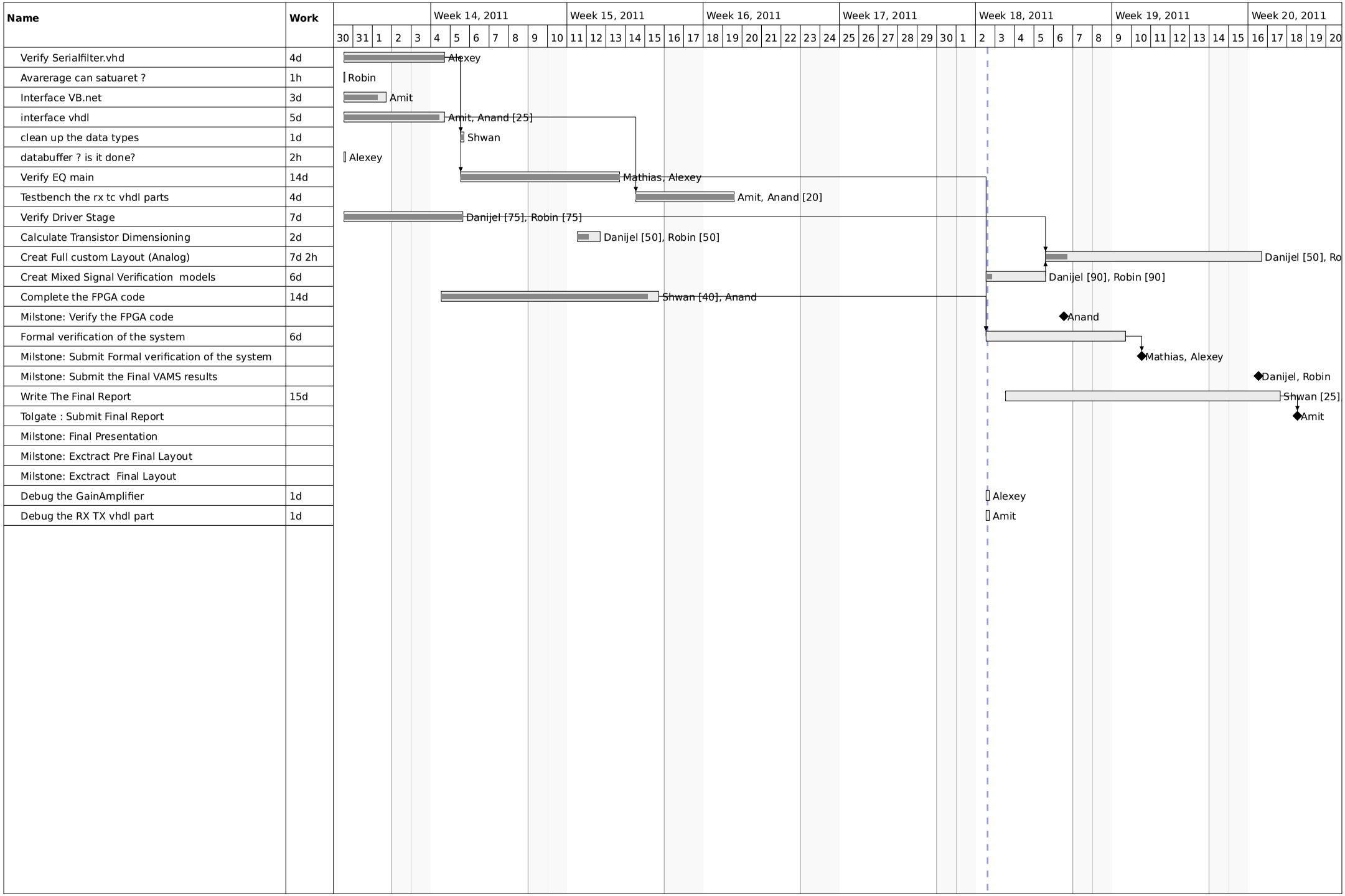
Name
Work
Week 14, 2011
Week 15, 2011
Week 16, 2011
Week 17, 2011
Week 18, 2011
Week 19, 2011
Week 20, 2011
30 31 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
Verify Serialfilter.vhd 4d
Alexey
Avarerage can satuaret ? 1h
Robin
Interface VB.net 3d
Amit
interface vhdl 5d
Amit, Anand [25]
clean up the data types 1d
Shwan
databuffer ? is it done? 2h
Alexey
Verify EQ main 14d
Mathias, Alexey
Testbench the rx tc vhdl parts 4d
Amit, Anand [20]
Verify Driver Stage 7d
Danijel [75], Robin [75]
Calculate Transistor Dimensioning 2d
Danijel [50], Robin [50]
Creat Full custom Layout (Analog) 7d 2h
Danijel [50], Ro
Creat Mixed Signal Verification models 6d
Danijel [90], Robin [90]
Complete the FPGA code 14d
Shwan [40], Anand
Milstone: Verify the FPGA code
Anand
Formal verification of the system 6d
Milstone: Submit Formal verification of the system
Mathias, Alexey
Milstone: Submit the Final VAMS results
Danijel, Robin
Write The Final Report 15d
Shwan [25]
Tolgate : Submit Final Report
Amit
Milstone: Final Presentation
Milstone: Exctract Pre Final Layout
Milstone: Exctract Final Layout
Debug the GainAmplifier 1d
Alexey
Debug the RX TX vhdl part 1d
Amit


Week 21, 2011
Week 22, 2011
Week 23, 2011
Week 24, 2011
Week 25, 2011
Week 26, 2011
Week 27, 2011
Week 28, 2011
Week 29, 2011
Week 30, 2...
21 22 23 24 25 26 27 28 29 30 31 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 ..
Robin, Anand
Danijel [75], Robin [75], Anand [50]
Danijel, Robin, Anand

WBS	Name	Start	Finish	Work	Duration	Slack	Cost	Assigned to	% Complete
1	Verify Serialfilter.vhd	Mar 30	Apr 4	4d	4d	25d	0	Alexey	100
2	Avarerage can satuaret ?	Mar 30	Mar 30	1h	1h	41d 3h	0	Robin	0
3	Interface VB.net	Mar 30	Apr 1	3d	3d	39d	0	Amit	80
4	interface vhdl	Mar 30	Apr 4	5d	4d	34d	0	Amit, Anand	95
5	clean up the data types	Apr 5	Apr 5	1d	1d	37d	0	Shwan	100
6	databuffer ? is it done?	Mar 30	Mar 30	2h	2h	41d 2h	0	Alexey	0
7	Verify EQ main	Apr 5	Apr 13	14d	7d	25d	0	Alexey, Mathias	100
8	Testbench the rx tc vhdl parts	Apr 14	Apr 19	4d	3d 1h	27d 2h	0	Amit, Anand	100
9	Verify Driver Stage	Mar 30	Apr 5	7d	4d 2h	28d 1h	0	Danijel, Robin	100
10	Calculate Transistor Dimensioning	Apr 11	Apr 12	2d	2d	32d	0	Danijel, Robin	50
11	Creat Full custom Layout (Analog)	May 5	May 16	7d 2h	7d 2h	8d	0	Danijel, Robin	10
12	Creat Mixed Signal Verification models	May 2	May 5	6d	3d 1h	6d 2h	0	Danijel, Robin	10
13	Complete the FPGA code	Apr 4	Apr 15	14d	10d	23d	0	Anand, Shwan	95
14	Milstone: Verify the FPGA code	May 6	May 6	N/A	N/A	15d	0	Anand	0
15	Formal verification of the system	May 2	May 9	6d	6d	13d	0		0
16	Milstone: Submit Formal verification of the system	May 10	May 10	N/A	N/A	13d	0	Alexey, Mathias	0
17	Milstone: Submit the Final VAMS results	May 16	May 15	N/A	N/A	9d	0	Danijel, Robin	0
18	Write The Final Report	May 3	May 17	15d	10d 2h	7d 1h	0	Alexey, Amit, Anand, Danijel, Mathias, Robin, Shwan	0
19	Tolgate : Submit Final Report	May 18	May 18	N/A	N/A	7d	0	Amit	0
20	Milstone: Final Presentation	May 24	May 24	N/A	N/A	3d	0	Anand, Robin	0
21	Milstone: Exctract Pre Final Layout	May 27	May 27	N/A	N/A		0	Anand, Danijel, Robin	0
22	Milstone: Exctract Final Layout	May 27	May 27	N/A	N/A		0	Anand, Danijel, Robin	0
23	Debug the GainAmplifier	May 2	May 2	1d	1d	18d	0	Alexey	0
24	Debug the RX TX vhdl part	May 2	May 2	1d	1d	18d	0	Amit	0

Name	Short name	Type	Group	Email	Cost
Anandhavel S	Anand	Work			0
Amit Kulkani	Amit	Work			0
Robin Andersson	Robin	Work			0
Danijel R	Danijel	Work			0
Alexey	Alexey	Work			0
Mathias Lundell	Mathias	Work			0
Shwan Ciyako	Shwan	Work			0