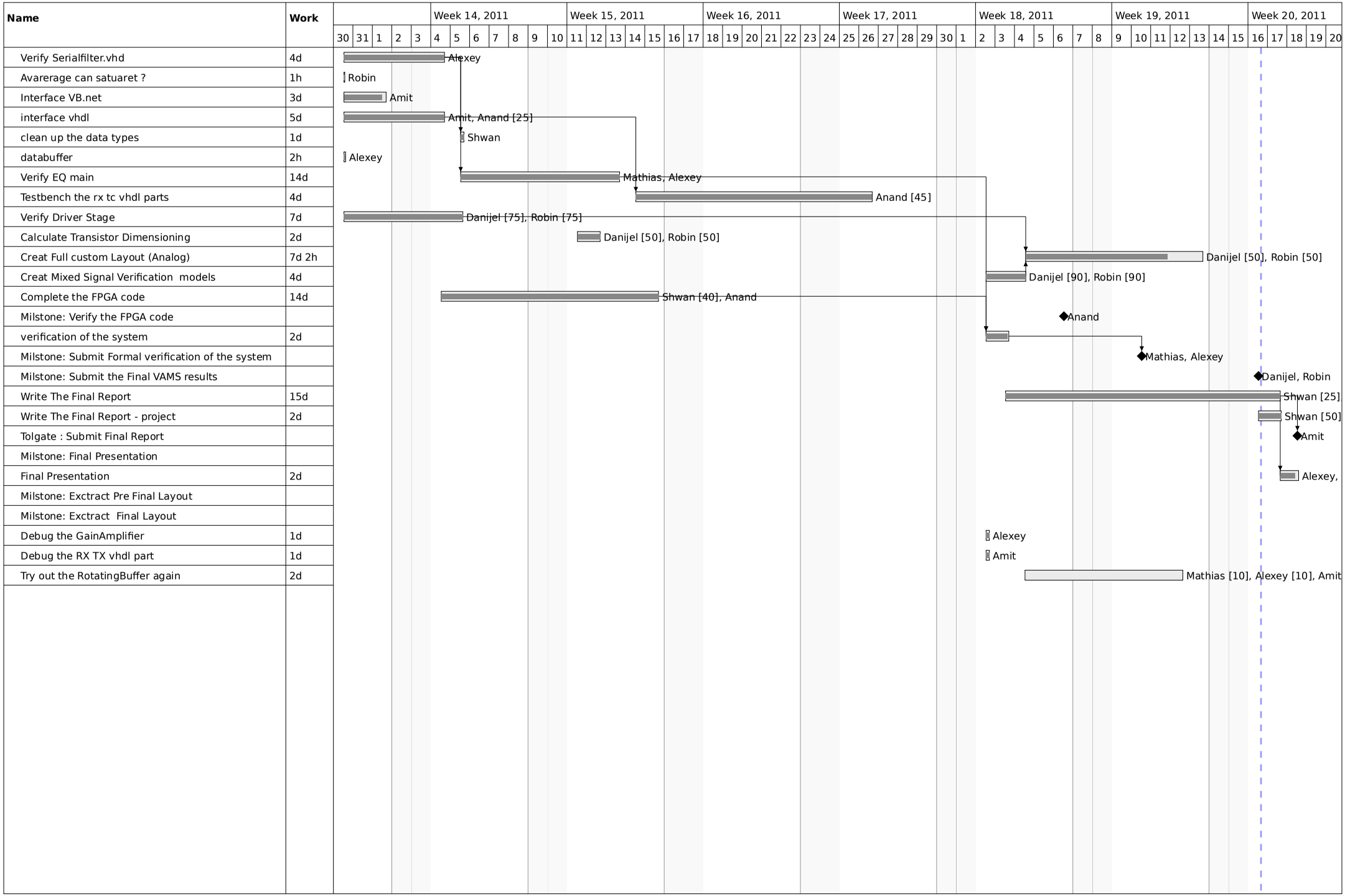
Name
Work
Week 14, 2011
Week 15, 2011
Week 16, 2011
Week 17, 2011
Week 18, 2011
Week 19, 2011
Week 20, 2011
30 31 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
Verify Serialfilter.vhd 4d
Alexey
Avarerage can satuaret ? 1h
Robin
Interface VB.net 3d
Amit
interface vhdl 5d
Amit, Anand [25]
clean up the data types 1d
Shwan
databuffer 2h
Alexey
Verify EQ main 14d
Mathias, Alexey
Testbench the rx tc vhdl parts 4d
Anand [45]
Verify Driver Stage 7d
Danijel [75], Robin [75]
Calculate Transistor Dimensioning 2d
Danijel [50], Robin [50]
Creat Full custom Layout (Analog) 7d 2h
Danijel [50], Robin [50]
Creat Mixed Signal Verification models 4d
Danijel [90], Robin [90]
Complete the FPGA code 14d
Shwan [40], Anand
Milstone: Verify the FPGA code
Anand
verification of the system 2d
Milstone: Submit Formal verification of the system
Mathias, Alexey
Milstone: Submit the Final VAMS results
Danijel, Robin
Write The Final Report 15d
Shwan [25]
Write The Final Report - project 2d
Shwan [50]
Tolgate : Submit Final Report
Amit
Milstone: Final Presentation
Final Presentation 2d
Alexey,
Milstone: Exctract Pre Final Layout
Milstone: Exctract Final Layout
Debug the GainAmplifier 1d
Alexey
Debug the RX TX vhdl part 1d
Amit
Try out the RotatingBuffer again 2d
Mathias [10], Alexey [10], Amit


Week 21, 2011
Week 22, 2011
Week 23, 2011
Week 24, 2011
Week 25, 2011
Week 26, 2011
Week 27, 2011
Week 28, 2011
Week 29, 2011
Week 30, 2...
21 22 23 24 25 26 27 28 29 30 31 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 ..
Robin, Anand
Danijel [75], Robin [75], Anand [50]
Danijel, Robin, Anand

WBS	Name	Start	Finish	Work	Duration	Slack	Cost	Assigned to	% Complete
1	Verify Serialfilter.vhd	Mar 30	Apr 4	4d	4d	29d	0	Alexey	100
2	Avarerage can satuaret ?	Mar 30	Mar 30	1h	1h	41d 3h	0	Robin	100
3	Interface VB.net	Mar 30	Apr 1	3d	3d	39d	0	Amit	90
4	interface vhdl	Mar 30	Apr 4	5d	4d	29d	0	Amit, Anand	100
5	clean up the data types	Apr 5	Apr 5	1d	1d	37d	0	Shwan	100
6	databuffer	Mar 30	Mar 30	2h	2h	41d 2h	0	Alexey	100
7	Verify EQ main	Apr 5	Apr 13	14d	7d	29d	0	Alexey, Mathias	100
8	Testbench the rx tc vhdl parts	Apr 14	Apr 26	4d	8d 3h	22d	0	Anand	100
9	Verify Driver Stage	Mar 30	Apr 5	7d	4d 2h	30d 1h	0	Danijel, Robin	100
10	Calculate Transistor Dimensioning	Apr 11	Apr 12	2d	2d	32d	0	Danijel, Robin	100
11	Creat Full custom Layout (Analog)	May 4	May 13	7d 2h	7d 2h	9d	0	Danijel, Robin	80
12	Creat Mixed Signal Verification models	May 2	May 4	4d	2d	9d 3h	0	Danijel, Robin	100
13	Complete the FPGA code	Apr 4	Apr 15	14d	10d	27d	0	Anand, Shwan	100
14	Milstone: Verify the FPGA code	May 6	May 6	N/A	N/A	15d	0	Anand	0
15	verification of the system	May 2	May 3	2d	2d	17d	0		95
16	Milstone: Submit Formal verification of the system	May 10	May 10	N/A	N/A	13d	0	Alexey, Mathias	0
17	Milstone: Submit the Final VAMS results	May 16	May 15	N/A	N/A	9d	0	Danijel, Robin	0
18	Write The Final Report	May 3	May 17	15d	10d 2h	6d 1h	0	Alexey, Amit, Anand, Danijel, Mathias, Robin, Shwan	100
19	Write The Final Report - project	May 16	May 17	2d	2d	7d	0	Amit, Shwan	100
20	Tolgate : Submit Final Report	May 18	May 18	N/A	N/A	7d	0	Amit	0
21	Milstone: Final Presentation	May 24	May 24	N/A	N/A	3d	0	Anand, Robin	0
22	Final Presentation	May 17	May 18	2d	2h 40min	6d 2h	0	Alexey, Anand, Robin	80
23	Milstone: Exctract Pre Final Layout	May 27	May 27	N/A	N/A		0	Anand, Danijel, Robin	0
24	Milstone: Exctract Final Layout	May 27	May 27	N/A	N/A		0	Anand, Danijel, Robin	0
25	Debug the GainAmplifier	May 2	May 2	1d	1d	18d	0	Alexey	100
26	Debug the RX TX vhdl part	May 2	May 2	1d	1d	18d	0	Amit	100
27	Try out the RotatingBuffer again	May 4	May 12	2d	6d 2h	10d 1h	0	Alexey, Amit, Mathias	0

Name	Short name	Type	Group	Email	Cost
Anandhavel S	Anand	Work			0
Amit Kulkani	Amit	Work			0
Robin Andersson	Robin	Work			0
Danijel R	Danijel	Work			0
Alexey	Alexey	Work			0
Mathias Lundell	Mathias	Work			0
Shwan Ciyako	Shwan	Work			0