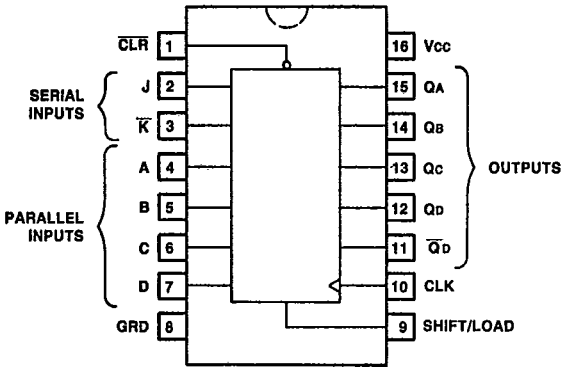
4-Bit Parallel/Serial-In/Parallel-Out Shift Register

The LS195 is a bipolar, NPN, sealed-junction, silicon integrated circuit. It is manufactured in low-power Schottky technology and is available in a wire-bonded, 16-pin plastic DIP or surface mount package. This device is a universal shift register allowing serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.



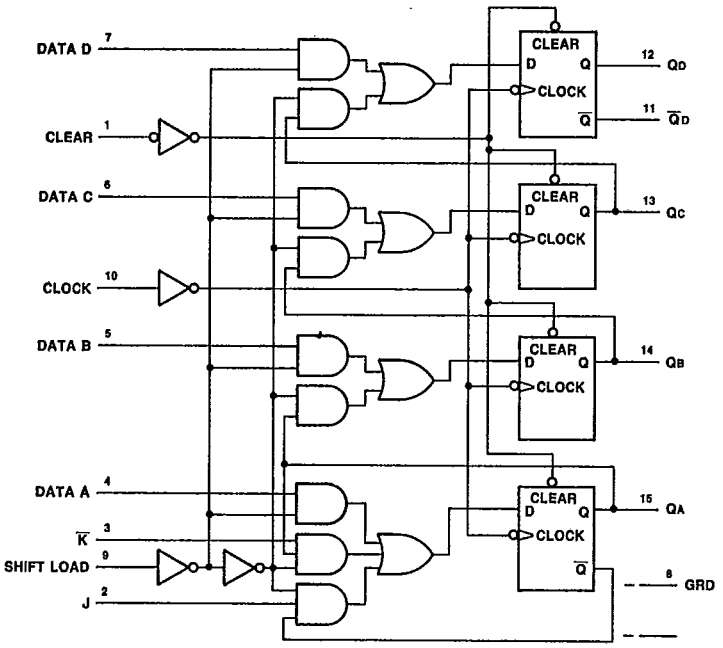
Truth Table

Inputs									Outputs				
			Serial		Parallel								
Clear	Shift/ Load	Clock	J	$\overline{K}$	A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = High level (steady state)
L = Low level (steady state)
X = Irrelevant (any input, including transitions)
↑ = Transition from low to high level
a, b, c, d = The level of steady-state at inputs A, B, C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn} = The level of Q_A, Q_B, or Q_C, respectively, before the most recent transition of the clock

WA-LS195, WP90350 List 4

Logic Diagram



Electrical Characteristics

V_{CC} = 5.0 ±0.5 V, T_A = −55 to +125°C (WA-LS)
V_{CC} = 5.0 ±0.25 V, T_A = 0 to 70°C (WP)

		WA-LS		WP		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**
Output Voltage, V_{CC} = 4.5 V (WA-LS), V_{CC} = 4.75 V (WP)						
Low, I_{OL} = 4.0 mA	V_{OL}	–	0.4	–	0.4	V
I_{OL} = 8.0 mA	V_{OL}	–	0.5	–	0.5	V
High, I_{OH} = −0.4 mA	V_{OH}	2.5	–	2.7	–	V
Input Voltage, V_{CC} = 4.5 V (WA-LS), V_{CC} = 4.75 V (WP)						
Low	V_{IL}	–	0.7	–	0.8	V
High	V_{IH}	2.0	7.5	2.0	5.5	V
Clamp, I_{IN} = −18.0 mA	V_{IK}	–	−1.5	–	−1.5	V
Input Current, V_{CC} = 5.5 V (WA-LS), V_{CC} = 5.25 V (WP)						
Low, V_{IL} = 0.4 V	I_{IL}	–	−0.4	–	−0.4	mA
High, V_{IH} = 2.7 V	I_{IH}	–	20.0	–	20.0	μA
@ V_I max, V_I = 7.0 V (WA-LS), V_I = 5.5 V (WP)	I_I	–	0.1	–	0.1	mA
Output Current, V_{CC} = 5.5 V (WA-LS), V_{CC} = 5.25 V (WP)						
Short-Circuit	I_{OS}	−20.0	−100.0	−20.0	−100.0	mA
Supply Current, V_{CC} = 5.5 V (WA-LS), V_{CC} = 5.25 V (WP)	I_{CC}	–	21.0	–	21.0	mA

Timing Characteristics

V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

Parameter	Symbol	WA-LS Min	WA-LS Max	WP Min	WP Max	Units
Propagation Delay						
Clear-to-Output						
High-to-Low	t_{PHL}	–	30.0	–	30.0	ns
Clock-to-Output						
Low-to-High	t_{PLH}	–	22.0	–	22.0	ns
High-to-Low	t_{PHL}	–	26.0	–	26.0	ns
Operating Conditions						
Width of Clock Pulse	t_W	16.0	–	16.0	–	ns
Width of Clear Pulse	t_W	12.0	–	12.0	–	ns
Setup Time						
Shift/Load, Low	t_{DSL}	25.0	–	25.0	–	ns
High	t_{DSH}	25.0	–	25.0	–	ns
Data-to-Clock, Low	t_{DSL}	15.0	–	15.0	–	ns
High	t_{DSH}	15.0	–	15.0	–	ns
Clear Inactive State, Low	t_{DSL}	25.0	–	25.0	–	ns
High	t_{DSH}	25.0	–	25.0	–	ns
Hold Time						
Data-to-Clock, Low	t_{DHL}	0	–	0	–	ns
High	t_{DHH}	0	–	0	–	ns
Shift/Load, Low	t_{DHL}	0	–	0	–	ns
High	t_{DHH}	0	–	0	–	ns
Release Time						
Shift/Load	t_{rel}	–	10.0	–	10.0	ns
Maximum Clock Frequency	f_{max}	30.0	–	30.0	–	MHz

Maximum Ratings*

Power supply voltage (V_{CC}) ..... 7.0 V
Operating temperature (T_A) ..... −55 to +125°C (WA-LS), 0 to 70°C (WP)
Storage temperature (T_{stg})** ..... −65 to +150°C

* Maximum ratings are defined as the limiting conditions that the user can apply to the device under all variations of circuit and environmental conditions. If any rating is exceeded, permanent damage to the device may result.

** Bonding or soldering of the external leads of this device can be performed safely at temperatures up to 300°C.

Timing Diagrams

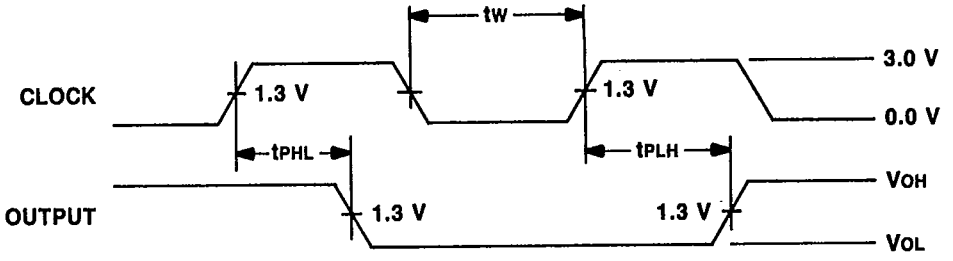


Figure 1. Clock and Output Waveforms

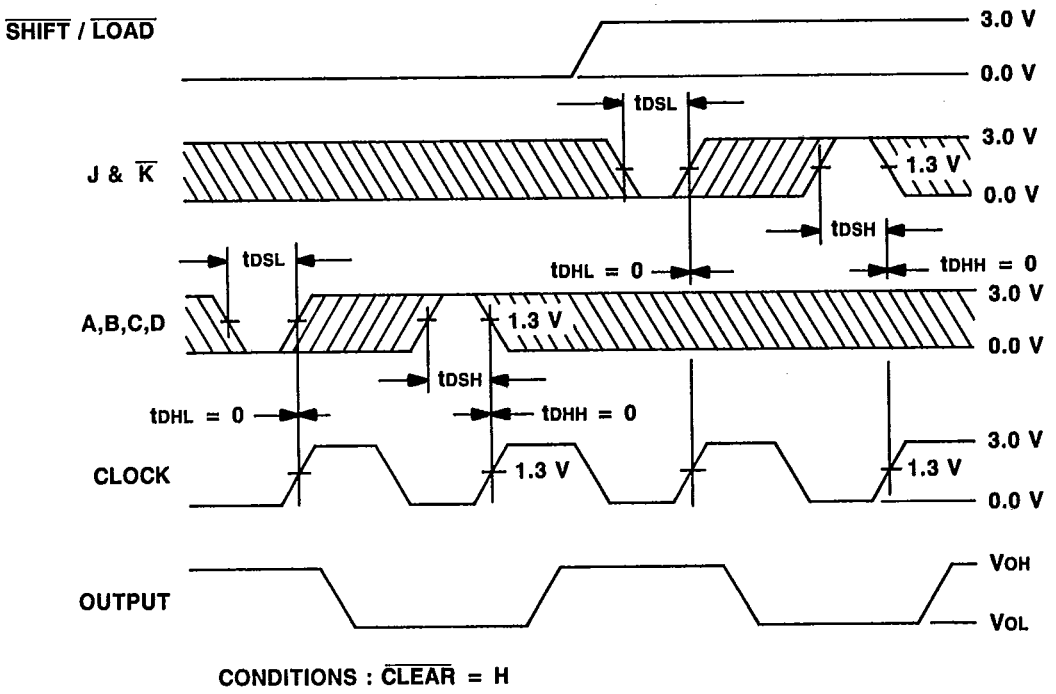


Figure 2. Shift/Load, Set-Up, Hold Time, Parallel Data, and Serial Data Waveforms

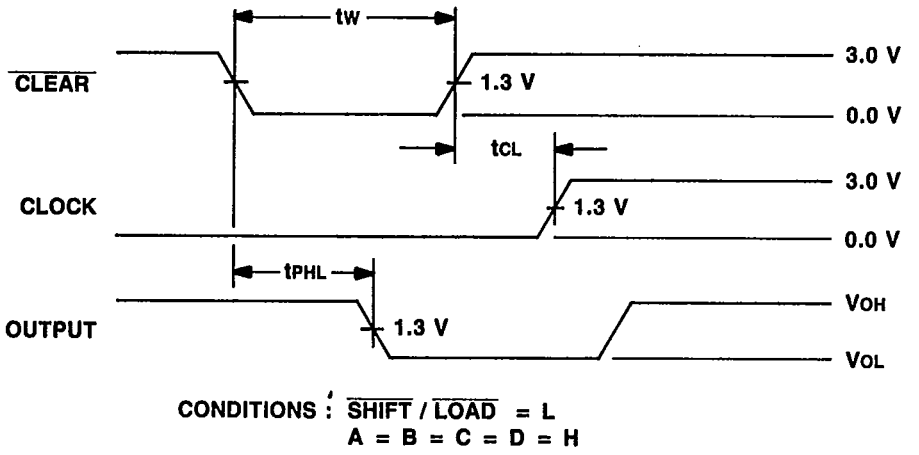


Figure 3. Clear, Clock, and Output Waveforms

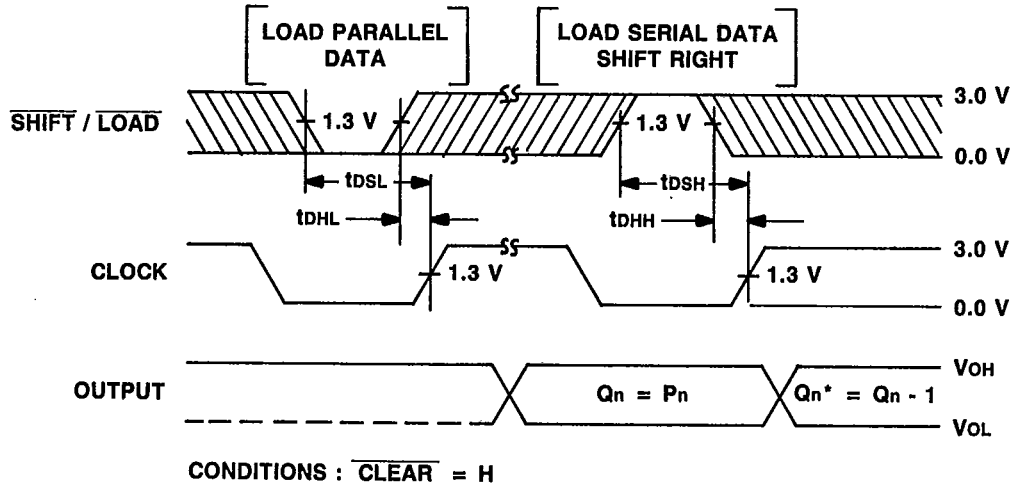
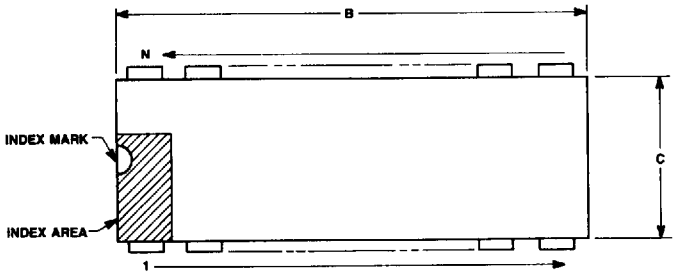
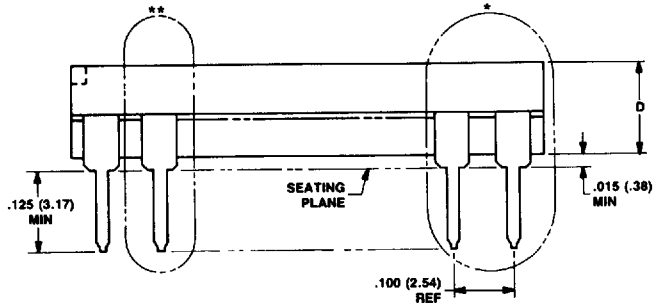
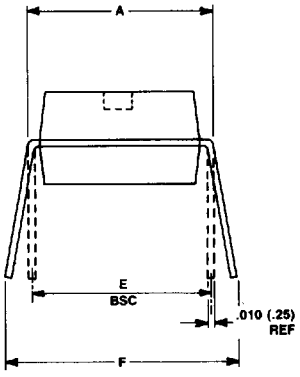


Figure 4. Shift/Load, Clock, and Output Waveforms



* See End-Lead Configuration for Lead Dimensions (Refer to Detail $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$)
** See Center-Lead Configuration for Lead Dimensions (Refer to Detail $\overline{E}$, $\overline{F}$, $\overline{G}$)





Postmolded Plastic DIP Dimensions†

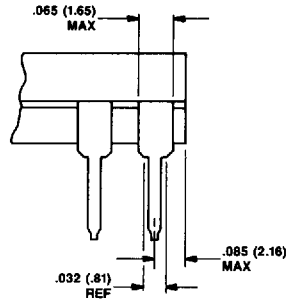
No. Leads	A Max	B Max	C Max	D Max	E BSC	F Max	Notes	Lead Configuration
14	.320 (8.13)	.795 (20.19)	.255 (6.48)	.140 (3.56)	.300 (7.62)	.400 (10.16)	1,2,3,4	$\overline{A}$ $\overline{B}$ $\overline{E}$ $\overline{G}$
16	.320 (8.13)	.795 (20.19)	.265 (6.73)	.140 (3.56)	.300 (7.62)	.400 (10.16)	1,2,3,4	$\overline{B}$ $\overline{C}$ $\overline{D}$ $\overline{E}$ $\overline{F}$ $\overline{G}$
20	.320 (8.13)	1.040 (26.42)	.255 (6.48)	.140 (3.56)	.300 (7.62)	.400 (10.16)	1,2,3,4	$\overline{A}$ $\overline{B}$ $\overline{D}$ $\overline{E}$ $\overline{F}$ $\overline{G}$

† Dimensions are in inches and (millimeters).

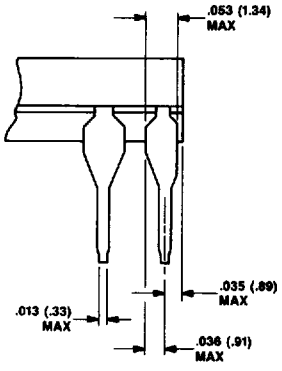
Notes:
1. Meets JEDEC standards.
2. Index mark may be semicircular notch located in index area.
3. Index mark may be circular dimple located in index area.
4. Actual dimensions may vary depending on location of assembly, but all meet limits shown in table.

Postmolded Plastic DIP Lead Configurations

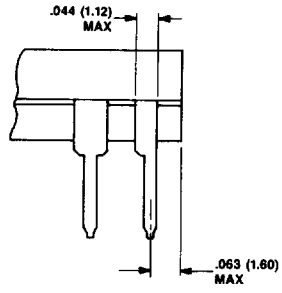
End Leads



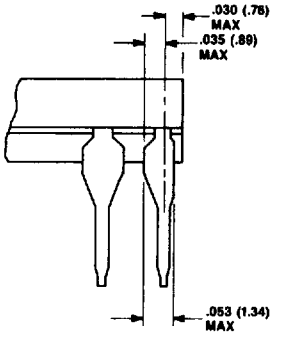
Detail $\bar{A}$: Full-Lead/Square Shoulder



Detail $\bar{B}$: Full-Lead/Tapered Offset

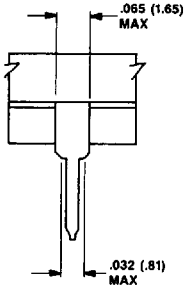


Detail $\bar{C}$: Half-Lead/Square Shoulder

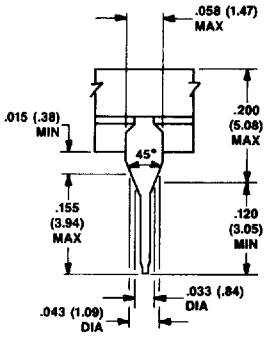


Detail $\bar{D}$: Half-Lead/Tapered

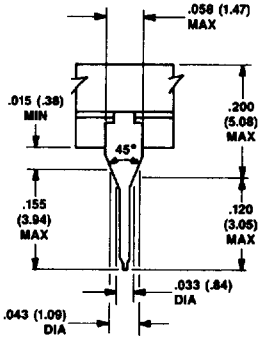
Center Leads



Detail $\bar{E}$: Square Shoulder



Detail $\bar{F}$: Taper



Detail $\bar{G}$: Taper

Notes: Lead configurations vary depending on location of assembly.
Dimensions are in inches and (millimeters).