Report for Lab 3 of CIS 610: Digital System Design

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1 Introduction

In this project the goal was to construct a pipelined RISCV processor with two hardware threads. Unfortunately, only a single cycle processor was developed and has not been fully tested.

This processor is designed to work with most of the base level 32-bit integer ISA described in [1] [2]. This set includes general integer instructions such as arithmetic, comparison, bit-wise boolean, memory access, branch, and others (see Fig. 2). Due to time constraints, jump, fence, scall, and other system instructions were left out.

2 Design

The processor was broken down into smaller modules to ease the development. These modules include memory, register file, control blocks and an execution unit. Fig. 1 shows the block diagram.

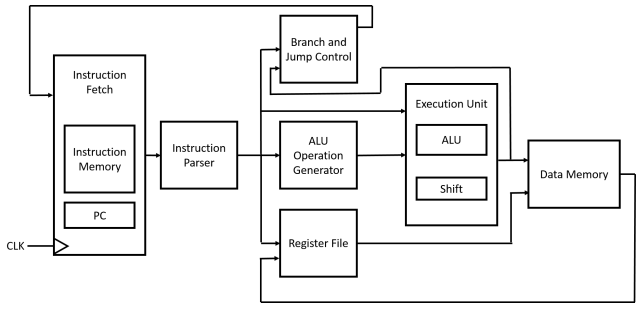

Figure 1: Block Diagram

3 Challenges and Lessons learned

Unfortunately, the progress was significantly less than originally intended. This shortfall occurred due to a lack of time management and underestimation of the project by the designer. In the future better decisions will be made based on the experience of coming up short in this project.

Additionally, this projected helped the designer develop a broader understanding of RISC processors, particularly the differences between the MIPS ISA and the RISCV ISA. Notably MIPS is heavily tailored to a five stage pipeline including design features such as branch delay slots while the developers of the RISCV ISA intended the ISA to be more versatile and left out such optimizations. These features gave the designer more leeway in constructing the system. Although lack of knowledge prevented him from taking advantage, the additional options and possibilities help provide a better understanding of the 5-stage pipeline and the possibilities outside this box.

References

[1] Andrew Waterman, *Design of the RISC-V Instruction Set Architecture*, Ph.D. thesis, University of California, Berkeley, 2016.

[2] Andrew Waterman, Yunsup Lee, , David A Patterson, and Krste Asanović, "The risc-v instruction set manual volume i: Privileged architecture version 2.1," *EECS Department, University of California, Berkeley, Tech. Rep. UCB/EECS-2016-118*, 2016.

RV32I Base Instruction Set

imm[31:12]					rd	0110111	LUI rd,imm
imm[31:12]					rd	0010111	AUIPC rd,imm
imm[20|10:1|11|19:12]					rd	1101111	JAL rd,imm
imm[11:0]			rs1	000	rd	1100111	JALR rd,rs1,imm
imm[12|10:5]	rs2		rs1	000	imm[4:1|11]	1100011	BEQ rs1,rs2,imm
imm[12|10:5]	rs2		rs1	001	imm[4:1|11]	1100011	BNE rs1,rs2,imm
imm[12|10:5]	rs2		rs1	100	imm[4:1|11]	1100011	BLT rs1,rs2,imm
imm[12|10:5]	rs2		rs1	101	imm[4:1|11]	1100011	BGE rs1,rs2,imm
imm[12|10:5]	rs2		rs1	110	imm[4:1|11]	1100011	BLTU rs1,rs2,imm
imm[12|10:5]	rs2		rs1	111	imm[4:1|11]	1100011	BGEU rs1,rs2,imm
imm[11:0]			rs1	000	rd	0000011	LB rd,rs1,imm
imm[11:0]			rs1	001	rd	0000011	LH rd,rs1,imm
imm[11:0]			rs1	010	rd	0000011	LW rd,rs1,imm
imm[11:0]			rs1	100	rd	0000011	LBU rd,rs1,imm
imm[11:0]			rs1	101	rd	0000011	LHU rd,rs1,imm
imm[11:5]	rs2		rs1	000	imm[4:0]	0100011	SB rs1,rs2,imm
imm[11:5]	rs2		rs1	001	imm[4:0]	0100011	SH rs1,rs2,imm
imm[11:5]	rs2		rs1	010	imm[4:0]	0100011	SW rs1,rs2,imm
imm[11:0]			rs1	000	rd	0010011	ADDI rd,rs1,imm
imm[11:0]			rs1	010	rd	0010011	SLTI rd,rs1,imm
imm[11:0]			rs1	011	rd	0010011	SLTIU rd,rs1,imm
imm[11:0]			rs1	100	rd	0010011	XORI rd,rs1,imm
imm[11:0]			rs1	110	rd	0010011	ORI rd,rs1,imm
imm[11:0]			rs1	111	rd	0010011	ANDI rd,rs1,imm
0000000	shamt		rs1	001	rd	0010011	SLLI rd,rs1,shamt
0000000	shamt		rs1	101	rd	0010011	SRLI rd,rs1,shamt
0100000	shamt		rs1	101	rd	0010011	SRAI rd,rs1,shamt
0000000	rs2		rs1	000	rd	0110011	ADD rd,rs1,rs2
0100000	rs2		rs1	000	rd	0110011	SUB rd,rs1,rs2
0000000	rs2		rs1	001	rd	0110011	SLL rd,rs1,rs2
0000000	rs2		rs1	010	rd	0110011	SLT rd,rs1,rs2
0000000	rs2		rs1	011	rd	0110011	SLTU rd,rs1,rs2
0000000	rs2		rs1	100	rd	0110011	XOR rd,rs1,rs2
0000000	rs2		rs1	101	rd	0110011	SRL rd,rs1,rs2
0100000	rs2		rs1	101	rd	0110011	SRA rd,rs1,rs2
0000000	rs2		rs1	110	rd	0110011	OR rd,rs1,rs2
0000000	rs2		rs1	111	rd	0110011	AND rd,rs1,rs2
0000	pred	succ	00000	000	00000	0001111	FENCE
0000	0000	0000	00000	001	00000	0001111	FENCE.I
000000000000			00000	000	00000	1110011	SCALL
000000000001			00000	000	00000	1110011	SBREAK
110000000000			00000	010	rd	1110011	RDCYCLE rd
110010000000			00000	010	rd	1110011	RDCYCLEH rd
110000000001			00000	010	rd	1110011	RDTIME rd
110010000001			00000	010	rd	1110011	RDTIMEH rd
110000000010			00000	010	rd	1110011	RDINSTRET rd
110010000010			00000	010	rd	1110011	RDINSTRETH rd

Figure 2: List of RISCV Instructions. Reproduced from [1]