



Green University of Bangladesh

*Department of Computer Science and Engineering (CSE)
Semester: (Fall, Year: 2024), B.Sc. in CSE (Day)*

KSA 01 After Mid for Final

*Course Title: Microprocessor and Microcontroller
Course Code: CSE-303
Section: 222-D09*

Students Details

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[For teachers use only: **Don't write anything inside this box**]

<u>Lab Project Status</u>	
Marks:	Signature:
Comments:	Date:

Microprocess & Microcontroller

Subject

Sat	Sun	Mon	Tue	Wed	Thu	Fri
0	0	0	0	0	0	0

Date: 15/11/2024

$V_{cc} = 1$ (Minimum Mode)

Minimum Mode = single processor active

Maximum Mode = multiple

For 20 bit bus = $2 \times 8^2 = 16$
 $3 \times 8 = 24$ V_c (Maximum)

Transistor = $8 \times 2 = 16$

1 (Transmit)

0 (Receive)

control Bus এর সাথে

কাজ হয়।

In = 8085

I/O / M
1 0

In 8086,

M / I/O
1 0

vice versa of 8085

Maximum Mode.

RR' / GT0 (priority high)

RR' / GT1 (priority low)

↓
Grant

Ready
asserted

LOCK = Internal and external
peripheral can't
modify the data

* Minimum vs Maximum (Question)
Mode.

Subject Microprocessor and Microcontroller

Sat Sun Mon Tue Wed Thu Fri
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Date: / /

Pipeline Architecture

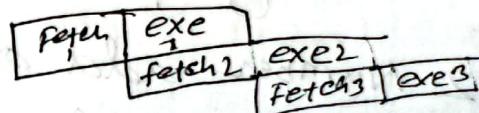
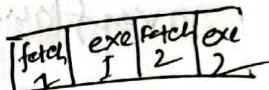
8086 contains two independent functional units

- 1) Bus Interface Unit (BIU)
- 2) Execution Unit (EU)
 - Transfer data and address between processor memory & I/O devices
 - Receive opcode of an instruction

opcode = What to do (mov, add, sub)

The BIU and EU operates independently

Non-pipeline



Advantages:

- ④ Read the next instruction
- ④ Eliminates waiting time
- ④ Enhance the performance

pipelining possible
due to Queue

Disadvantage:

④ Complex and costly to manufacture

The Instruction Queue:

④ Decode or execute an instruction

④ Decode doesn't require busses

④ When EU busy, the BIU fetches upto six instruction bytes

④ pre-fetched bytes FIFO register set.

Flag Register (16 bits)

Date: 16 / 11 / 2024

6 = status flag (5) are like 8085

3 = control flag

parity flag = lower 8 bit 1(odd) = 1
even(1) = 1

carry flag = 17th bit

auxiliary carry = 4 bit (1 nibble) এবং

zero flag = 16 bit all are zero

Control Flag

overflag flow = 8 bit signed number

2 Number add or sub for MSB then overflow.
 $0+0=1$ (overflow)

Side Math Work

Addition: SF = 1

PF = 10

OF = 1

Subtraction:

$$\begin{array}{r}
 0110 \quad 0101 + 1101 \quad 0001 \\
 0010 \quad 0011 - 0101 \quad 1001 \\
 \hline
 0100 \quad 0010 - 0111 \quad 1000
 \end{array}$$

SF = 0

ZF = 0

PF = 1 (8 bit)

CF = 0

AF = 1 (4 bit)

OF = 0

* Binary subtraction 6 flag identification.

Control Flag:

- 1) Interrupt Flag (IF)
- 2) Direction Flag (DF) and
- 3) Trap Flag (TF)

lower to upper

MSB ← LSB (DF=0) Increment

MSB → LSB (Decrement)
(DF=1)

Trap flag: Total program in a single step (0)
single step (1) } TF = 0 (Run single time)
TF(1) = step by step

Question Hint: If we are asked to verify that if there is an error for the full program $\boxed{TF = 0}$ set

Subject Mi & Mi

Sat Sun Mon Tue Wed Thu Fri
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Interrupt

Date: / /

Hardware interrupt has 2 pins

NMI and MI

- IF(1) → Unmaskable (Enable)
IF(0) → Maskable (Disable)

critical Response Time = After a certain period time program will be wait

Software Interrupt

- Group of 256 interrupt
- 1) Type 0 to 4
 - 2) Type 5 to 31
 - 3) Type 32 to 255

Type 0 → Divide Error Interrupt

Type 1 → Single step

Type 2 → Non maskable

Type 3 → Break point interrupt

Type 7 → overflow interrupt

Subject Microprocessor
Interfacing

Sat Sun Mon Tue Wed Thu Fri
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Date: 23/11/2024

$$2^{20} = 1 \text{ MB} \quad \text{Data Line} = 16$$

D8 - D15

HB

512 KB

Odd Bank

1

3

5

.

:

9

$D_0 - D_7$: IA
 CB : HA

512 KB,
 Even Bank

0

2

4

.

:

10(A)

12(C)

ROM: 27XX, 27XXX

RAM: 61XX, 61XXX
62XX, 62XXX

XX → Memory size in K bits

IC: 2716
 ↳ ROM

16 K bits

16 × 8

= 128 KB

= $2^{11} \times 8$

Address Line = 11

Data Line = 8

IC = 6264

 \hookrightarrow RAM

ROM = 64 K bits

$$\pm 64/8$$

$$\Rightarrow 8 \text{ KB}$$

$$= 2^{13} \times 8 \rightarrow \begin{array}{l} \text{Data line} = 8 \\ \text{Address} = 13 \end{array}$$

Bank selection for odd and even bank

BHE

A0

Bank Selection

0

0

Both select

0

1

odd.

1

0

even

A1

No. T

Ex-1: Interface microprocessor 8086 with two micro-chip IC - 27512 chip.

Given,

27512

 \hookrightarrow EP ROM

Memory size = 512 K bits

$$= 512/8 = 64 \text{ KB}$$

$$= 2^{16} \times 8 \rightarrow \begin{array}{l} \text{Address} = 16 \\ \text{Data} = 8 \end{array}$$

Subject _____

Sat	Sun	Mon	Tue	Wed	Thu	Fri
0	0	0	0	0	0	0

Date : / /

Even

A ₁₉	A ₁₈	A ₁₇	A ₁₆ --- A ₂	A ₁	B ₁₆ = 01
1	1	1	0 0 0	0 0 0	MA960
1	1	1	1 1 1	1	0
1	1	1	0 0 0	0 0 0	81A2
1	1	1	1 1 1	1	1
					1

EX-2:

16K * 8 b60 not m75162 800K

$$= 16K / 2 * 8$$

(8+8 for odd and even bank respectively)

= 8K * 8

data line

address line = 13

= $2^{13} * 8$

or, chip selector = 00000111

A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃A ₃	A ₂	A ₁	A ₀
1	1	0	0	0	0	0 0 ... 0 0 0 0	0	0	0
1	1	0	0	0	0	1 1 ... 1 1 1 1	1	1	0
1	1	0	0	0	0	0 0 ... 0 0 0 0	1	1	1

1	1	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	1
1	1	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	1
1	1	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	1
1	1	0 0 0	0 0 0	0 0 0	0 0 0	0 0 0	1

Subject _____

(mm) JUN 1990

Sat Sun Mon Tue Wed Thu Fri
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Date: _____

Last odd = C3FFEHT

Last even = C3FFFH

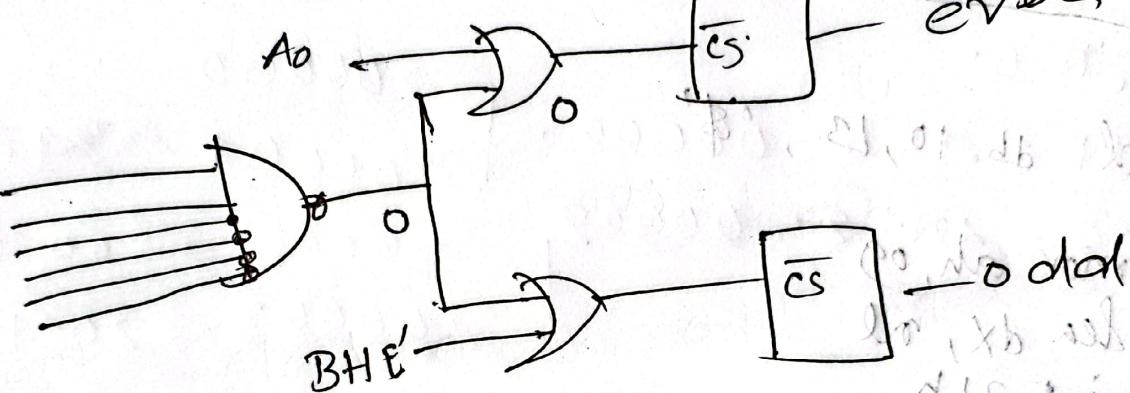
even

odd

Starting = C0000HT

= C0001HT

A18
A19



BHE'	A
0	0
0	1
1	0
1	1

2 both odd even
No.T

Microprocessor & Microcontroller

Sat Sun Mon Tue Wed Thu Fri
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Subject : Interrupt Vector Table (IVT)

Date : 24/11/2024

FSR contains : Physical address (multiple for multiple intr.)

Specific ISR physical addr. location \rightarrow found by S800 : IVT. Vec. Table

$$P.\text{ Addr} = CS \times IO + IP$$

$$(P.\text{ Addr})_{(5\text{ digit})} = (0000 \times 10) + 0001$$

$$= 00001$$

$$(2 \text{ bytes}) \quad H = 0000 = 0 \times A = 9E$$

$$CS \rightarrow \text{code segment} \quad (2 \text{ bytes})$$

$$IP \rightarrow \text{instruction pointer} \quad (2 \text{ bytes})$$

$$P.\text{ Address} \rightarrow 1 \text{ byte} \quad H = 0001 = 1 \times A = 9E$$

$$P.\text{ Addr} = 00001 = 00000001 = 25$$

$$\text{For } 256 \text{ intr.} \quad H = 00000001 = 1 \times A = 9E$$

$$\text{mem size} = (256 \times 4) \text{ bytes}$$

$$= 1 \text{ KB}$$

$$(P.\text{ Addr})_{(6\text{ digit})} = 000000$$

$$CS \leftarrow 0000 \quad IP \leftarrow 0000$$

$$H = 0000 = 0 \times A = 9E$$

$$\text{for type 0: } IP = 4 \times 0 = 0 \approx (0000)_2$$

$$CS = 4N + 2$$

$$IP = 4N$$

$$\therefore \text{type 0: } [LB \rightarrow 0000_2] \quad CS -$$

$$[HB \rightarrow 0000_1] \quad IP \quad [LB \rightarrow 0000_3]$$

LB = Lower Byte
HB = Higher Byte

Sat Sun Mon Tue Wed Thu Fri

Subject _____

P. O.S. II Asem

(M) Addressing & memory

Date: _____

<u>CS:IP</u>	<u>Phys Addr</u>	<u>Memory</u>
0000:0000	00000	05H
0000:0001	00001	34H
0000:0002	00002	00H
0000:0003	00003	20H

$$\text{TYPE 0: } 1000 + (01 \times 0000) \rightarrow 00000 \rightarrow 05(\text{LB})$$

$$IP = 4 \times 0 = 00000 \rightarrow 00001 \rightarrow 34(\text{HB})$$

$$CS = 4N + 2 = 00002 \rightarrow 00(\text{LB})$$

$$(not 00) \rightarrow 00003 \rightarrow 20(\text{HB})$$

$$IP = HB.LB = 3405$$

$$CS = HBLB = 2000$$

$$\text{ISR. Add Phys. Address} \rightarrow CS \times 10 + IP$$

$$84 = 2000 \times 10 + 3405$$

$$= 23405 \text{ H (Ans)}$$

TYPE 255 (table in slide)

$$IP = 4 \times 255 = (1020)_{10} = (003FC)H \rightarrow 003FD$$

$$CS = (4 \times 255) + 2 = 1022 = 003FB \rightarrow 0041$$

$$\therefore IP: 3322 \text{ H}$$

$$- 003AF \rightarrow 40 \text{ H}$$

$$\therefore CS: 4000 \text{ H}$$

$$H.P = 91$$

$$\therefore \text{ISR. P.A} \rightarrow 4000 \times 10 + 3322$$

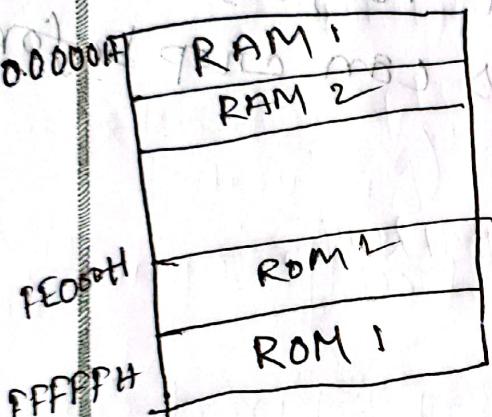
$$\rightarrow 43322 \text{ H}$$

TOPIC NAME: Microprocessor (self)

DAY: _____
TIME: _____ DATE: / /

Ex-4 Interface two $4K \times 8$ EPROM and two $4K \times 8$ RAM chips with 8086.

$$\text{ROM 2 chips} = (4K \times 8) \times 2 \Rightarrow 8K \times 8 \Rightarrow 8 \text{ KB}$$



$$\begin{aligned} &\Rightarrow 2^3 \times 10 \times 8 \\ &= 2^{13} \times 8 \\ \text{Address} &= 13 \quad (\text{only for offset}) \\ \text{Data} &= 8 \end{aligned}$$

Suppose,
Ending Address ROM = FFFFH

0000 0001 1111 1111 1111
0 1 F F F H

$$\begin{aligned} \text{Starting Address ROM} &= (FFFFF - 01FFF)H \\ &= FEO00H \end{aligned}$$

for RAM = 00000H

starting

RAM = 4KB

$= 2^{12}$. Address = 12

A0 = Bank selection.

TOPIC NAME: _____ DAY: _____

TIME: _____ DATE: / /

RAM	$\rightarrow E$	A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

ROM	$\rightarrow Even$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
ROM	$\rightarrow odd$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

- Total Memory
- Address Line
- Offset
- Starting

RAM + ROM $\xrightarrow{\text{Total Memory}}$

- $\rightarrow Even + odd$
- $\rightarrow Even + odd \rightarrow Add Line$
- $\rightarrow starting \& ending$

TOPIC NAME: _____

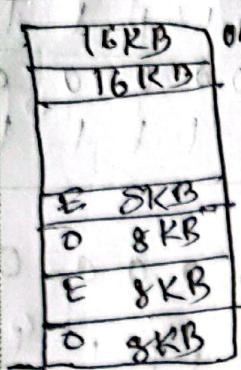
DAY: _____

TIME: _____

DATE: 2 / /

Ex-5:

ROM =

$$\begin{array}{l} 32 \text{ KB} \\ \times 2^4 \\ \hline 32 \text{ KB} \\ = 4 \end{array}$$


$$\begin{aligned} & 32 \text{ KB} \\ & = 2^5 \times 2^{10} \times 8 \end{aligned}$$

$$= 2^{15} \quad \text{Address} = 15$$

$$\text{Data} = 8$$

FFFFF H

$$\begin{array}{ccccccccc} \text{Offset} = & 0000 & 0111 & 111 & 111 & 111 & 111 & 111 \\ & 0 & . & 7 & F & F & F & F \end{array}$$

$$\text{Starting} = \text{FFFFF} - 07FFF$$

$$= \text{F800D H}$$

Topic Name: Microprocessors & Microcontrollers

Day: Friday

Time:

Date: 06/12/2024

Interface two 4KB EPROM and two 4KB chips 8086.

EP ROM → Even → 4KB
I/O DID → 4KB

RAM → Even → 4KB

Odd → 4KB

partial decoding → All is not required.

Absolute decoding → All pins required to design

Partial Decoding vs Absolute Decoding

Minimum Mode = Partial Decoding

Maximum Mode = Absolute

Memory Interfacing vs I/O Interfacing

CT - 8, 9, 11

