Interfacing Memory with 8086

Address decoding

- In general all the address lines are not used by the memory devices to select particular memory locations.
- The remaining line are used to generate chip select logic.
- Following two techniques are used to decode the address:

1) Absolute or Full decoding

2) Linear or Partial decoding

Absolute or full decoding

- All the higher address lines are decoded to select the memory chip.
- The memory chip is selected only for the specified logic levels on these higher order address lines.
- So each location have fixed address.
- This technique is expensive
- It needs more hardware than partial decoding.

Partial or Linear Decoding

- This technique is used in the small system
- All the address lines are not used to generate chip select logic
- Individual High order address lines are used to decode the chip select for the memory chips.
- Less hardware is required.
- Drawback is address of location is not fixed, so each location may have multiple address.

Q. 1: Interface 32 KB of RAM memory to the 8086 microprocessor system using absolute decoding with the suitable address.

Step_1: Total RAM memory = 32 KB
Half RAM capacity = 16 KB
hence,
number of RAM IC required = 2 ICs of 16 KB
so,

EVEN Bank = 1 ICs of 16 KB RAM

ODD Bank = 1 ICs of 16 KB RAM

Even bank	Odd bank
RAM _1 (16KB)	RAM _2 (16KB)

Step_2: Number of address lines required = 15 address lines

Step_3: Address decoding table

MEMORY IC	HEX ADDRESS	BINARY ADDRESS																			
		A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
16 K x 8 RAM-(1)	00000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	07FFE	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

RAM-2 < 00001H
07FFFH

Q. 2: Interface 32 K word of memory to the 8086 microprocessor system . Available memory chips are 16 K x 8 RAM. Use suitable decoder for generating chip select logic.

Step_1: Total memory = 32 K word = 32*2 K = 64 K

IC available = 16 K

hence,

number of RAM IC required = 64 K x 8/ 16 Kx8 = 4 ICs

so,

EVEN Bank = 2 ICs of 16 Kx8 RAM

ODD Bank = 2 ICs of 16 Kx8 RAM

Even bank	Odd bank
RAM _1 (16K)	RAM _2 (16K)
RAM_ 3 (16K)	RAM _4 (16K)

Step_2: Number of address lines required = 15 address lines

Step_3: Address decoding table

MEMORY IC	HEX ADDRESS	BINARY ADDRESS																			
		A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
16 K x 8 RAM-(1)	OOOOO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	07FFE	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
16 K x 8 RAM-(3)	8000	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0FFFE	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Q. 3: Interface the following memory ICs with the 8086 microprocessor system in minimum mode configuration.
ROM 4K-2 Numbers
EPROM 64K-1 Numbers
RAM 32K- 1Number . Use partial decoding.

Step_1: Total ROM memory = 4 KB ---- 2 ICs

EVEN Bank = 1 ICs of 4 KB ROM

ODD Bank = 1 ICs of 4 KB ROM

Total EPROM memory = 64 KB

EVEN Bank = 1 ICs of 32 KB EPROM
ODD Bank = 1 ICs of 32 KB EPROM

Total RAM memory = 64 KB

EVEN Bank = 1 ICs of 16 KB RAM
ODD Bank = 1 ICs of 16 KB RAM

Even bank	Odd bank
ROM _1 (4KB)	ROM _2 (4KB)
EPROM _1 (32KB)	EPROM _2 (32KB)
RAM _1 (16KB)	RAM _2 (16KB)

Step 2:

Number of address lines required for ROM = 13 address lines
Number of address lines required for EPROM = 16 address lines
Number of address lines required for RAM = 15 address lines

Step_3: Address decoding table

MEMORY IC	HEX ADDRESS	BINARY ADDRESS																		
		A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
4 K x 8 ROM-(1)	**FFFFE**	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
	FE000	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
									← To ROM IC →												
32 K x 8 EPROM-(1)	**EFFFE**	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
	E0000	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
						← To EPROM IC →															
16 K x 8 RAM-(1)	**D0000**	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	D7FFE	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
		← To decoder →					← To RAM IC →														