Mulat Tiruye
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Personal Summary:

I am currently pursuing a Master's in Computer Engineering at the University of Pisa, Italy. I am a dedicated and highly motivated professional actively seeking opportunities for employment, internships, or further studies. My interests and expertise span computer architecture, photonic computing, quantum computing, cloud computing, parallel and distributing computing, high-perfomance computing, artificial intelligence (AI), machine learning (ML), VLSI design (digital IC design), software engineering and hardware acceleration for ML and AI, as well as other areas related to electrical, nanoelectronics, and computer engineering.

EDUCATION

Sep 2023 - Current — **University of Pisa, Italy**
Master's in Computer Engineering

Sep 2021 to April 2023 — **Singapore University of Technology and Design(SUTD), Singapore**
Master of Engineering in Nano Electronics Engineering and Design
Dissertation: "Dual Mode Systolic Array based Processing Element for CNN accelerator"
Advisor: Dr. Teo Tee Hui

Sep 2021 to April 2023 — **Chang Gung University(CGU), Taiwan**
Master of Science in Nano Electronics Engineering and Design
Dissertation: "Dual Mode Systolic Array based Processing Element for CNN accelerator"
Advisor: Professor, I Wey & Dr. Teo Tee Hui

Jul 2017 to Aug 2021 — **Kalinga Institute of Industrial Technology (KIIT) University, India**
Bachelor of Technology in Electronics and Electrical Engineering

RESEARCH EXPERTISE

Skills and Qualifications

- Digital IC Design
- CMOS Design, FPGA based design
- Hardware design on FPGA, ASIC
- Hardware accelerator design
- Machine Learning and Artificial Intelligence
- Public speaking, training, and speechwriting
- Outstanding written and oral communications
- Team building and leadership
- VLSI design
- Computer processor (INTEL, ARM)
- Software Engineering
- Full Stack Development
- ML tool (CNN, DLL, ANN, Torch, NN)
- Database analysis
- Computer networking
- Research and analysis.

Computing skills:

Hardware/Software Design Tool

- Xilinx–Vivado
- LTSPICE-IC design
- Cadence-IC Design
- Altium PCB Design
- MATLAB/Simulink

Computer Language

- Verilog
- VHDL
- C/ C++ Programming
- Python, JAVA and MATLAB Programing
- JAVASCRIPT, HTML & CSS

Languages: Amharic (native), English (Proficient), Italiano (Beginner)

Project:

May 2024- July 2024: **Analyze letter count through Hadoop**
- Cloud Computing based.

March 2024-April 2024: **Object Recognition Using Yolov5**
- Design for object recognition.
- Machine Learning using CNN.

April 2022- June 2022**: Design and Simulation of PLL**
- For stability and jitter analyses for IC clocking.
- The designed PLL achieved a 155MHz and
- Suitable for a highspeed circuit design.

April2022- June 2022**: Delta Modulator**
- Designed and simulated using LTSPICE**.**
- Used for encoding signals from analog to PCM.
- Suitable for ADC or DAC design.

May 2024 -: **Designing Photonic IC (<u>under progress</u>)**
- For Quantum Computing
- Neuromorphic Systems

Nov 2023- Feb 2024: **Database Management System**
- Design for database management.
- CineLink: Application platform.

March 2022-April 2022**: Sampling Circuit**
- Design and simulated for sample and hold circuits.
- Used for ADC or DAC design.
- Suitable for a Mixed Signal circuit design.

Nov2021- Jan 2022**: High Gain Op-amp**
- Design and simulated for stability analysis.
- The designed OpAmp achieved a 106dB and
- Suitable for a High-Gain circuit design.

TEACHINNG ASSISTANT: Singapore University of Technology and Design (SUTD)

Jun 2022-Mar 2023
- Digital Electronics: contributed to provide lecture note.
- Machine Learning and AI: contributed to data collection.

AWARDS
- **MAECI Scholarship, Italian Government, Aug 2023**
- NEED Scholarship, SUTD, Aug 2021
- Betere Science Scholarship, Ethiopian Government, July 2017

PROFESSIONAL ASSOCIATIONS
- IEEE (Institute of Electrical and Electronics Engineering) Members
- IEEE Young Professionals

PUBLICATIONS

- **MA Tiruye**, OB Gerba, T.Hui Teo. A 155 MHz Low-Jitter PLL for Enhanced Signal Integrity in High-Speed Interconnects. IEEE. [2024] [**<u>Accepted and will be presented</u>**]
- Shi Hui Chua, T. Hui Teo, **Mulat Ayinet Tiruye**, I-Chyn Wey. Systolic Array-Based Convolutional Neural Network Inference on FPGA. IEEE. [2023]
- Tan Rong Loo, T. Hui Teo, **Mulat Ayinet Tiruye**, I-Chyn Wey (2023). High-Performance Asynchronous CNN Accelerator with Early Termination. IEEE. [2023]

References:

1**. <u>Dr.Teo Tee Hui</u>**: Engineering Product Development, Science, Mathematics and Technology, Singapore University of Technology and Design, Singapore. [Thesis Advisor]
Phone:+**656564994604**, Email: **<u>tthui@sutd.edu.sg</u>**

2**. <u>Professor Tan Cher Ming</u>**: Chair professor, director, CReST center, Chang Gung University, Tiawan. [Instructor]
Phone number: **(+886) 88632118800**, Email: **<u>cmtan@cgu.edu.tw</u>**

3. **<u>Professor Bing J. Sheu</u>:** Chair Professor, Department of Electronics Engineering, Chang Gung University, Tiawan. [Instructor]
Phone number: **(+886) 88632118800**, Email: **<u>bsheu@mail.cgu.edu.tw</u>**