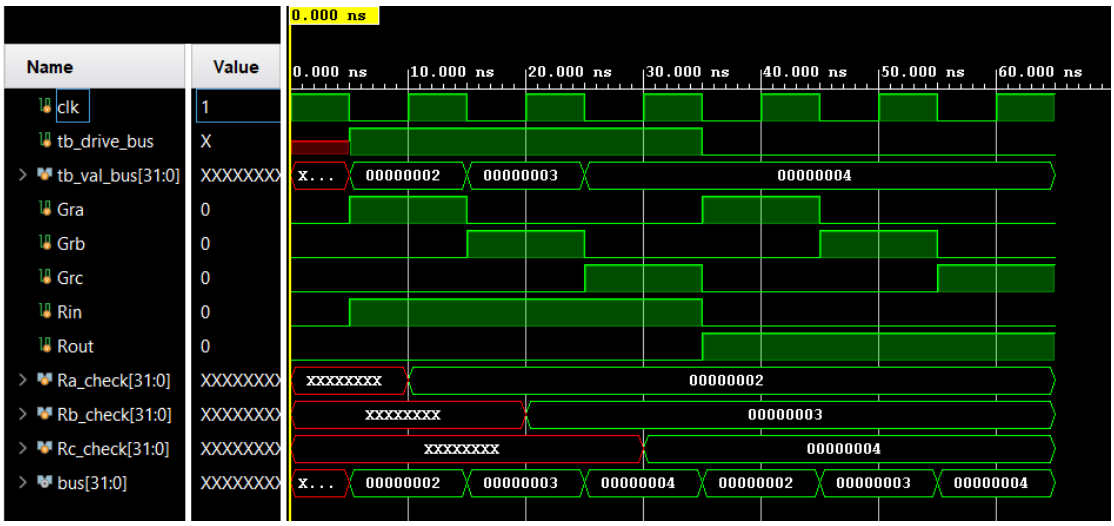
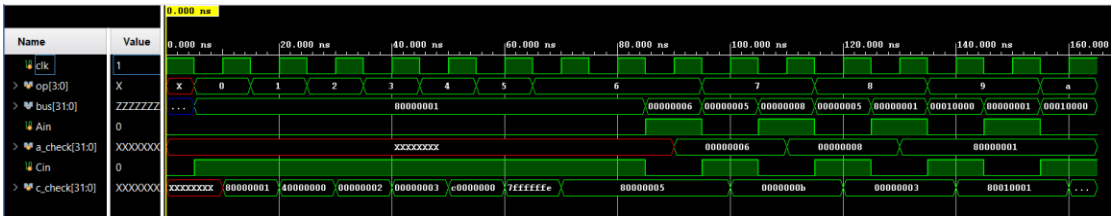
Waveform Outputs from Multiple Testbenches

Register File :

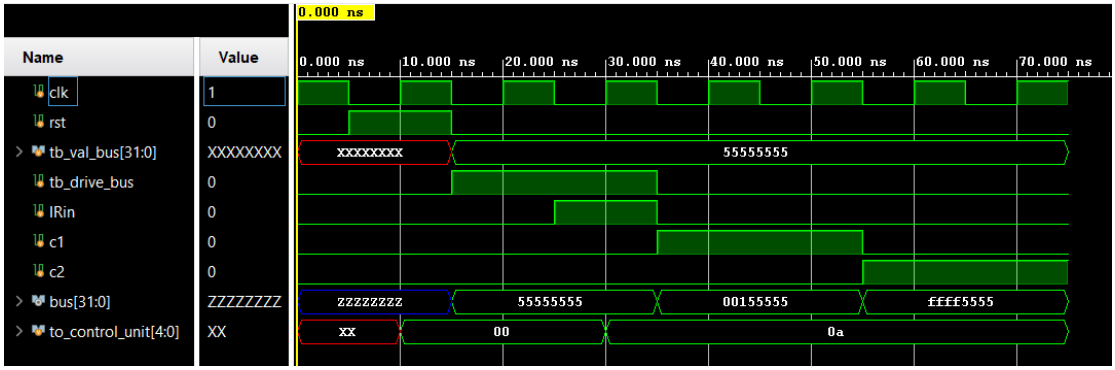


ALU :



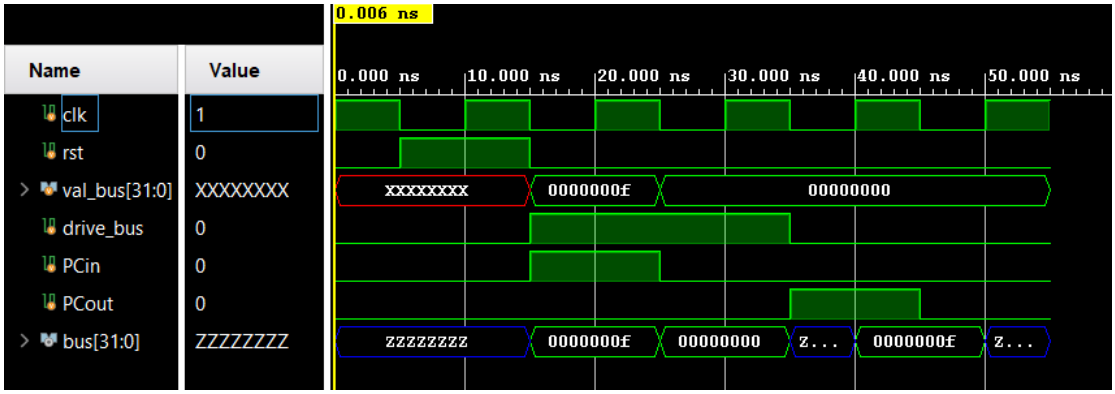

```
# run 1000ns
BtoC : b = 10000000000000000000000000000001 ; c = 10000000000000000000000000000001
shr  : b = 10000000000000000000000000000001 ; c = 01000000000000000000000000000000
shl  : b = 10000000000000000000000000000001 ; c = 00000000000000000000000000000010
shc  : b = 10000000000000000000000000000001 ; c = 00000000000000000000000000000011
shra : b = 10000000000000000000000000000001 ; c = 11000000000000000000000000000000
not  : b = 10000000000000000000000000000001 ; c = 01111111111111111111111111111110
inc4 : b = 2147483649 ; c = 2147483653
add  : 6 + 5 = 11
sub  : 8 - 5 = 3
or   : 10000000000000000000000000000001 OR 00000000000000001000000000000000 = 10000000000000001000000000000001
and  : 10000000000000000000000000000001 AND 00000000000000001000000000000000 = 00000000000000000000000000000000
$finish called at time : 175 ns : File "C:/Users/ADMIN1/Vivado_projects/project_1/project_1.srcs/sim_1/new/tb_ALU.sv" Line 117
```

IR :

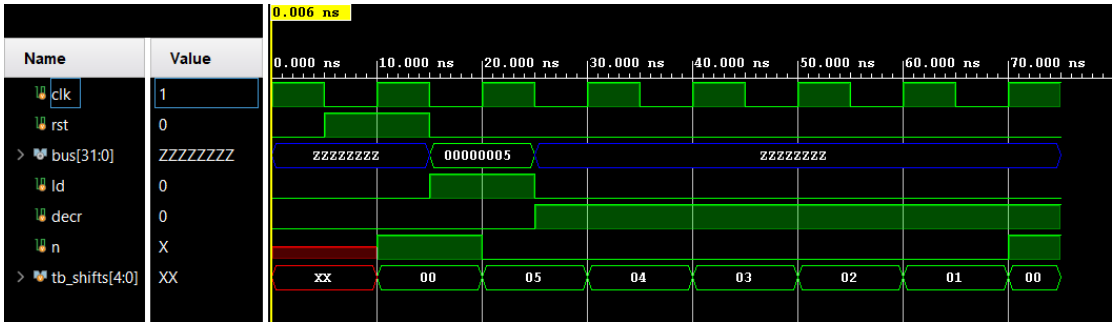



```
bus_in = 01010101010101010101010101010101
bus_c1 = 00000000000101010101010101010101
bus_c2 = 11111111111111110101010101010101
$finish called at time : 65 ns : File "C:/Users/ADMIN1/Vivado_projects/
```

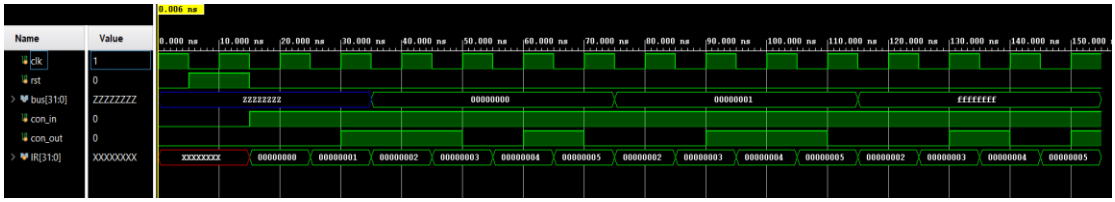
PC :



Shift Control Unit :



Condition Unit :

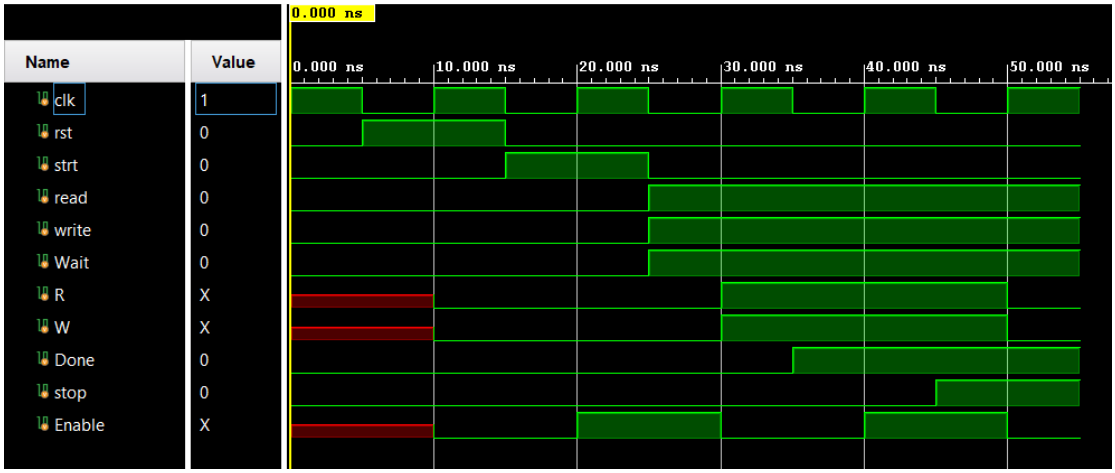



```
*value = 0*
=0  : 1
!=0 : 0
>=0 : 1
<0  : 0

*value = 1*
=0  : 0
!=0 : 1
>=0 : 1
<0  : 0

*value = -1*
=0  : 0
!=0 : 1
>=0 : 0
<0  : 1
$finish called at time : 144999 ps : File "C:/Users/ADMIN1/Vivado_projects/simple_riscV/CPU_simple_riscV/sim_1/new/tb_con_u.sv" Line 93
```

Clocking Logic



Control Unit