1.4.1. Format summary

This section provides a summary of the ARM, and Thumb instruction sets:

- *ARM instruction summary*
- *Thumb instruction summary*.

A key to the instruction set tables is provided in Table 1.1.

The ARM7TDMI processor uses an implementation of the ARMv4T architecture. For a complete description of both instruction sets, see the *ARM Architecture Reference Manual*.

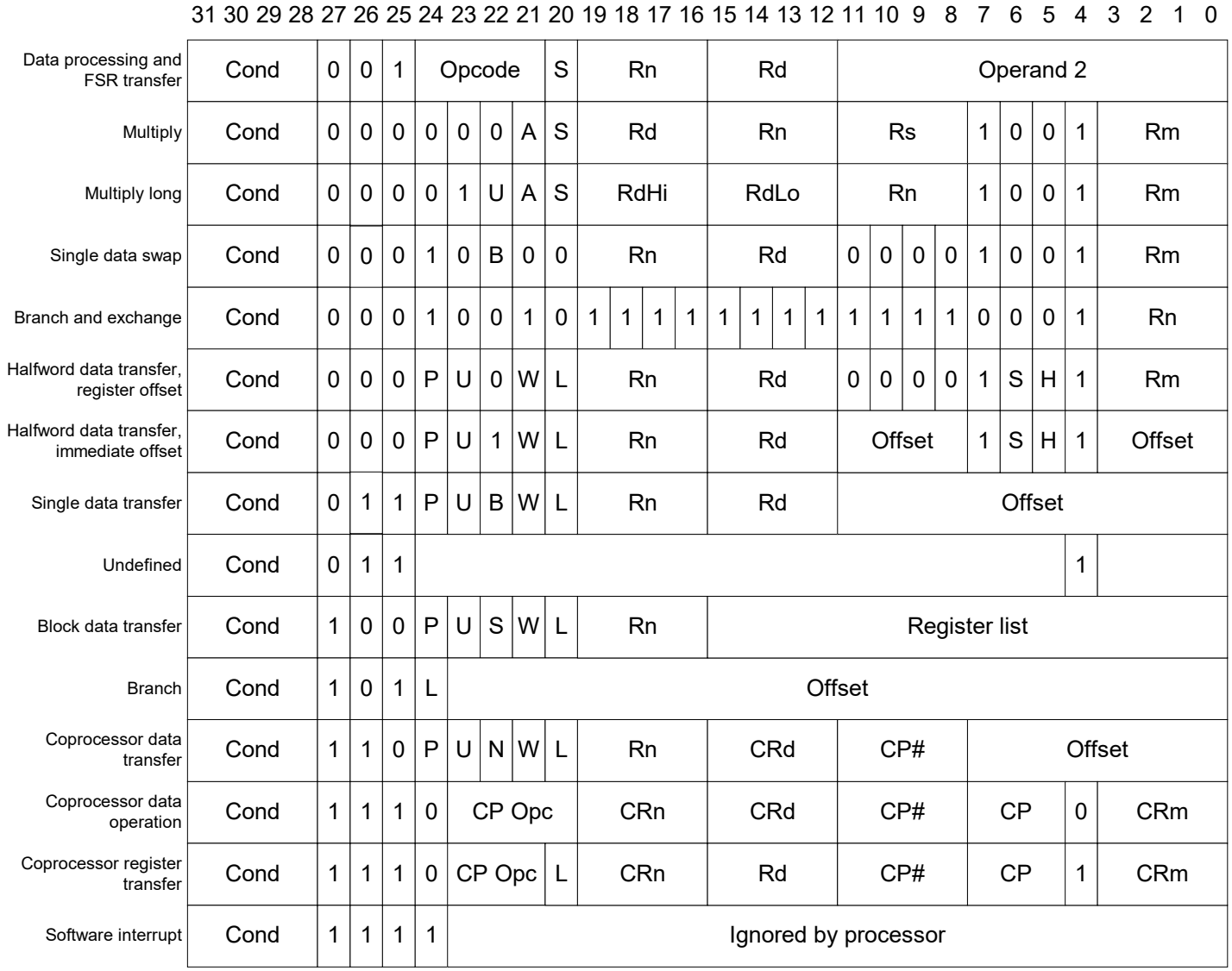
Table 1.1. Key to tables

Type	Description
`{cond}`	Condition field, see Table 1.6.
`<Oprnd2>`	Operand2, see Table 1.4.
`{field}`	Control field, see Table 1.5.
S	Sets condition codes, optional.
B	Byte operation, optional.
H	Halfword operation, optional.
T	Forces address translation. Cannot be used with pre-indexed addresses.
Addressing modes	See *Addressing modes*.
`#32bit_Imm`	A 32-bit constant, formed by right-rotating an 8-bit value by an even number of bits.
`<reglist>`	A comma-separated list of registers, enclosed in braces ({ and }).

The ARM instruction set formats are shown in Figure 1.5.

See the *ARM Architectural Reference Manual* for more information about the ARM instruction set formats.

Figure 1.5. ARM instruction set formats



Note

Some instruction codes are not defined but do not cause the Undefined instruction trap to be taken, for instance a multiply instruction with bit [6] changed to a 1. These instructions must not be used because their action might change in future ARM implementations. The behavior of these instruction codes on the ARM7TDMI processor is unpredictable.