

1.4.1. Format summary

This section provides a summary of the ARM, and Thumb instruction sets:

- *ARM instruction summary*
- *Thumb instruction summary.*

A key to the instruction set tables is provided in Table 1.1.

The ARM7TDMI processor uses an implementation of the ARMv4T architecture. For a complete description of both instruction sets, see the *ARM Architecture Reference Manual*.

Table 1.1. Key to tables

Type	Description
{cond}	Condition field, see Table 1.6.
<Oprnd2>	Operand2, see Table 1.4.
{field}	Control field, see Table 1.5.
S	Sets condition codes, optional.
B	Byte operation, optional.
H	Halfword operation, optional.
T	Forces address translation. Cannot be used with pre-indexed addresses.
Addressing modes	See <i>Addressing modes</i> .
#32bit_Imm	A 32-bit constant, formed by right-rotating an 8-bit value by an even number of bits.
<reglist>	A comma-separated list of registers, enclosed in braces ({ and }).

The ARM instruction set formats are shown in Figure 1.5.

See the *ARM Architectural Reference Manual* for more information about the ARM instruction set formats.

Figure 1.5. ARM instruction set formats

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Data processing and FSR transfer	Cond	0	0	1	Opcode				S	Rn				Rd				Operand 2																
Multiply	Cond	0	0	0	0	0	0	A	S	Rd				Rn				Rs				1	0	0	1	Rm								
Multiply long	Cond	0	0	0	0	1	U	A	S	RdHi				RdLo				Rn				1	0	0	1	Rm								
Single data swap	Cond	0	0	0	1	0	B	0	0	Rn				Rd				0	0	0	0	1	0	0	1	Rm								
Branch and exchange	Cond	0	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	Rn						
Halfword data transfer, register offset	Cond	0	0	0	P	U	0	W	L	Rn				Rd				0	0	0	0	1	S	H	1	Rm								
Halfword data transfer, immediate offset	Cond	0	0	0	P	U	1	W	L	Rn				Rd				Offset				1	S	H	1	Offset								
Single data transfer	Cond	0	1	1	P	U	B	W	L	Rn				Rd				Offset																
Undefined	Cond	0	1	1																							1							
Block data transfer	Cond	1	0	0	P	U	S	W	L	Rn				Register list																				
Branch	Cond	1	0	1	L	Offset																												
Coprocessor data transfer	Cond	1	1	0	P	U	N	W	L	Rn				CRd				CP#				Offset												
Coprocessor data operation	Cond	1	1	1	0	CP Opc				CRn				CRd				CP#				CP		0	CRm									
Coprocessor register transfer	Cond	1	1	1	0	CP Opc				L	CRn				Rd				CP#				CP		1	CRm								
Software interrupt	Cond	1	1	1	1	Ignored by processor																												
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		

Note

Some instruction codes are not defined but do not cause the Undefined instruction trap to be taken, for instance a multiply instruction with bit [6] changed to a 1. These instructions must not be used because their action might change in future ARM implementations. The behavior of these instruction codes on the ARM7TDMI processor is unpredictable.