

Lab. 06

Logic Design Lab.

Spring 2022

Prof. ChangGun Lee

(cglee@snu.ac.kr)

TA. Hayeon Park

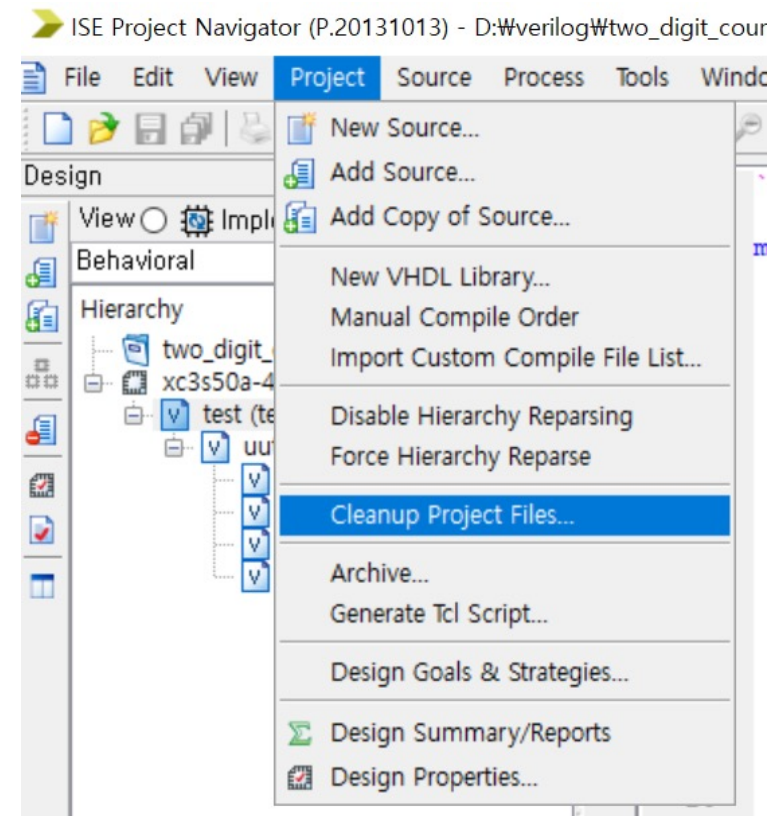
TA. Haejoo Jeon

TA. Seohwan Yoo

(rubis.ld.ta@gmail.com)

Announcement

- Do not open multiple simulation window
- Before exiting the Xilinx ISE program, take the following two steps:
 - Close the simulation window
 - Project → Cleanup Project Files...
- There is an issue where the log file becomes abnormally large in certain situations. In this case, the log file runs out of disk space and cannot use the computer normally.



Sequential logic

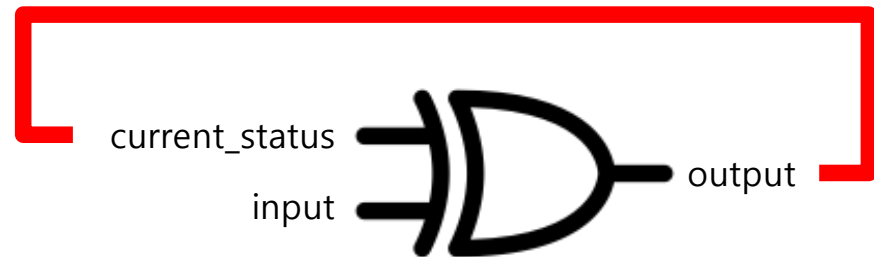
Sequential logic (1)

- Output is determined by both of **current state** and **input**
- To save current state, **feedback** is used to implement storage

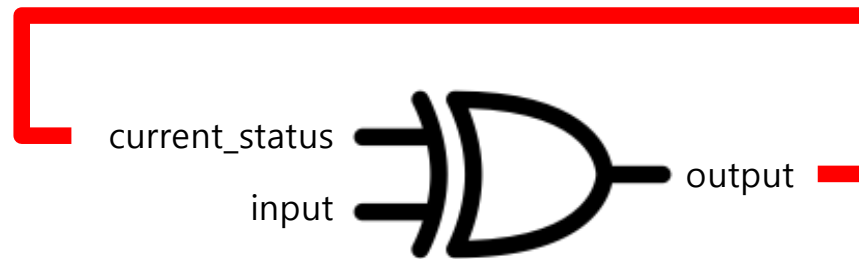
Example > sequential logic

If **input == 0** then **hold current status**, else if **input == 1** then **toggle current status**.
Output is same as current status.

current_status	input	output
0	0	0
0	1	1
1	0	1
1	1	0



Sequential logic (2)

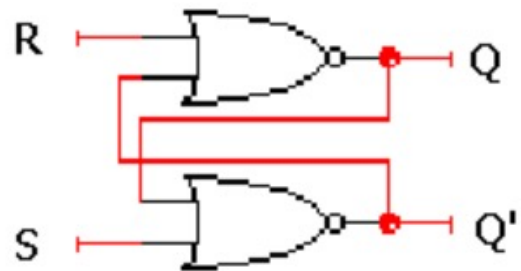


Taxonomy ...

- Never mind, always work
→ Latch
- Work only when it is enabled
→ Gated latch
- Work only when it is edge triggered
→ Flip-flop

R-S Latch

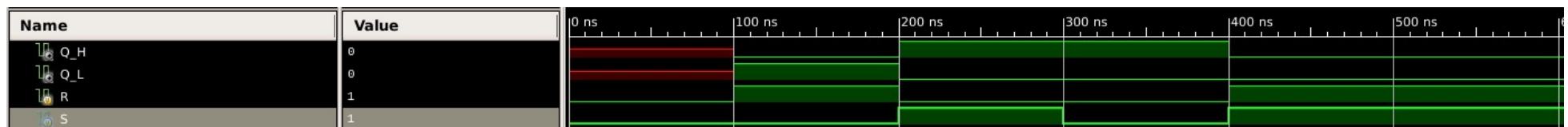
- R-S latch is a **1 bit memory** with cross-coupled gates.



S	R	Q
0	0	hold
0	1	0
1	0	1
1	1	unstable

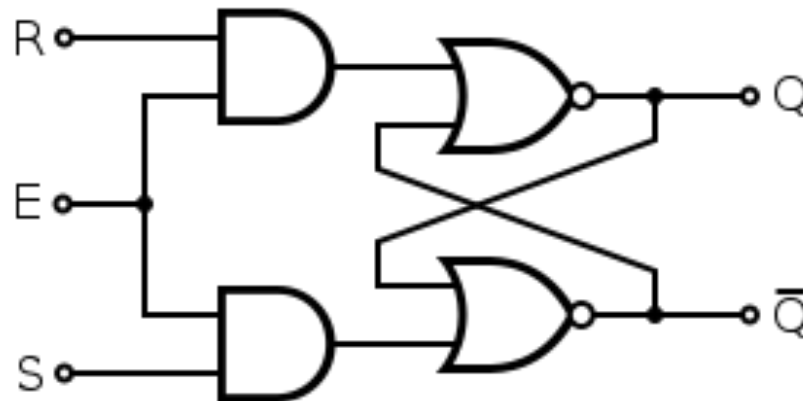
S	R	Q(t)	Q(t+Δ)	
0	0	0	0	hold
0	0	1	1	
0	1	0	0	reset
0	1	1	0	
1	0	0	1	set
1	0	1	1	
1	1	0	X	not allowed
1	1	1	X	

Q	RS	00	01	11	10
0			1	X	
1		1	1	X	

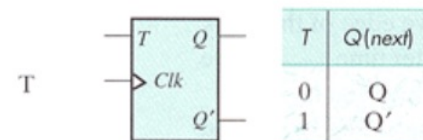
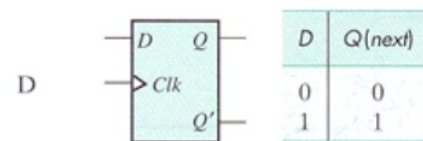
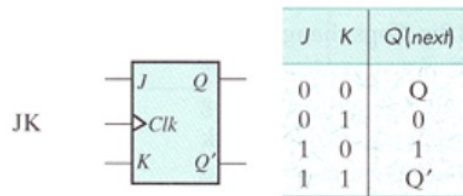
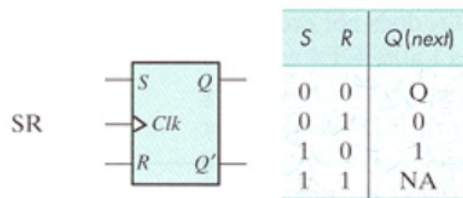


Gated R-S Latch

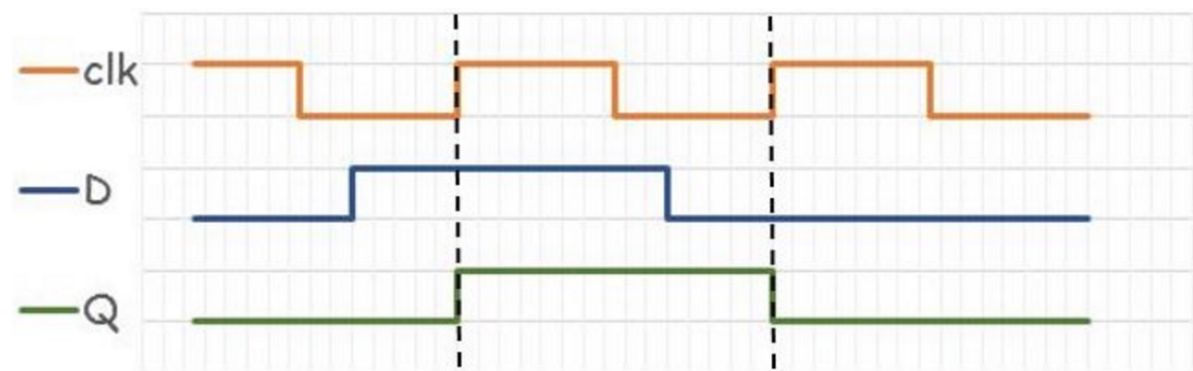
- R and S(inputs) matter only when E(enable) = 1
- Otherwise, hold current state



Flip-Flops



D FlipFlop



Clock

Clock

- Provide **timing** to sequential logic (ex. Flip-Flop)

74LS74, 74ALS74, 74VLS74
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

Recommended operating conditions			
	MIN.	MAX.	UNIT
V _{CC} Supply voltage	4.5	5.5	V
V _{IL} Input low-level voltage	0	1.5	V
V _{OL} Output low-level voltage	0	0.5	V
I _{IL} Input low-level current	-1.6	1.6	mA
I _{OL} Output low-level current	-4	4	mA
t _{CLK} Clock frequency	0	25	kHz
t _{PD} Pulse duration	20	20	ns
t _{SET} Setup time before CLK ↑	20	20	ns
t _{CLR} Clear time before CLK ↑	20	20	ns
t _{CO} Propagation delay CLK → Q	5	6	ns
T _A Operating free-air temperature	-55	125	°C

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS ¹	MIN. VALUE	MAX. VALUE
V _{TH}	V _{CC} = MIN. V _{CC} = MAX. V _{IL} = 2 V. V _{OL} = MAX.		
V _{OL}	V _{CC} = MIN. V _{CC} = MAX. V _{IL} = 0 mA. V _{OL} = MAX.		
I _{IL}	V _{CC} = MAX. V _I = 1 V.		
I _{OL}	V _{CC} = MAX. V _I = 2 V.		
I _{CC1}	V _{CC} = MAX. V _I = 0 V.		
I _{CC2}	V _{CC} = MAX. V _I = 1 V.		
I _{CC3}	V _{CC} = MAX. V _I = 2 V.		
I _{CC4}	V _{CC} = MAX. V _I = 0 V.		
I _{CC5}	V _{CC} = MAX. V _I = 1 V.		

¹ For measurements shown at MIN. or MAX., use the appropriate value specified under test 1 and 2. For measurements shown at 25°C, use the appropriate value specified under test 3.

² For measurements shown at 25°C, use the appropriate value specified under test 3.

³ For measurements shown at 25°C, use the appropriate value specified under test 3.

⁴ For measurements shown at 25°C, use the appropriate value specified under test 3.

⁵ For measurements shown at 25°C, use the appropriate value specified under test 3.

⁶ For measurements shown at 25°C, use the appropriate value specified under test 3.

⁷ For measurements shown at 25°C, use the appropriate value specified under test 3.

⁸ For measurements shown at 25°C, use the appropriate value specified under test 3.

⁹ For measurements shown at 25°C, use the appropriate value specified under test 3.

¹⁰ For measurements shown at 25°C, use the appropriate value specified under test 3.

¹¹ For measurements shown at 25°C, use the appropriate value specified under test 3.

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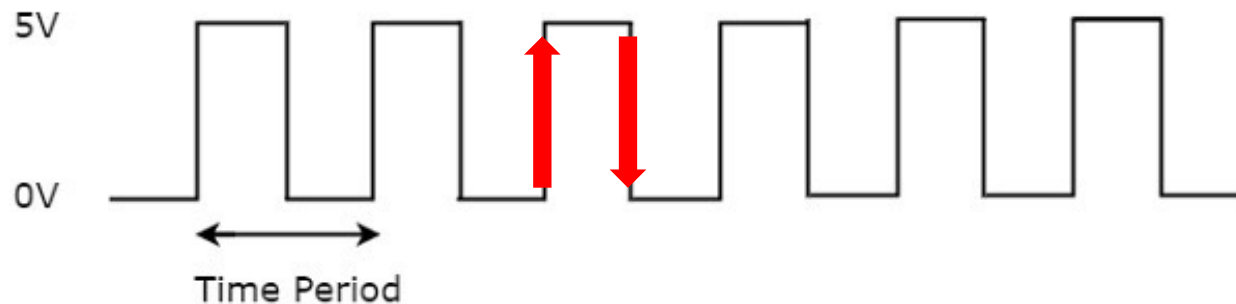
⁵⁰ For measurements shown at 25°C, use the appropriate value specified under test 3.

74LS74 Data

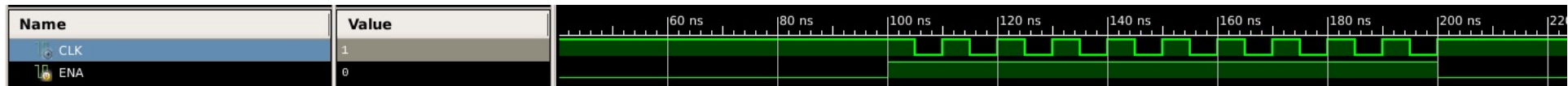
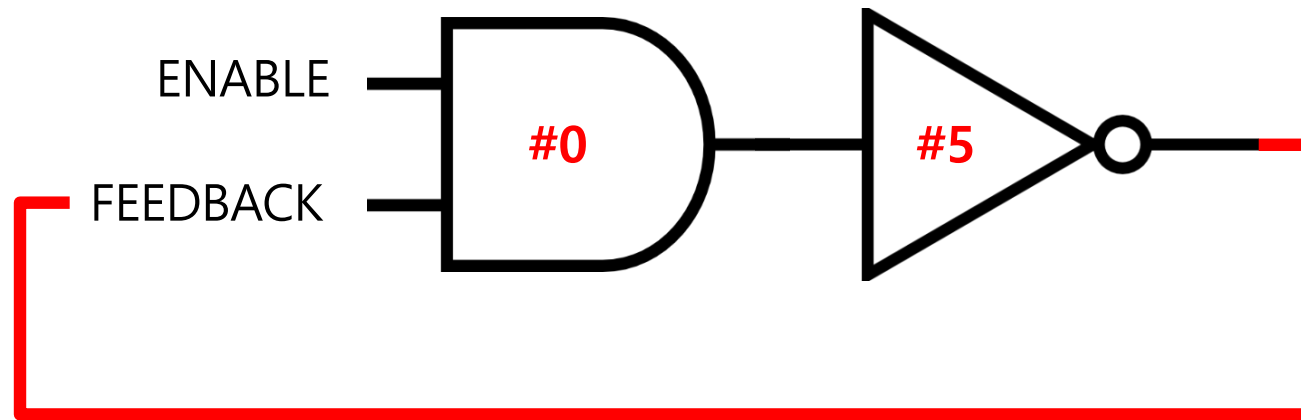
Parameter	Symbol	Value	Unit
t _W Pulse Width - Clock High - Preset Low - Clear Low	t _W	20	ns
t _{SL} Setup Time	t _{SL}	20	ns
t _{HL} Hold Time	t _{HL}	0	ns
f _{MAX} Max Clock Frequency	f _{MAX}	20	MHz
t _{PLH} Prop Delay, Clock-to-Q	t _{PLH}	35	ns
t _{PLH} Prop Delay, Preset-to-Q	t _{PLH}	35	ns
t _{PLH} Prop Delay, Clear-to-Q	t _{PLH}	35	ns

Absolute Maximum Ratings			
EZYTrigger Type			
Parameter	Symbol	AT416 - 40	AT416 - 80
Peak voltage - positive and negative	V _p	4000 V	8000 V
Nominal mains voltage	V _m	1250 V	2500 V
Continuous DC voltage	V _c	2500 V	2500 V
Thyristor turn-on time (t _{on} = t _{on} + t _r)	t _{on}	6 μs	6 μs
Anode-Cathode transient immunity (dv/dt) _{IC}	(dv/dt) _{IC}	5000 V/μs	5000 V/μs
Ambient temperature range	T _a	-20°C to +85°C	-20°C to +85°C

Technical Data at 25°C			
500 mA Gate current threshold	V _{GT}	40 V	40 V
2.5 A Gate current threshold	V _{GT}	90 V	140 V
Gate current rise time @ Anode voltage = 800V	(dV/dt) _{IG}	1.2 A/μs	1.2 A/μs
Peak gate current	I _p	2.5 A	2.5 A
Anode-cathode current at V _p and I _g = 0	I _n	4 mA	4.6 mA
Maximum off-state gate current	I _o	2 μA	2 μA
Minimum control current (SFH756 Transm./ 3m fibre)	I _{cm}	5 mA	5 mA
Recommended control current (SFH756 Transm./ 3m fibre)	I _c	10 mA	10 mA
Control input voltage drop at 10mA	V _{in}	Typ 1.2 ± 1.5V	Typ 1.2 ± 1.5V
Maximum reverse control input voltage	V _{inv}	6 V	6 V
Turn-on delay time at I _{cm} = 10mA	t _{di}	7 μs	7 μs



Simple Oscillator



How to implement gate delay ?

Example >

```
wire tmp;  
assign #5 tmp = tmp & 1;
```

Homework

Homework

1. Implement the following in Verilog and simulate the behavior.

(1) a R-S latch

(2) a gated R-S latch using (1)

(3) a Simple Oscillator(the clock period is free)

(4) a R-S Flip-Flop(Edge-triggered) using above modules

Include Source codes(modules) and simulation result.

Explain that the modules you implement work well.

No need to attach testbench code.

2. (Optional) Explain the different Flipflops(SR, D, JK, etc.) and how they differ from each other.

Report

- Write a report
 - Either in Korean or in English
 - **Your report should include**
 - discussion
 - Homework (if there is any)
 - # of pages doesn't matter
 - Documents should be submitted as PDF file(**less than 25Mb**)
 - **Attach source code and waveform screenshot**
 - Due :
 - Class 001 - May, 2th (Before class begin at 7:00pm)
 - Class 002 - May, 3th (Before class begin at 7:00pm)
 - Class 003 - May, 4th (Before class begin at 7:00pm)