Lab. 04

Logic Design Lab.

Spring 2022

Prof. ChangGun Lee

(cglee@snu.ac.kr)

TA. Hayeon Park

TA. Seohwan Yoo

TA. Haejoo Jeon

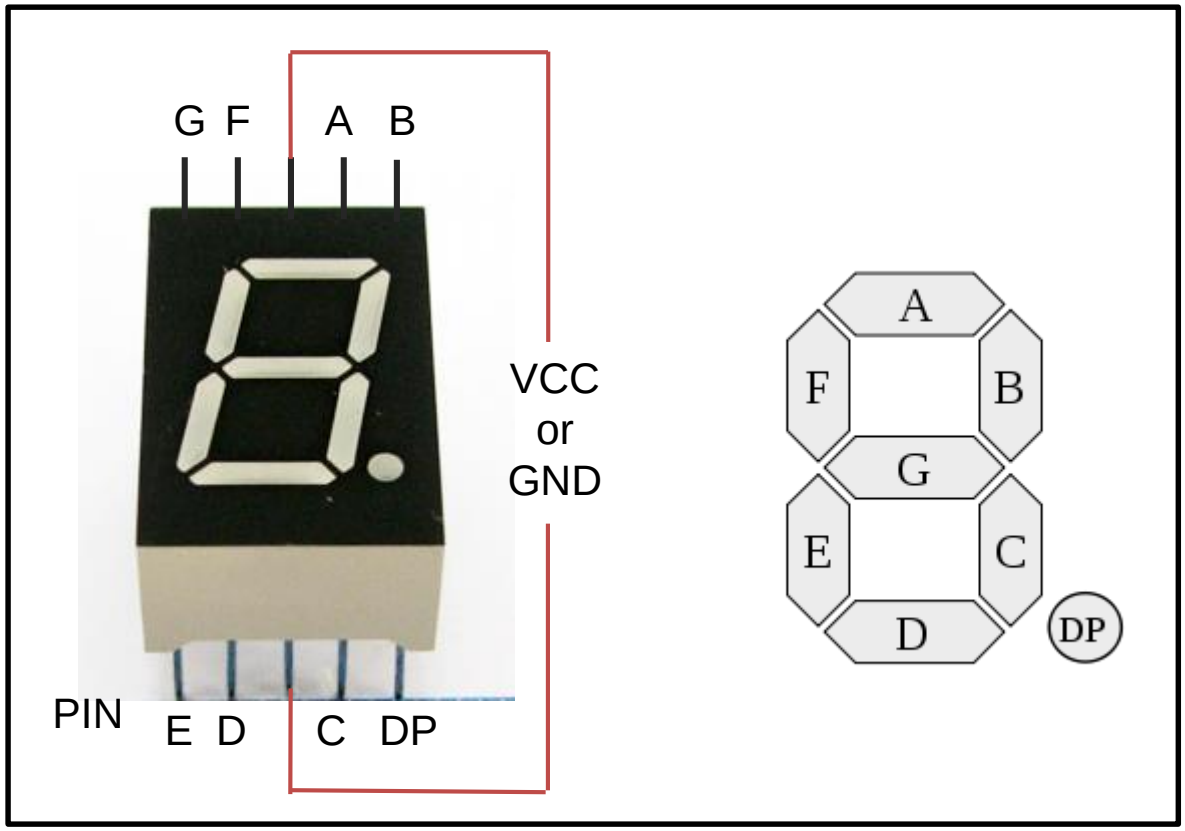
(ta@rubis.snu.ac.kr)

Contents

- **BCD to 7-segment Decoder**
- **Lab**
- **Homework**

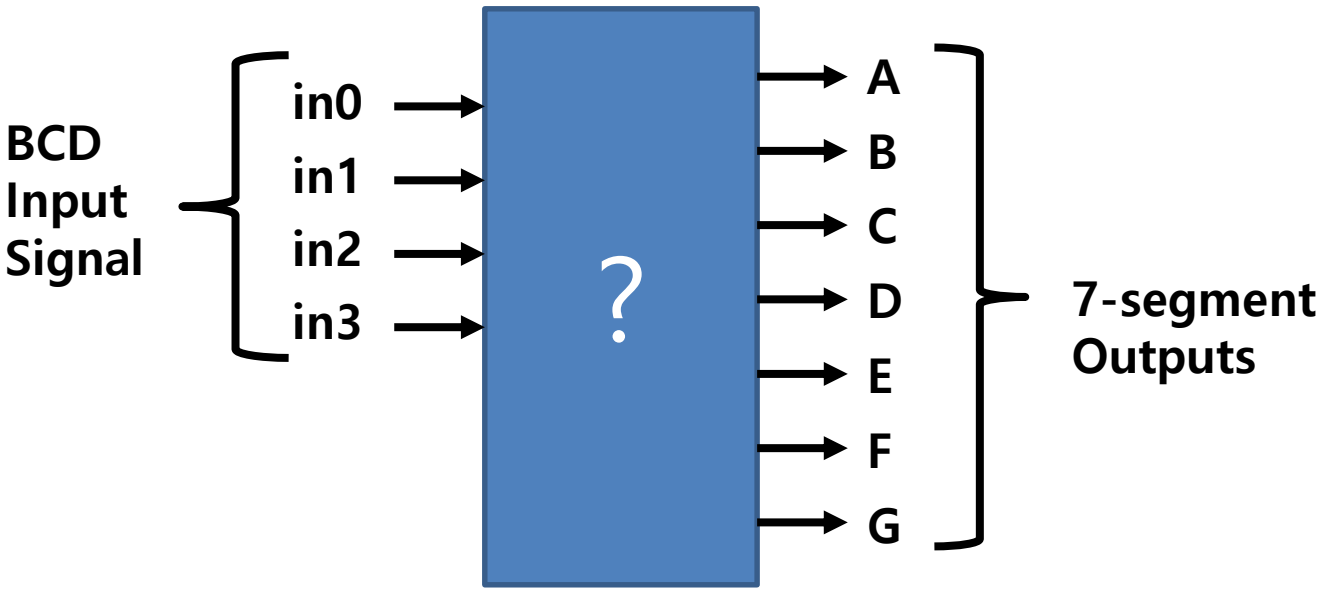
BCD to 7-segment Decoder

7-segment Display



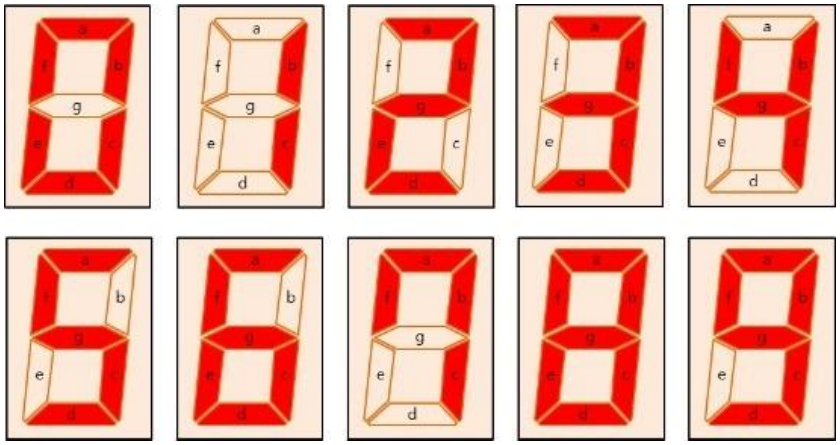
- A form of electronic display device for displaying decimal numerals that is an alternative to the more complex dot-matrix displays.
- Widely used in digital clocks, electronic meters, and other electronic devices for displaying numerical information.

BCD to 7-segment Decoder



We need a decoder like above
So we will make it

BCD to 7-segment Decoder (cont'd)



Step

1. Make a truth table with BCD and 7-segment outputs
2. Make Boolean expressions according to the table
3. Minimize them
4. Implement a decoder according to the expressions

Lab

Today

- **Implement BCD to 7-segment Decoder** on Xilinx ISE in

  1) Structural description

  2) Data-flow style description

  3) Behavioral description

  and simulate each of them

Homework

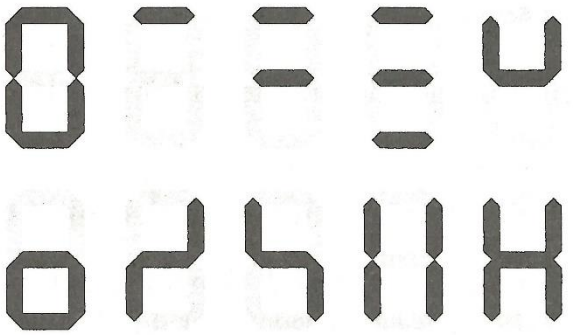
- **Implement 'Klingon number system' Decoder for 7-segment** on Xilinx ISE in

  1) Structural description

  2) Data-flow style description

  3) Behavioral description

  and simulate each of them



Pic. Klingon number system

Report

- **Lab part**
  1. Xilinx source code
  2. Result of simulation

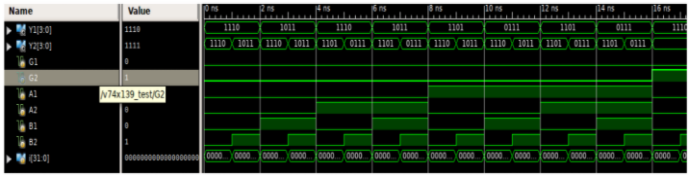
- **Homework part**
  1. Truth table, Karnaugh map, Boolean expression
  2. Xilinx source code
  3. Result of simulation

- **Due**
  - **4 / 18 (Mon) Class 001**
  - **4 / 19 (Tue) Class 002**
  - **4 / 20 (Wed) Class 003**

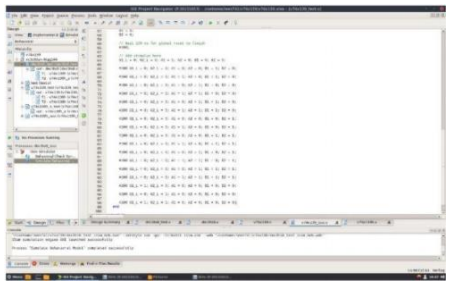
Report

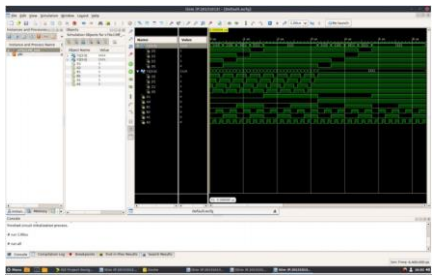
- **We can’t see your picture.**
  - **Please don’t capture the whole screen but only the proper bound of the screen.**
  - **Also don’t take picture of your monitor. Capture the page.**

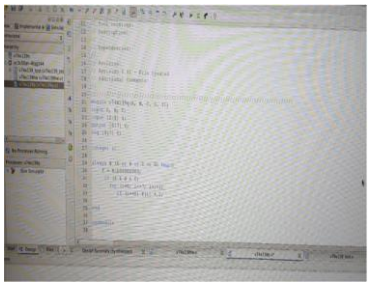
```
21  module v74x139(
22      input G1,
23      input G2,
24      input A1,
25      input A2,
26      input B1,
27      input B2,
28      output [3:0] Y1,
29      output [3:0] Y2
30      );
31
32      v74x139h T1(.G(G1), .A(A1), .B(B1), .Y(Y1));
33      v74x139hD T2(.G(G2), .A(A2), .B(B2), .Y(Y2));
34
35  endmodule
36
```



Good case







Bad case

Questions