Lab. 06

Logic Design Lab.

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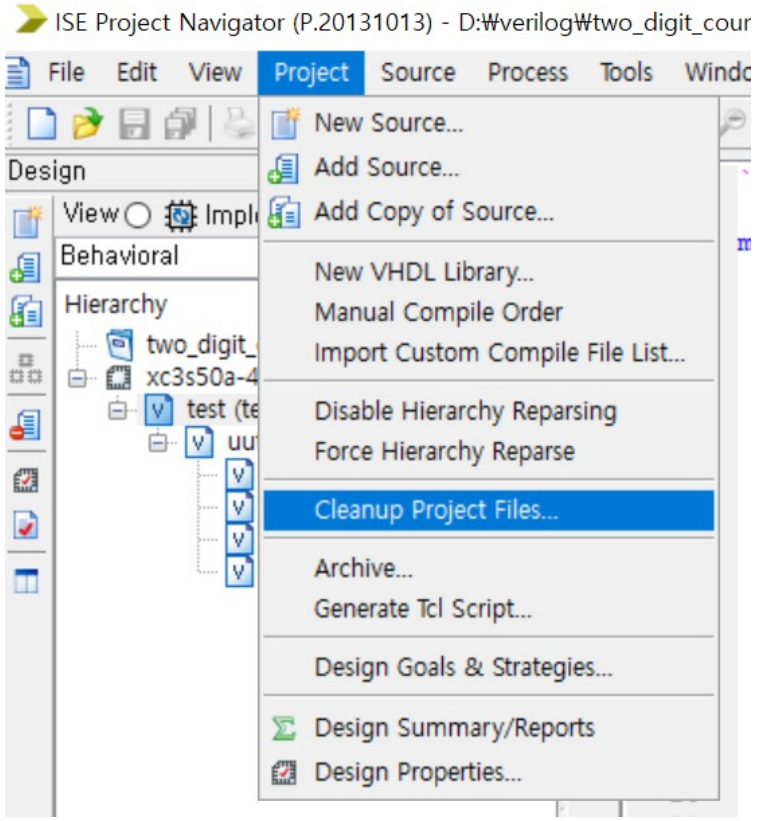
Announcement

- Do not open multiple simulation window
- Before exiting the Xilinx ISE program, take the following two steps:
  - Close the simulation window
  - Project → Cleanup Project Files…
- There is an issue where the log file becomes abnormally large in certain situations. In this case, the log file runs out of disk space and cannot use the computer normally.



Sequential logic

Sequential logic (1)

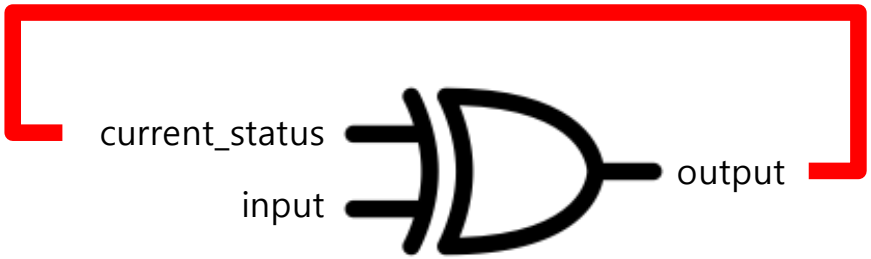
- Output is determined by both of **current state** and **input**
- To save current state, **feedback** is used to implement storage

Example > sequential logic

If **input == 0** then **hold current status**, else **if input == 1** then **toggle current status.**
Output is same as current status.

current_status	input	output
0	0	0
0	1	1
1	0	1
1	1	0

Sequential logic (2)

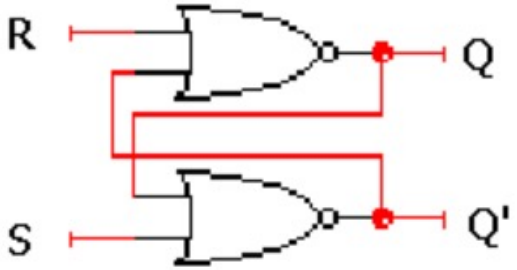


Taxonomy …

- Never mind, always work
  ➔ Latch
- Work only when it is enabled
  ➔ Gated latch
- Work only when it is edge triggered
  ➔ Flip-flop

R-S Latch

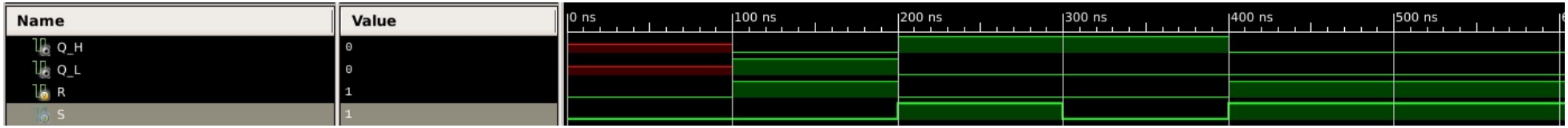
- R-S latch is a **1 bit memory** with cross-coupled gates.



S	R	Q
0	0	hold
0	1	0
1	0	1
1	1	unstable

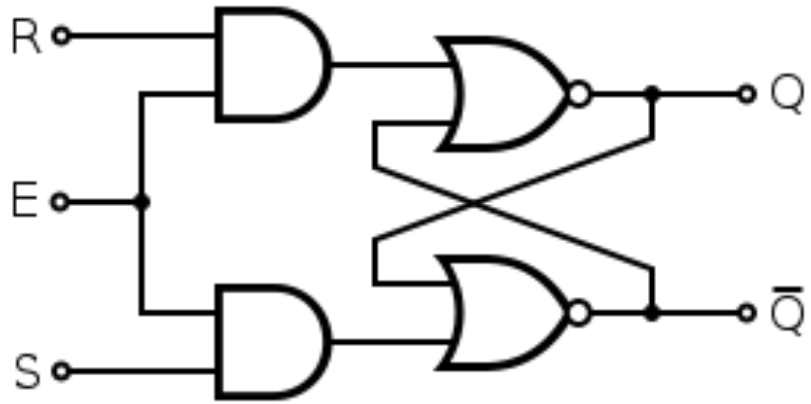
S	R	Q(t)	Q(t+Δ)	
0	0	0	0	hold
0	0	1	1	
0	1	0	0	reset
0	1	1	0	
1	0	0	1	set
1	0	1	1	
1	1	0	X	not allowed
1	1	1	X	

Q \ RS	00	01	11	10
0		1	X	
1	1	1	X	



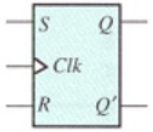
Gated R-S Latch

- R and S(inputs) matter only when E(enable) = 1
- Otherwise, hold current state



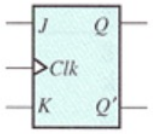
Flip-Flops

SR



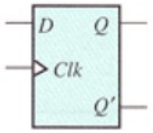
S	R	Q(next)
0	0	Q
0	1	0
1	0	1
1	1	NA

JK



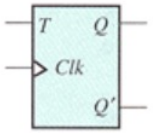
J	K	Q(next)
0	0	Q
0	1	0
1	0	1
1	1	Q′

D



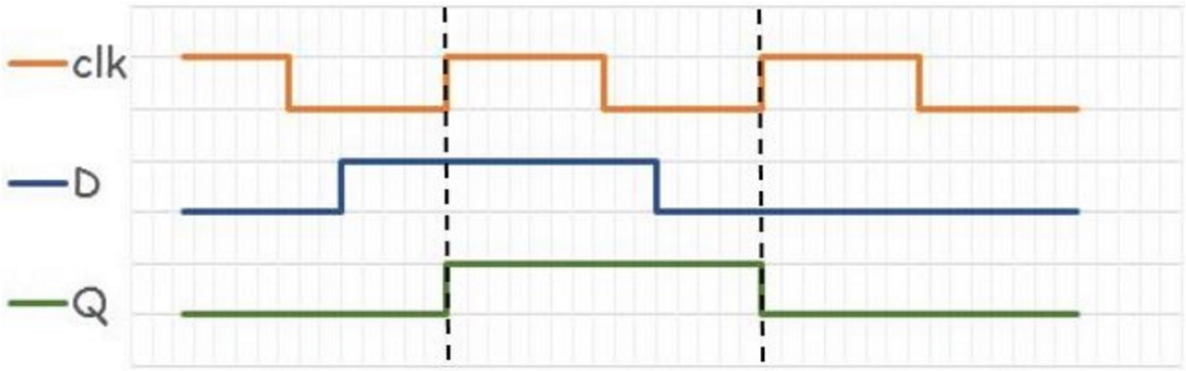
D	Q(next)
0	0
1	1

T



T	Q(next)
0	Q
1	Q′

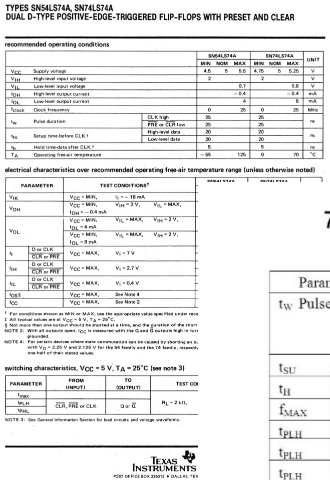
D FlipFlop



Clock

Clock

- Provide **timing** to sequential logic (ex. Flip-Flop)



74LS74 Data

Parameter			
t_W Pulse Width - Clock High			
- Preset Low			
- Clear Low			
t_{SU} Setup Time	20		ns
t_H Hold Time	0		ns
f_{MAX} Max Clock Frequency	20		MHz
t_{PLH} Prop Delay, Clock-to-Q		35	ns
t_{PLH} Prop Delay, Preset-to-Q		35	ns
t_{PLH} Prop Delay, Clear-to-Q		35	ns

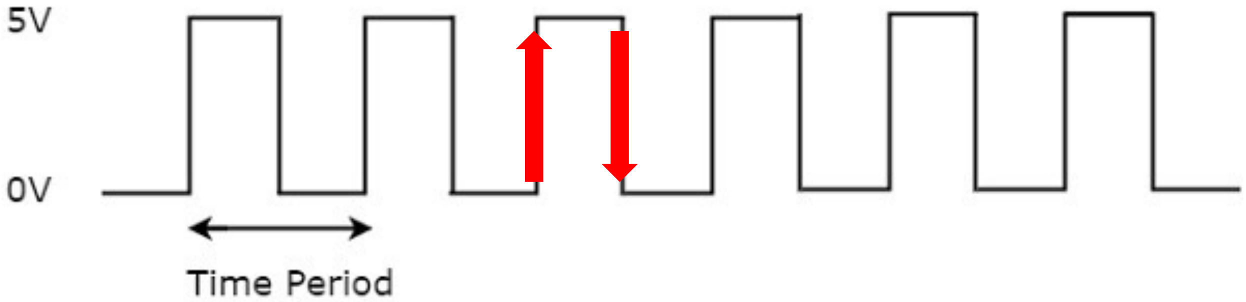
CEG 360/560 - EE 451/651 Section I - 74

Absolute Maximum Ratings — EZYTrigger Type

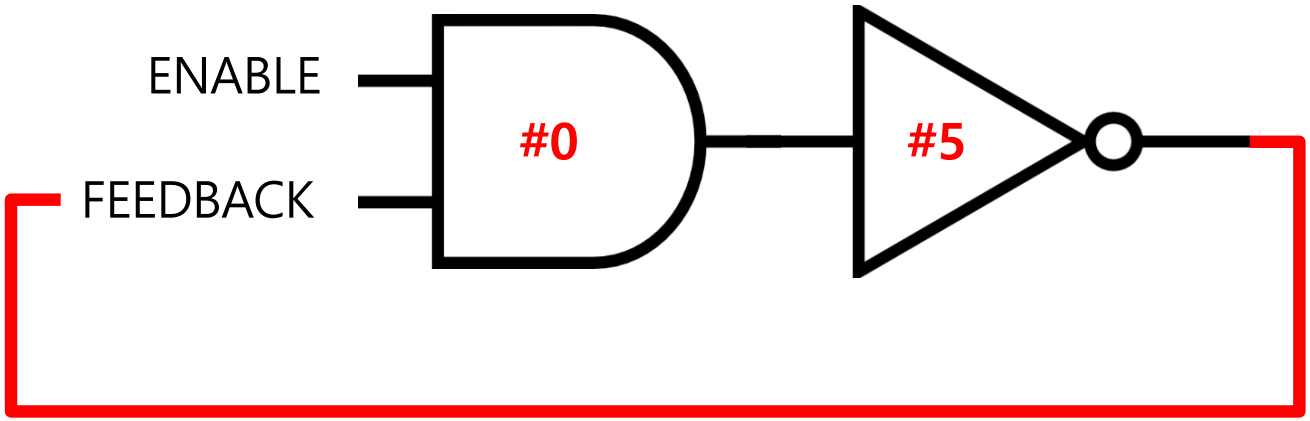
Parameter	Symbol	AT416 – 40	AT416 – 80
Peak voltage – positive and negative	Vp	4000 V	8000 V
Nominal mains voltage	Vm	1250 V	2500 V
Continuous DC voltage	V=	2500 V	2500 V
Thyristor turn-on time ($t_{gate-delay}$ + tr)	ton	6 µs	6 µs
Anode-Cathode transient immunity	(dv/dt)c	5000 V/µs	
Ambient temperature range	Ta	-20°C to +85°C	

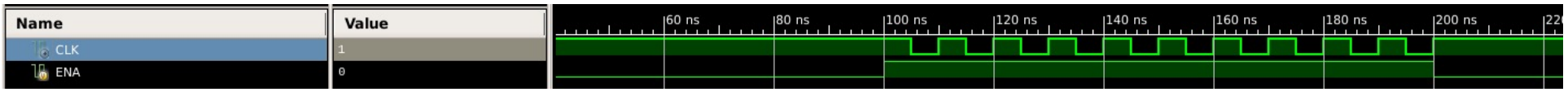
Technical Data at 25°C

500 mA Gate current threshold	Vgtl	40 V	40 V
2.5 A Gate current threshold	Vgth	90 V	140 V
Gate current rise time ⇨ Anode voltage ⇨ 800V	(di/dt)g	1.2 A/µs	1.2 A/µs
Peak gate current	Ip	2.5 A	2.5 A
Anode-cathode current at Vp and Ig = 0	In	4 mA	4.6 mA
Maximum off-state gate current	Io	2 µA	2 µA
Minimum control current (SFH756 Transm./ 1m fibre)	Icm	5 mA	5 mA
Recommended control current (SFH756 Transm./ 1m fibre)	Ic	10 mA	10 mA
Control input voltage drop at 10mA	Vin	Typ 1.2 < 1.5V	Typ 1.2 < 1.5V
Maximum reverse control input voltage	Vinr	6 V	6 V
Turn-on delay time at $I_{control}$ = 10mA	tdi	7 µs	7 µs



Simple Oscillator





How to implement gate delay ?

Example >

```
wire tmp;
assign #5 tmp = tmp & 1;
```

Homework

Homework

1. Implement the following in Verilog and simulate the behavior.
   (1) a R-S latch
   (2) a gated R-S latch using (1)
   (3) a Simple Oscillator(the clock period is free)
   (4) a R-S Flip-Flop(Edge-triggered) using above modules

   Include Source codes(modules) and simulation result.
   Explain that the modules you implement work well.
   No need to attach testbench code.

2. (Optional) Explain the different Flipflops(SR, D, JK, etc.) and how they differ from each other.

Report

- Write a report
  - Either in Korean or in English
  - Your report should include
    - discussion
    - Homework (if there is any)
  - # of pages doesn't matter
  - Documents should be submitted as PDF file(**less than 25Mb**)
  - **Attach source code and waveform screenshot**
  - Due :
    Class 001 - May, 2th (Before class begin at 7:00pm)
    Class 002 - May, 3th (Before class begin at 7:00pm)
    Class 003 - May, 4th (Before class begin at 7:00pm)