# EXPERIMENT NO.: - 4(A)

**AIM:** To Design Half-subtractor.

**THEORY:**

A combination circuit that performs the arithmetic subtraction of two bits is called half subtractor. In figure we assigns two symbols a and b are two input variables and D (difference) and B (borrow) are two output variables. The truth table for half subtractor is shown in figure.

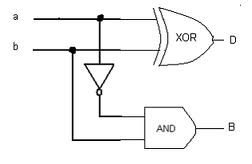
D = a’b + ab’

= a ⊕ b

B = ab’

The half subtractor consists of an X-OR gate and AND gate.

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | D | B |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |



**EQUIPMENTS REQUIRED:**

-Trainer kit

**COMPONENTS REQUIRED:**

* Connecting wires
* IC 7408 (AND gate)
* IC 7486 (X-OR gate)
* IC 7432 (OR gate)

**PROCEDURE**

1. Join the circuit as per circuit diagram.
2. Verify the truth-table.

**OBSERVATIONS:**

**CONCLUSION:**

# EXPERIMENT NO.: - 4(B)

**AIM:** To design Full-subtractor.

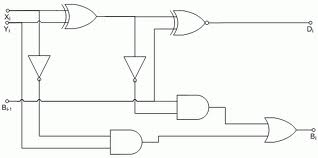
**THEORY:**

A combination circuit that performs the arithmetic subtraction of three bits is called full subtractor. In figure we assigns three symbols X, Y and Z are three input variables and D (difference) and B(borrow) are two output variables. The truth table for full subtractor is shown in figure.

D = x ⊕ y ⊕ z

B = x’y + x’z + yz

The full subtractor consists of two half-subtractor and one OR gate.

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|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Input | | | Output | |
| X | Y | Bi+1 | Borrow ( Bi ) | Diffe ( D ) |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**EQUIPMENTS REQUIRED:**

-Trainer kit

**COMPONENTS REQUIRED:**

* Connecting wires
* IC 7408 (AND gate)
* IC 7486 (X-OR gate)
* IC 7432 (OR gate)

**PROCEDURE:**

1. Join the circuit as per circuit diagram.
2. Verify the truth table for full-subtractor.

**OBSERVATION:**

**CONCLUSION:**