

# **CTL, VIS & Verilog – 1. aud vježba**

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**<http://www.fer.hr>**

- **CTL sintaksa (definicija i zadaci)**
- **CTL semantika (definicija i zadaci)**
- **Traffic light controller**
  - Primjer pretvorbe verilog koda u konačni automat
- **Pretvorba Verilog modela u Kripke strukturu**
- **Pretvorba Kripke strukture u Verilog model**

- Sintaksa i sematika (razlika)
- BNF

$$\phi ::= \perp \mid T \mid p \mid (\neg \phi) \mid (\phi \wedge \phi) \mid (\phi \vee \phi) \mid (\phi \rightarrow \phi) \mid AX\phi \mid EX\phi \mid \\ A(\phi U \phi) \mid E(\phi U \phi) \mid AG\phi \mid EG\phi \mid AF\phi \mid EF\phi$$

- $p, T, \perp$  – atom propozicija
- $\emptyset$  - formula u CTL-u
- ukoliko se uklone zagrade: prioritet –  
(negacija, AG, EG, AF, EF, AX, EX), konjukcija, disjunkcija,  
(implikacija, AU, EU)

- Izgradi sintaksno stablo za formule
  - $E(A(p1 \cup p2) \cup p3)$
  - $AG(p \rightarrow A(p \cup (\neg p \wedge A(\neg p \cup q))))$
  - $EF EG p \rightarrow AF r$
  - $A(p \cup EF r)$
  - $AG(q \rightarrow EG r)$

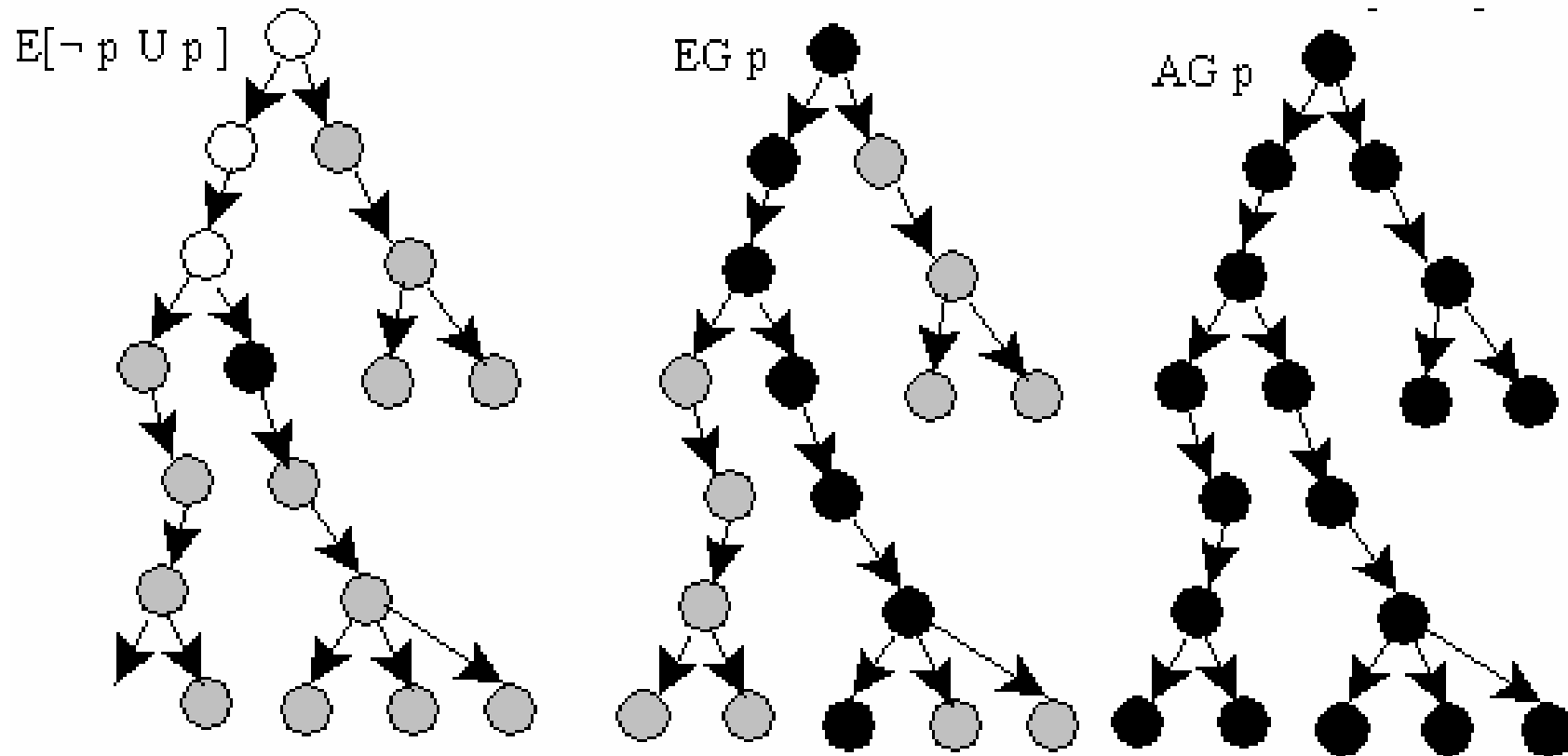
- Kripke struktura:

$$M = (S, \rightarrow, L)$$

$$\rightarrow \subseteq S \times S$$

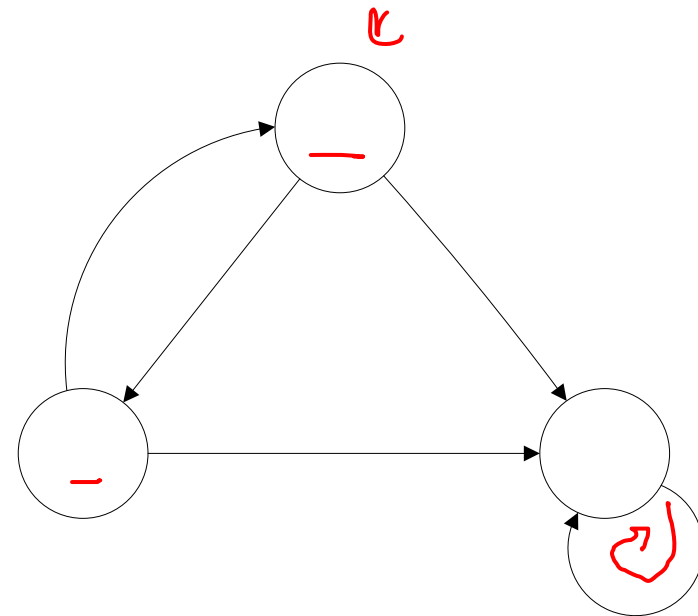
$$L: S \rightarrow P(Atoms)$$

- $M, s \models \Phi$

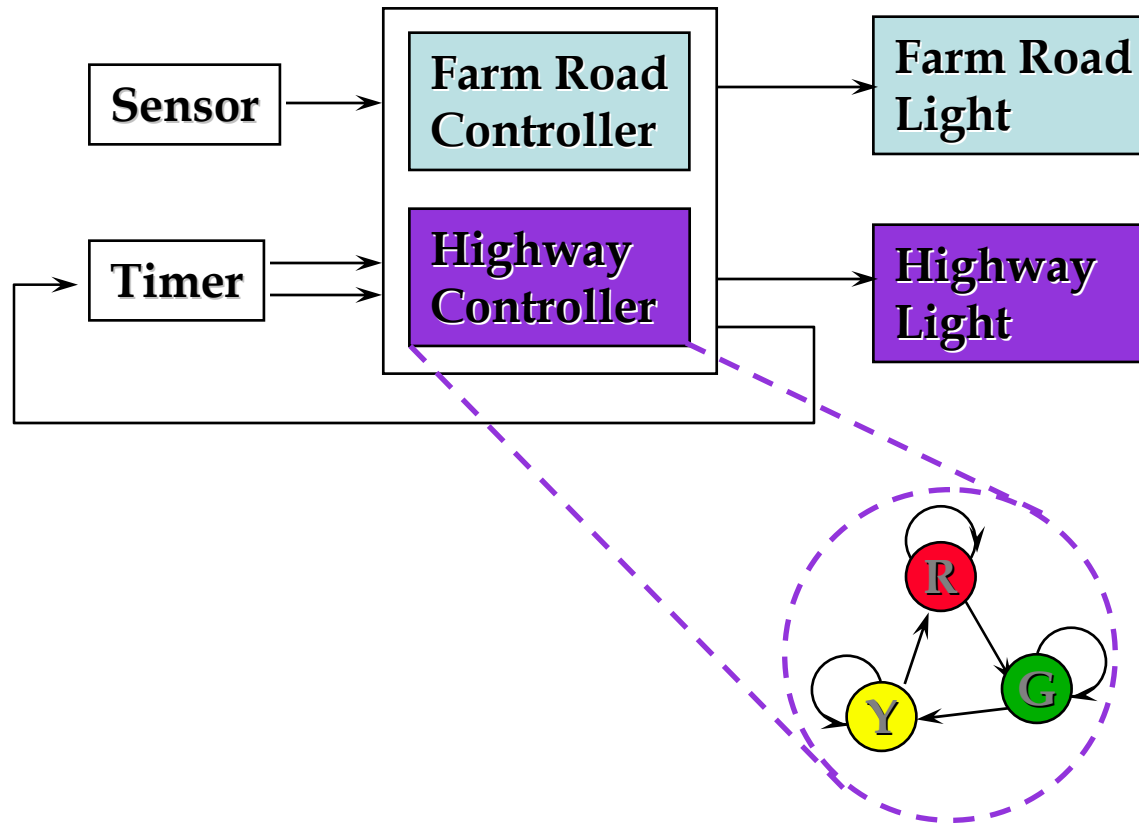


- Odredi istinite formule za model sa slike

- $M, s_0 \models (p \wedge q)$  ✓
- $M, s_0 \models \neg r$  ✓
- $M, s_0 \models T$  ✓
- $M, s_0 \models \underline{EX}(q \wedge r)$  ✓
- $M, s_0 \models \neg \underline{AX}(q \wedge r)$  ✓
- $M, s_0 \models \underline{EF}(p \wedge r)$  ✗
- $M, s_2 \models \underline{EG}(r)$  ✓
- $M, s_2 \models \neg \underline{AG}(r)$  ✗
- $M, s_0 \models \underline{AF}(r)$  ✓
- $M, s_0 \models E((p \wedge q) \cup r)$  ✓
- $M, s_0 \models \underline{A}(p \cup r)$  ✓



# Traffic light controller





# Traffic light controller – pretvorba Verilog to FSM



```
module timer(clk, start, short, long);
```

```
input clk;  
input start;  
output short;  
output long;
```

```
wire rand_choice;  
wire start, short, long;  
timer_state reg state;
```

```
initial state = START;
```

```
assign rand_choice = $ND(0,1);
```

```
assign short = ((state == SHORT) || (state == LONG));  
assign long = (state == LONG);
```

```
always @(posedge clk) begin
```

```
if (start) state = START;  
else
```

```
begin
```

```
case (state)
```

```
START:
```

```
if (rand_choice == 1) state = SHORT;
```

```
SHORT:
```

```
if (rand_choice == 1) state = LONG;
```

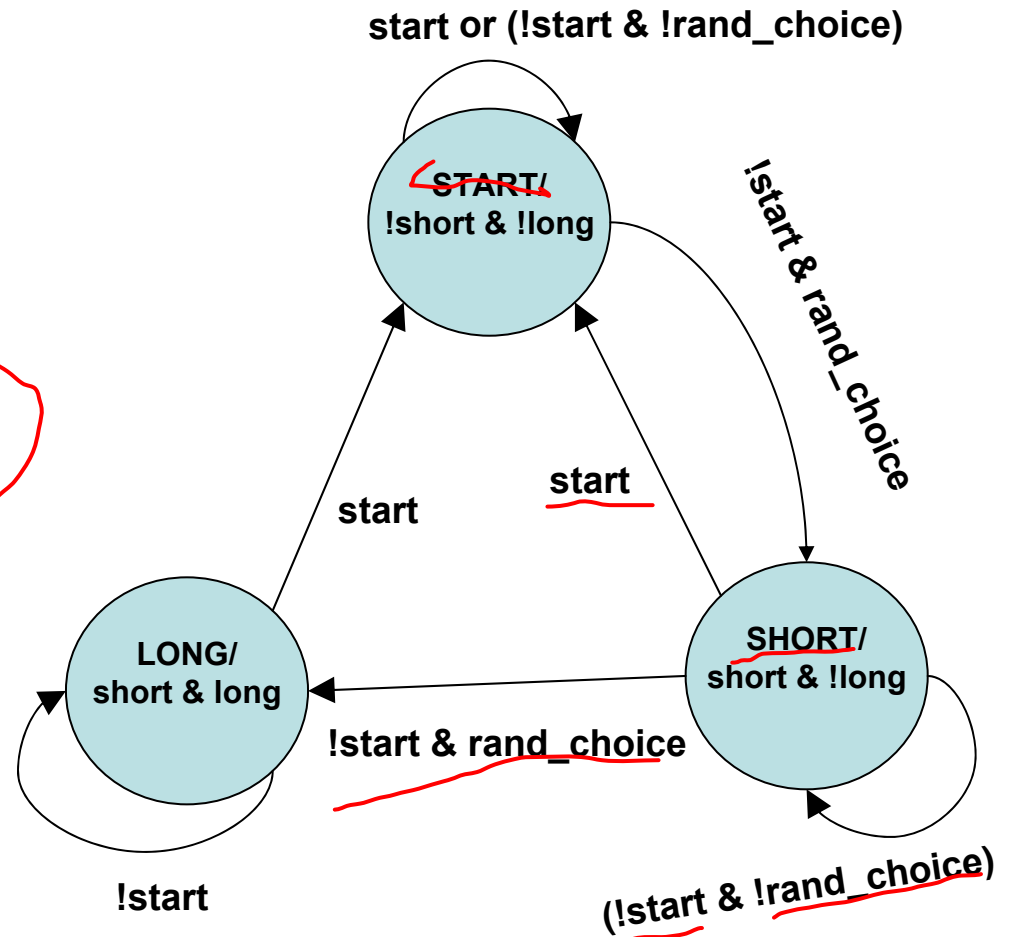
```
/* if LONG, remains LONG until start signal received */
```

```
endcase
```

```
end
```

```
end
```

```
endmodule
```



# Pretvorba Verilog modela u Kripke strukturu



- Za dva zadana odsječka Verilog koda:

```
module main(clk);
input clk;
reg a;
wire b;
    initial a=0;
    assign b = $ND(0,1);
    always @(posedge clk) begin
        a=b;
    end
endmodule
```

```
module main(clk);
reg a;
input clk;
    initial a=0;
    always @(posedge clk) begin
        a=!a;
    end
endmodule
```

odredi istinitost slijedećih CTL specifikacija: AG(a=0); EF(a=0);  
EG (a=0); AG(AF(a=0)).

Obrazloži odgovor.

- **Potrebno je izgraditi jedan Verilog modul koji zadovoljava slijedeće CTL specifikacije:**

- $AG(p \rightarrow EX(EG(q)))$
- $AG(q \rightarrow EX(EG(p)))$
- $AG((p \wedge \neg q) \vee (\neg p \wedge q))$

**Zadovoljava li izgrađeni modul specifikaciju  $AF(p)$**

- **Potrebno je izgraditi jedan Verilog modul koji zadovoljava slijedeće CTL specifikacije:**

- $AG(p \rightarrow EX(q))$
- $AG(q \rightarrow EX(EG(r)))$

**Zadovoljava li izgrađeni modul specifikaciju  $AG(p \rightarrow EF(r))$**