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Multi-gate SOI MOSFETs

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Abstract

This paper describes the evolution of the SOI MOSFET from single-gate structures to multigate (double-gate, trigate, Π-gate, Ω-gate and gate-all-around) structures. Increasing the "effective number of gates" improves the electrostatic control of the channel by the gate and, hence, reduces short-channel effects. Due to the very small dimensions of the devices, one-and two-dimensional confinement effects are observed, which results in the need of developing quantum modeling tools for accurate prediction of the electrical characteristics of the devices.

Keywords: FinFET; MuGFET; trigate FET; SOI; double-gate FET; GAA

1. Introduction

In a continuous effort to increase current drive and better control short-channel effects, silicon-on-insulator MOS transistors have evolved from classical, planar, single-gate devices into three-dimensional devices with a multi-gate structure (double-, triple- or quadruple- gate devices). It is worth noting that, in most cases, the term "double gate" refers to a single gate electrode that is present on two opposite sides of the device. Similarly, the term "triple gate" is used for a single gate electrode that is folded over three sides of the transistor.

2. Electrostatic integrity

Short-channel effects arise when control of the channel region by the gate is affected by electric field lines from source and drain.

In a bulk device (Fig. 1.A), the electric field lines propagate through the depletion regions associated with the junctions. Their influence on the channel can be reduced by increasing the doping concentration in the channel region. In very small devices, the doping concentration becomes too high (10^{19} cm^{-3}) for proper device operation, unfortunately.

In a fully depleted SOI (FDSOI) device, most of the field lines propagate through the buried oxide (BOX) before reaching the channel region (Fig. 1.B). Short-channel effects can be reduced in FDSOI MOSFETs by using a thin buried oxide and an underlying ground plane. This approach, however,

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has the inconvenience of increased junction capacitance and body effect [1].

A much more efficient device configuration is obtained by using the double-gate transistor structure. The electric field lines from source and drain underneath the device terminate on the bottom gate electrode and cannot, therefore, reach the channel region (Fig. 1.C).

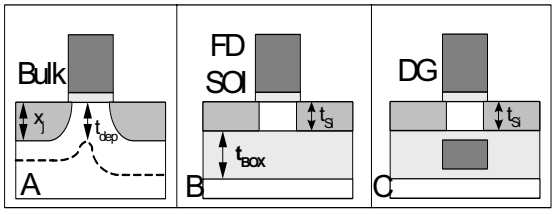

Fig. 1. Electrostatic Integrity in A: bulk, B: fully depleted SOI, and C: double-gate MOSFETs.

There is a parameter called the "Electrostatic Integrity" (*EI*) that can be related to the Drain-Induced Barrier Lowering (DIBL) and the threshold voltage roll-off Short-Channel Effect (SCE), and which describes how well the gate controls the channel region electrostatically [2]:

$$DIBL = 0.80\frac{\varepsilon_{Si}}{\varepsilon_{ox}} EI\, V_{DS} \quad \text{and} \quad SCE = 0.64\frac{\varepsilon_{Si}}{\varepsilon_{ox}} EI\, V_{bi} \qquad (1)$$

where V_{bi} is the source or drain built-in potential. The values for *EI* in a bulk, FDSOI and double-gate device are shown in Table 1.

Table 1.

Electrostatic Integrities corresponding to Fig. 1

A: Bulk	$EI = \left[1+\frac{x_j^2}{L_{el}^2}\right]\frac{t_{ox}}{L_{el}}\frac{t_{dep}}{L_{el}}$
B: FDSOI	$EI = \left[1+\frac{t_{Si}^2}{L_{el}^2}\right]\frac{t_{ox}}{L_{el}}\frac{t_{Si}+\lambda t_{BOX}}{L_{el}}$
C: Double Gate	$EI = \frac{1}{2}\left[1+\frac{t_{Si}^2/4}{L_{el}^2}\right]\frac{t_{ox}}{L_{el}}\frac{t_{Si}/2}{L_{el}}$

Based on short-channel and DIBL considerations, the minimum gate length that can be used with the different technologies has been calculated. The result of these calculations is shown in Fig. 2 for three different types of CMOS circuits: high-performance (HP), low operating power (LOP), and low standby power (LSTP) digital circuits. An important conclusion can be derived from the data presented in Fig. 2: bulk transistors run out of steam once they reach a gate length of 15-20 nm. FDSOI can be used until 10 nm, but smaller gate lengths can be only achieved by the double-gate structure.

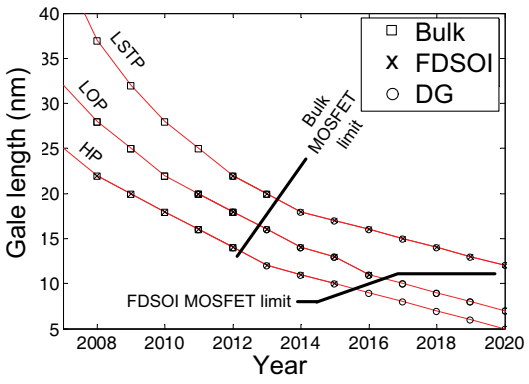

Fig. 2. Evolution of gate length predicted by the 2005 ITRS for high-performance (HP), low operating power (LOP), and low standby power (LSTP) digital circuits.

3. History of multi-gate MOSFETs

Figure 3 shows the "Family Tree" of SOI MOSFETs and shows the evolution from partially depleted, single-gate devices to multi-gate, fully depleted structures.

The first article on the double-gate MOS (DGMOS) transistor was published by T. Sekigawa and Y. Hayashi 1984 [3]. That paper shows that one can obtain significant reduction of short-channel effects by sandwiching a fully depleted SOI device between two gate electrodes connected together. The device was called XMOS because its cross section looks like the Greek letter Ξ (*Xi*). Using this configuration, a better control of the channel depletion region is obtained than in a "regular" SOI MOSFET, and, in particular, the influence of the drain electric field on the channel is reduced, which reduces short-channel [4]. The first fabricated double-gate SOI MOSFET was the "fully DEpleted Lean-channel TrAnsistor (DELTA, 1989)", where the device is made in a tall and narrow silicon island called "finger", "leg" or "fin".

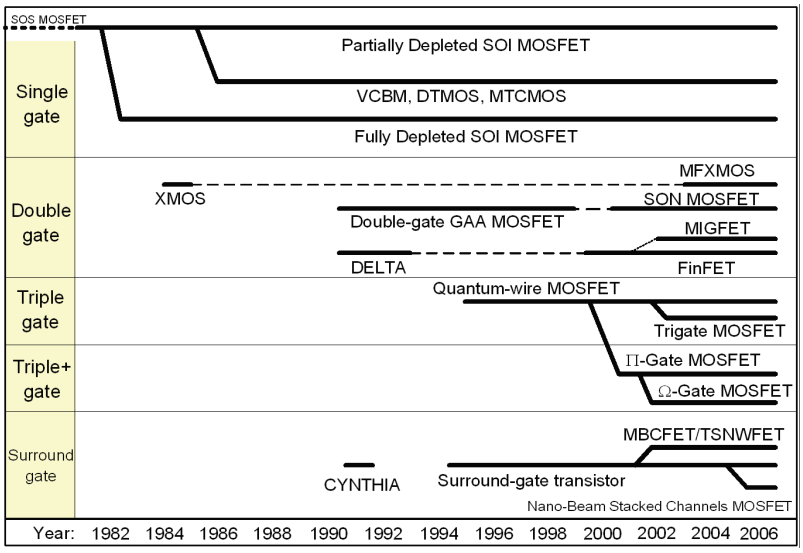

Fig. 3. "Family tree" of SOI and multigate MOSFETs

The FinFET structure is similar to DELTA, except for the presence of a dielectric layer called the "hard mask" on top of the silicon fin. The hard mask is used to prevent the formation of parasitic inversion channels at the top corners of the device.

Other implementations of vertical-channel, double-gate SOI MOSFETs include the "Gate-All-Around device" (GAA), which is a planar MOSFET with the gate electrode wrapped around the channel region [5,6], the Silicon-on-Nothing) MOSFET [7-9], the Multi-Fin XMOS (MFXMOS) [10], the triangular-wire SOI MOSFET [11] and the Δ-channel SOI MOSFET [12].

The triple-gate MOSFET is a thin-film, narrow silicon island with a gate on three of its sides [13]. Implementations include the quantum-wire SOI MOSFET [14,15] and the tri-gate MOSFET [16,17]. The Electrostatic Integrity of triple-gate MOSFETs can be improved by extending the sidewall portions of the gate electrode to some depth in the buried oxide and underneath the channel region (Π-gate device [18,19] and Ω-gate device [20-22]). From an electrostatic point of view, the Π-gate and Ω-gate MOSFETs have an effective number of gates between three and four. The use of strained silicon, a metal gate and/or high-k dielectric as gate insulator can further enhance the current drive of the device [23-25].

The structure that theoretically offers the best possible control of the channel region by the gate, and hence the best possible Electrostatic Integrity is the surrounding-gate MOSFET The first surrounding-gate MOSFETs were fabricated by wrapping a gate electrode around a vertical silicon pillar. Such devices include the CYNTHIA device (circular-section device) [26,27] and the pillar surrounding-gate MOSFET (square-section device) [28]. More recently, planar surrounding-gate devices with square or circular cross sections have reported [29,30]. Surrounding-gate SOI MOSFETs with a gate length as small as 5 nm have shown to be fully functional [31]. To increase the current drive per unit area, multiple surrounding-gate channels can be stacked on top of one another, while sharing common gate, source and drain. Such devices are called the Multi-Bridge Channel MOSFET (MBCFET) [32,33], the Twin-Silicon-Nanowire MOSFET (TSNWFET) [34], or the Nano-Beam Stacked Channels (GAA) MOSFET [35]. Schematic cross sections corresponding to the different gate structures described in the previous sections are shown in Fig 4.

4. Natural length

The concept of "*natural length*" can be derived from Poisson's equation. The natural length of a device basically represents the length of the region of

the channel that is controlled by the drain. It is related to the Electrostatic Integrity. A device is free of short-channel effects if the effective gate length of a MOS device is larger than 5 to 10 times the natural length [36]. Table 2 shows the natural length for different gate configurations.

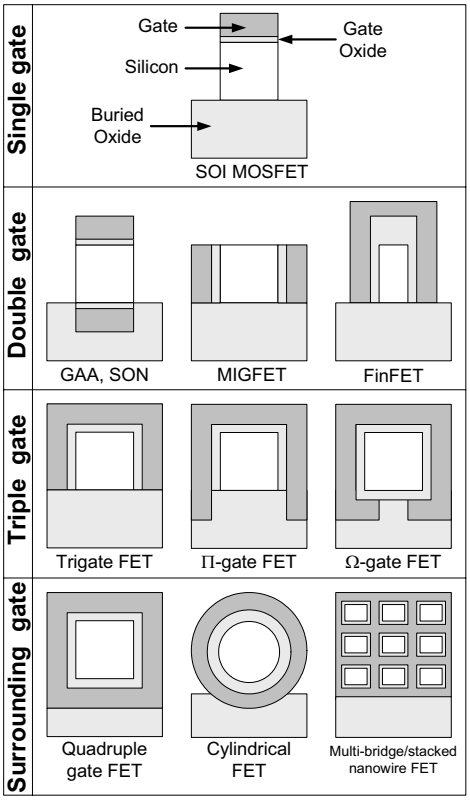

Fig. 4. Different gate structures.

The following observations can be made: the natural length (and hence short-channel effects) can be reduced by decreasing the gate oxide thickness, the silicon film thickness and by using a high-k gate dielectric instead of SiO_2. In addition, the natural length is reduced when the number of gates is increased. In very small devices, the reduction of oxide thickness below 1.5 nm causes gate tunneling current problems. Using multi-gate devices, it is possible to trade a thin gate oxide for thin silicon film/fin thinning since λ is proportional to the product $t_{si} \times t_{ox}$. The "*equivalent number of gates*" (*ENG*) is basically equal to the number of gates (a square cross section is assumed) but is also equal to the number that divides $\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{si} t_{ox}$ in the equations defining the natural length, λ. [37] Thus we have *ENG*=1 for a single-gate FDSOI MOSFET, *ENG*=2 for a double-gate device and *ENG*=4 for a quadruple-gate MOSFET. *ENG*=3 for a triple-gate device and, by some strange coincidence, *ENG* is close to π in a Π-gate device. In the Ω-gate device the value of *ENG* ranges between 3 and 4 depending on the extension of the gate under the fin.

Table 2.

Natural length in devices with different geometries

Single gate	$\lambda_1 = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{si} t_{ox}}$
Double gate	$\lambda_2 = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}} t_{si} t_{ox}}$
Quadruple gate (square section)	$\lambda_4 \cong \sqrt{\frac{\varepsilon_{si}}{4\varepsilon_{ox}} t_{si} t_{ox}}$
Surrounding gate (circular section)	$\lambda_o = \sqrt{\frac{2\varepsilon_{si} t_{si}^2 \ln\left(1 + \frac{2t_{ox}}{t_{si}}\right) + \varepsilon_{ox} t_{si}^2}{16\varepsilon_{ox}}}$

5. Current drive

In a multigate FET the current drive is essentially equal to the sum of the currents flowing along all the interfaces covered by the gate electrode. It is, therefore, equal to the current in a single-gate device multiplied by the equivalent number of gates (a square cross section is assumed) if carriers have the same mobility at each interfaces. To drive large currents multi-fin devices are used. The current drive of a multi-fin MOSFET is equal to the current of an individual fin multiplied by the number of fins. Considering a pitch P for the fins, the current in a multigate device is given by:

$$I_D = I_{Do} \frac{\theta \mu_{top} W_{si} + 2\mu_{side} t_{si}}{\mu_{top} P} \quad (2)$$

where I_{Do} is the current in the single-gate, planar device occupying the same area as the multi-fin device (Fig. 5), W_{si} is the width of each individual fin, t_{si} is the silicon film thickness; $\theta=1$ in a triple-gate device where conduction occurs long three interfaces, and $\theta=0$ in a FinFET where channels are formed at the sidewall interfaces only [38].

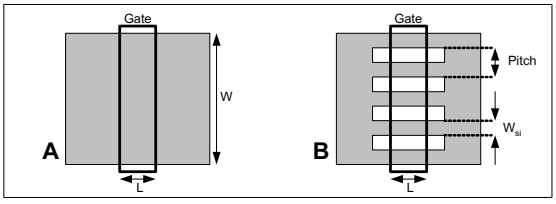

Fig. 5. A: Single-gate, planar MOSFET layout; B: Multi-fin multigate FET layout.

A multigate device can deliver significantly more current that single-gate planar MOSFET, provided a small enough fin pitch can be achieved. The current drive can be increased by increasing the fin height, t_{si}, but the use of tall fins often raises difficulties during device processing. It is worth noting that gate capacitance increases with the Effective Number of Gates (*ENG*). As a result, the gate delay C_gV_{DD}/I_{ON} does not improve when the *ENG* is increased. On the contrary, the delay increases with the ENG and is, therefore, larger in GAA than in trigate devices and larger in double-gate FETs than in single-gate devices [39].

6. Low-dimensional quantum effects

The thickness and/or width of multi-gate FETs is reaching values that are less than 10 nanometers. Under these conditions the electrons in the "channel" (if we take the example of an n-channel device) form either a two-Dimensional Electron Gas (2DEG) if we consider a double-gate device or a one-Dimensional Electron Gas (1DEG) if we consider a triple or quadruple-gate MOSFET. This confinement is at the origin of the "volume inversion" effect [40] and yields an increase of threshold voltage when the width/thickness of the devices is reduced [41,42].

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