PIC12F629/675 INSTRUCTIONS

Mnemonic, operands		Description	Status	!
BYTE-ORIENTED FILE REGISTER OPERATIONS				
ADDWF	f, d	Add W and f	C,DC,Z	1,2
ANDWF	f, d	AND W with f	Z	1,2
CLRF	f	Clear f	Z	2
CLRW	-	Clear W	Z	
COMF	f, d	Complement f	Z	1,2
DECF	f, d	Decrement f	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0		1,2
INCF	f, d	Increment f	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0		1,2
IORWF	f, d	Inclusive OR W with f	Z	1,2
MOVF	f, d	Move f	Z	1,2
MOVWF	f	Move W to f		
NOP	-	No Operation		
RLF	f, d	Rotate Left f through Carry	C	1,2
RRF	f, d	Rotate Right f through Carry	C	1,2
SUBWF	f, d	Subtract W from f	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f		1,2
XORWF	f, d	Exclusive OR W with f	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS				
BCF	f, b	Bit Clear f		1,2
BSF	f, b	Bit Set f		1,2
BTFSC	f, b	Bit Test f, Skip if Clear		
BTFSS	f, b	Bit Test f, Skip if Set		
LITERAL AND CONTROL OPERATIONS				
ADDLW	k	Add literal and W	C,DC,Z	
ANDLW	k	AND literal with W	Z	
CALL	k	Call subroutine		
CLRWDT	-	Clear Watchdog Timer	/TO,/PD	
GOTO	k	Go to address		
IORLW	k	Inclusive OR literal with W	Z	
MOVLW	k	Move literal to W		
RETFIE	-	Return from interrupt		
RETLW	k	Return with literal in W		
RETURN	-	Return from Subroutine		
SLEEP	-	Go into Standby mode	/TO,/PD	
SUBLW	k	Subtract W from literal	C,DC,Z	
XORLW	k	Exclusive OR literal with W	Z	

f: register file address (0x00 to 0x7F)
W: working register (accumulator)
b: bit address within an 8-bit file register
k: literal field, constant data or label
PC: program counter
PD: power-down bit
d: destination select;
d = 0: store result in W,
d = 1: store result in file register f.
Default is d = 1.
TO: time-out bit

1: When an I/O register is modified as a function of itself (e.g., MOVF GPIO, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

STATUS register (03h, 83h)

7	6	5	4	3	2	1	0
IRP	**RP1**	**RP0**	**/TO**	**/PD**	**Z**	**DC**	**C**
reserved		**R/W-0**	**R-1**	**R-1**	**R/W-x**	**R/W-x**	**R/W-x**

IRP	Reserved, should be maintained as '0'
RP1: RP0	**Register Bank Select** bits, RP1 must be maintained as '0' 00 = Bank 0 (00h - 7Fh) 01 = Bank 1 (80h - FFh)
/TO	**Time-out** bit 1 = After power-up, CLRWDT instruction, or SLEEP instruction 0 = A WDT time-out occurred
/PD	**Power-down** bit 1 = After power-up or by the CLRWDT instruction 0 = By execution of the SLEEP instruction
Z	**Zero** bit 1 = The result of an arithmetic or logic operation is zero 0 = The result of an arithmetic or logic operation is not zero
DC	**Digit carry/~borrow** bit (ADDWF, ADDLW, SUBLW, SUBWF) 1 = A carry-out from the 4th low order bit of the result occurred 0 = No carry-out from the 4th low order bit of the result
C	**Carry/~borrow** bit (ADDWF, ADDLW, SUBLW, SUBWF) 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred **Note:** For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source

DATA MEMORY MAP

	Indirect address		
00h	TMR0	OPTION_REG	80h
01h	PCL	PCL	81h
02h	STATUS	STATUS	82h
03h	FSR	FSR	83h
04h	GPIO	TRISIO	84h
…			…
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh	TMR1L	PCON	8Eh
0Fh	TMR1H		8Fh
10h	T1CON	OSCCAL	90h
…			…
15h		WPU	95h
16h		IOC	96h
…			…
19h	CMCON	VRCON	99h
1Ah		EEDATA	9Ah
1Bh		EEADR	9Bh
1Ch		EECON2*	9Ch
1Dh		EECON1	9Dh
1Eh	ADRESH	ADRESL	9Eh
1Fh	ADCON0	ANSEL	9Fh
20h	General purpose registers 64bytes	Accesses locations 20h-5Fh	A0h
…			…
5Fh			DFh
60h			E0h
7Fh			FFh

*: Not a physical register

OPTION register (81h)

7	6	5	4	3	2	1	0
/GPPU	**INTEDG**	**T0CS**	**T0SE**	**PSA**	**PS2**	**PS1**	**PS0**
R/W-1	**R/W-1**	**R/W-1**	**R/W-1**	**R/W-1**	**R/W-1**	**R/W-1**	**R/W-1**

/GPPU	**Pull-up Enable** bit 1 = GPIO pull-ups are disabled 0 = GPIO pull-ups are enabled by individual port latch values
INTEDG	**Interrupt Edge Select** bit 1 = Interrupt on rising edge of GP2/INT pin 0 = Interrupt on falling edge of GP2/INT pin
T0CS	**TMR0 Clock Source Select** bit 1 = Transition on GP2/T0CKI pin 0 = Internal instruction cycle clock (CLKOUT)
T0SE	**TMR0 Source Edge Select** bit 1 = Increment on high-to-low transition on GP2/T0CKI pin 0 = Increment on low-to-high transition on GP2/T0CKI pin
PSA	**Prescaler Assignment** bit 1 = Prescaler is assigned to the WDT 0 = Prescaler is assigned to the TIMER0 module
PS2:PS0	**Prescaler Rate Select** bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

R: readable bit
W: writable bit
U: unimplemented bit, read as '0'
-n: value at POR
'0': bit is cleared
'1': bit is set
x: bit is unknown

INTCON register (0Bh, 8Bh)

7	6	5	4	3	2	1	0
GIE	**PEIE**	**T0IE**	**INTE**	**GPIE**	**T0IF**	**INTF**	**GPIF**
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

GIE	**Global Interrupt Enable** bit 1 = Enables all unmasked interrupts 0 = Disables all interrupts
PEIE	**Peripheral Interrupt Enable** bit 1 = Enables all unmasked peripheral interrupts 0 = Disables all peripheral interrupts
T0IE	**TMR0 Overflow Interrupt Enable** bit 1 = Enables the TMR0 interrupt 0 = Disables the TMR0 interrupt
INTE	**GP2/INT External Interrupt Enable** bit 1 = Enables the GP2/INT external interrupt 0 = Disables the GP2/INT external interrupt
GPIE	**Port Change Interrupt Enable** bit[1] 1 = Enables the GPIO port change interrupt 0 = Disables the GPIO port change interrupt
T0IF	**TMR0 Overflow Interrupt Flag** bit[2] 1 = TMR0 register has overflowed (*) 0 = TMR0 register did not overflow
INTF	**GP2/INT External Interrupt Flag** bit 1 = The GP2/INT external interrupt occurred (*) 0 = The GP2/INT external interrupt did not occur
GPIF	**Port Change Interrupt Flag** bit 1 = When at least one of the GP5:GP0 pins changed state (*) 0 = None of the GP5:GP0 pins have changed state

***:** bits 0-2 (GPIF, INTF, T0IF) must be cleared in software before re-enabling interrupts
1: IOC register must also be enabled to enable an interrupt-on-change.
2: T0IF bit is set when TIMER0 rolls over. TIMER0 is unchanged on RESET and should be initialized before clearing T0IF bit.