

## **ADC's control**

The principle of operation of the 12 bits ADC and the 10 bits ADC is approximately the same. The parameters registers latches the parameters of a conversion. Those registers contains the conversion mode, sequential or single-channel conversion, the conversion sequence and the number of channel, in case of a sequential conversion, the conversion channel, in case of a single-channel conversion, and the number of conversion cycle. Depending on the chosen conversion mode, the FSM mode control module configure the ADC and recuperate the conversion result via the ADC configuration and ADC data recuperation modules. The ADC's output control the SPI interface of the two ADCs. The conversion result is latches in the conversion result register and an output report for one clock cycle that a conversion result is ready. For the 12 bits ADC, the conversion time is 19 clock cycles and for the 10 bits ADC, the conversion time is, at most, 40 clock cycles. The 12 bits ADC data is 16 bits of length and contain the conversion channel, a bit sign and the 12 bits conversion. The 10 bits ADC data is also 16 bits of length and contain a bit sign, the 10 bits conversion and 5 trailing zeros. The conversion channel is added manually by replacing the 3 last trailing zeros. For both the 12 bits ADC and the 10 bits ADC, the conversion data are in two's complement format.

## **Wave generation module**

The wave generation module allow the user to generate a square wave, a triangular wave, a sin wave and a pulsed triangular wave. This module can generate a wave at a frequency of 0.01 Hz to 10 kHz. The amplitude and the DC offset of the generated wave --insertword-- from 0 to 2 V and from -2.5 to 2.5 V, respectively. The wave is generated for a determined number of cycle. Furthermore, the duty cycle of the square wave can be set from 10% to 90%. Also, the pulse clock of the pulsed triangular wave is adjustable from the user interface and the frequency varies from 12.5 MHz to 381 Hz. The generated wave is 16 bits long in one's complement format. The parameters contained in the parameters registers are calculated and sent on the serial port for each wave depending on the user interface parameters. The FSM wave control module latches the parameters into the parameters registers and command the start of the wave generation depending on the wave choice from the user interface. Also, this module initiate the transfer of the 16 bits generated wave trough the DAC serial interface.

## **DAC control module**

The DAC control module command the serial interface of the 16 bits DAC. This interface consist of 3 signals: SCLK, DIN and FSYNC. SCLK is the serial clock, DIN is the data input and FSYNC is the word clock. The FSM DAC serial control module latches the input data into the 16 bits shift register and transfer the data MSB first trough the serial interface. 18 clock cycles are required, in total, to transfer a 16 bits data to the DAC.

## **Cyclic voltametry module**

This module allow the user to perform a cyclic voltametric experiment. The user interface display the current vs voltage curve or the current curve and the voltage curve separately, for each channel. Also, the user can choose the type of generated wave, the conversion channels, the conversion time and the type of display (real time or not). The parameters of the experiments are sent trough the serial port and latches in the parameters registers. The FSM serial control module manage the serial buffer and the latching of the parameters depending on the wave choice and the experiment parameters. Also, this module initiate the wave generation and the ADC's conversion after all the

parameters are received. In this case, the 10 bits ADC is measuring the voltage and the 12 bits ADC is measuring the current. The CLK management unit divide de 50 MHz clock for the other modules. 3 clocks are required for the cyclic voltametry module : 25 MHZ clock for wave generation module, 12.5 MHZ clock for the 12 bits ADC control module and 781.25 kHz clock for the 10 bits ADC control module. The frequency of the 10 bits ADC has to be lowered to allow sending the data directly trough the serial port. Also, because the ADC's conversion time are different, the 12 bits ADC had to operate at its maximum frequency. In fact, it minimize the gap between the current and the voltage measurement. In addition, the FSM serial control module send the conversion result trough the serial port each time a new data is latches from the 10 bits ADC control module to the conversion result register. A Matlab script retrieves the data and display the curve on the user interface.