

BME154L (Palmeri)

Spring 2012

Exam #2 Solutions

Instructions:

- Write your name at the top of each page.
- Show all work (this is *critical* for partial credit!), including block diagrams for all design problems!
- Remember to include units with all answers and label all plot axes.
- Clearly box all answers.
- Assume that all components are ideal unless otherwise stated.
- Assume that op amps rail at ± 12 V unless otherwise stated.

Abbreviations:

ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
MSB	Most Significant Bit
LSB	Least Significant Bit
RMS	Root Mean Square
SNR	Signal-to-Noise Ratio

In keeping with the Duke Community Standard, I have neither given nor received aid in completion of this examination.

Signature:_____

Problem #1 [70 points]

Another approach to half-wave rectification is to utilize the ADC/DAC process instead of diodes. We will work through this process in the following problem. Consider a sinusoidal signal $f(t) = 5 \sin(2000\pi t)$ V (Figure 1.1(a)) and a desired output signal (a half-wave rectified input signal) (Figure 1.1(b)):

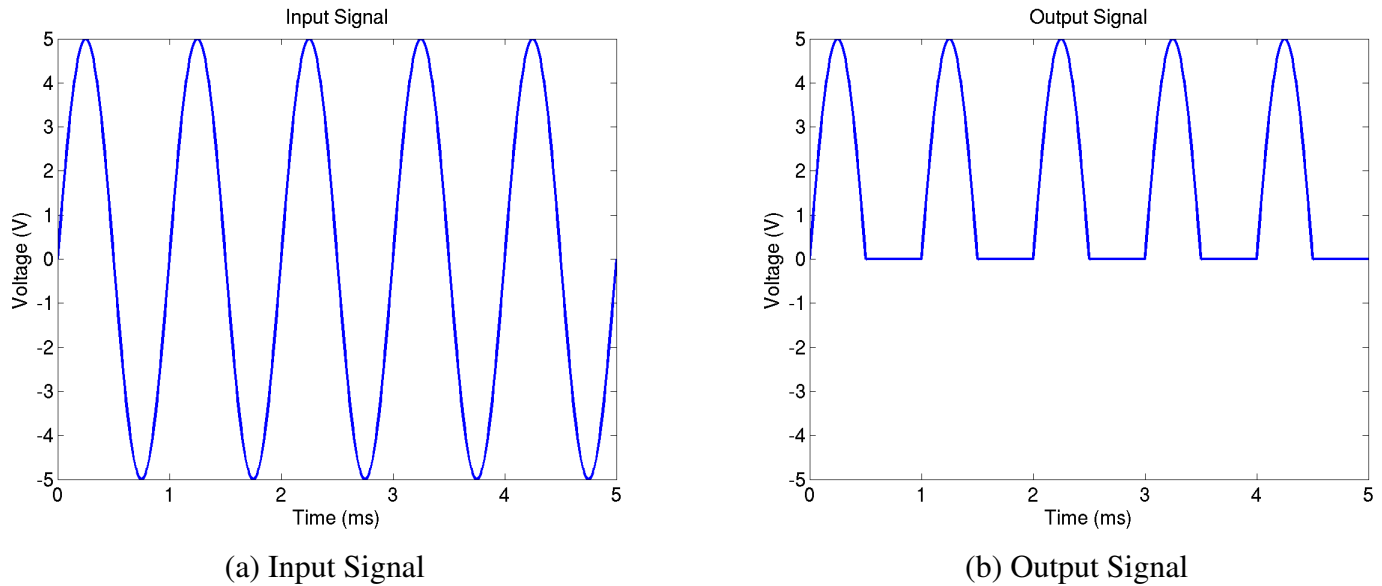


Figure 1.1: Input and Output Signals

We will use the following block diagram:

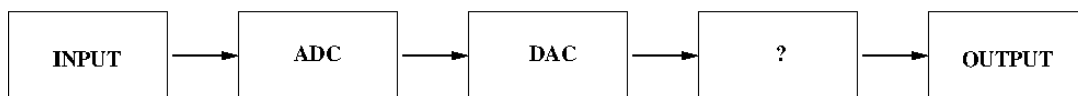


Figure 1.2: Block Diagram

- (a) Sketch the power spectra of input (Figure 1.1(a)) and output (Figure 1.1(b)) signals, labeling key features.¹ [10 points]

The input signal (continuous wave sinusoid) has a delta function at $f_o = 1000$ Hz, which the output signal has harmonics at multiples of f_o . These harmonics account for the sharper “notches” for the half-rectified sinusoid at $V = 0$. The way to figure this out involves recognizing that the half-wave rectified output is the continuous sinusoidal input multiplied by a rect that has been convolved with a comb. The rect convolved with a comb yields a sinc that has been multiplied by a set of delta functions in the frequency domain, which is then convolved with the delta function associated with the input sinusoid. You can plot this output power spectrum using Matlab.

- (b) Some sampling frequency considerations:

- What is the minimum sampling frequency of the ADC that you need to faithfully reproduce the input signal to the DAC? [5 points]

2000 Hz

- What is the minimum DAC update frequency that you need to faithfully reproduce the output signal? Consider your answer to (a) and if there is any benefit to updating your DAC output more frequently than the sampling frequency of the ADC? [5 points]

There is no additional information above 1000 Hz from the ADC process, so while the output signal has the harmonics ideally in it, having a DAC output updated more often won't help.

- (c) Given an RMS white noise voltage of 0.5 V (not shown in Figure 1.1(a)),

- What is the SNR of the input signal? [5 points]

$$SNR = 20 * \log_{10} \frac{Signal_{RMS}}{Noise_{RMS}}$$

- What is the ideal number of bits that should be used to sample the input signal to generate the desired output signal?²³ [5 points]

$$\frac{\frac{5V}{\sqrt{2}}}{0.5V} = 2 \text{ bits}$$

- (d) Design the fastest ADC possible for this process. Be sure to specify all relevant component values. [10 points]

Flash ADC

Make sure that node voltages at the comparators represent voltage from 0:5 V, in $\frac{5}{2^n - 1} = 1.33V$ increments. Resistors needed to be in the k Ω range.

- (e) Successive Approximation ADC

¹If you are having trouble sketching these power spectra, then describe your thought process for partial credit.

²“Ideal” means the number of bits needed to fully represent the signal without wasting bits sampling just noise.

³Hint: Saturation of an ADC can be considered a design flaw in some circuits, but it can be taken advantage of in this problem to remove parts of your input signal that you do not want in your output signal.

- If you were to use a successive approximation ADC for this problem, then how many approximations would be needed for each binary number representation? [5 points]

Number of approximations = number of bits (2)

- Write a general expression that relates the minimum frequency of these successive approximations to the sampling rate of the input signal such that there is no loss of frequency content of the input signal. [5 points]

n = number of bits

f_s = sampling rate

$$f_{min} = n \times f_s$$

- (f) Design an R-2R DAC for your circuit. Be sure to specify all component values. [10 points]

See lecture notes for general form of R-2R ladder. Make sure that the voltage source is set such that a max output voltage of 5 V is achieved, with 0 as a minimum output voltage. There are 2 “arms” to this DAC, which is equal to the number of bits.

- (g) What error would be introduced into your DAC if the “2R” for your MSB was 20% greater than your ideal design? (Provide a quantitative answer.) [5 points]

MSB and LSB are both affected since the current division has been skewed. Full credit for circuit analysis showing the error on both branches.

- (h) Design the “?” block in Figure 1.2 to achieve the desired output signal (Figure 1.1(b)). [5 points]

Low pass filter with cutoff frequency greater than f_{max} of the desired output waveform.

Problem #2 [30 points]

Various physiologic systems in the body can be represented as second-order systems. Below is a voltage trace from a lab group measuring the output (impulse response) of the system you designed in Lab 8 with a finger tap (“delta-like”) input.

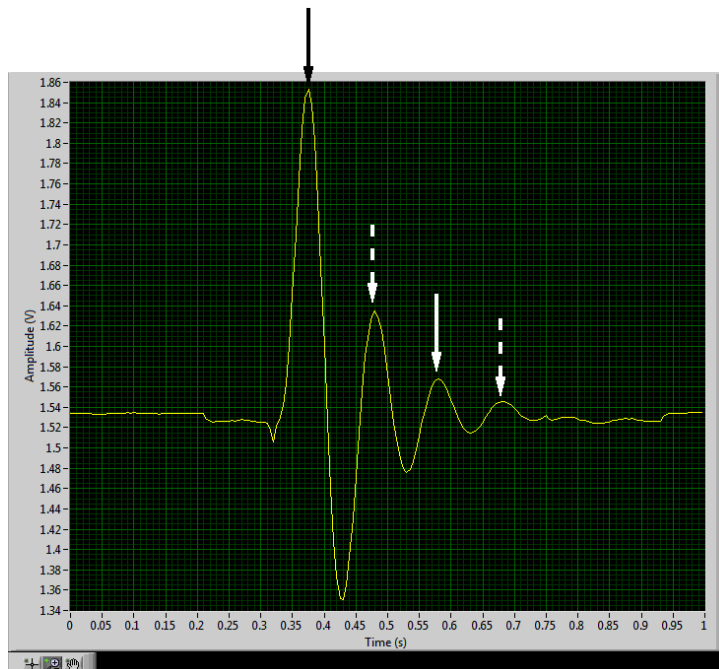


Figure 2.3: Second-Order System Impulse Response

- (a) The oscillations in Figure 2.3 occur at the damped frequency of this system (ω_d). Is ω_d greater than or less than the natural frequency (ω_n) of this system given this impulse response? Why? [5 points]

$$\omega_d = \omega_n \sqrt{1 - \zeta^2}$$

This is an underdamped system, so $\zeta < 1$, meaning that $\omega_d < \omega_n$. Physically, this should make sense because the damping means that energy is being lost, and that loss mechanism has a finite time constant associated with it that is lower than the natural resonance frequency, causing the downshift (as a function of the damping).

- (b) Bandwidth:

- What is the relative bandwidth (greater or less) of this impulse response compared to that of a continuous sinusoid oscillating at ω_d ? Why? [5 points]

The bandwidth of the impulse response is greater since that of a continuous sinusoid is a delta function in frequency space and can be considered infinitely narrow (bandwidth = 0).

- What would happen to the bandwidth of this impulse (increase or decrease) if the damping coefficient of this system increased? Why? [5 points]

$$2\zeta = \frac{1}{Q}$$

Q is the quality factor, which is inversely proportional to bandwidth, so as ζ increases, it approaches a critically-damped system, and the quality factor decreases, meaning bandwidth increases. Physically, an increased damping coefficient means faster decay of the oscillations, and a tighter envelope on that oscillation means a higher bandwidth (Fourier scaling property).

- (c) Draw the block diagram for a circuit that powers an LED with a 0.7 V threshold voltage on every **other** positive peak of the impulse response signal above 1.54 V (two solid arrows in Figure 2.3) (i.e., use the impulse response as the input signal into your circuit). The LED can remain on until the next temporal positive peak occurs (dashed arrows in Figure 2.3). Be as detailed as possible in your block diagram. [15 points]

The following are the key components to **one** of many designs that could work for this problem.

- Comparator without hysteresis that transitions at a threshold voltage of 1.54 V.
- Convert rail voltages of comparator to logical levels (0 & 5 V). (There are lots of ways to do this.)
- Utilize a JK flip flop that will change its output stage on ever negative edge (could be positive if you specific that, depending on the comparator output); this will frequency divide the count by 2, inherently indicating every other comparator transition.
- Voltage divide (or switch to another source) to provide 0.7 V to the LED and burn the rest of the voltage from the logical high output across a resistor or some other voltage drop.