BME354L (Palmeri)

Spring 2013

Exam #2

Instructions:

- Write your name at the top of each page.
- **Show all work (this is *critical* for partial credit!)**.
- Remember to include units with all answers and label all plot axes.
- Clearly delineate all answers.
- Assume that all components are ideal unless otherwise stated.
- Please keep your answers brief for questions where I ask 'why?'.

In keeping with the Duke Community Standard, I have neither given nor received aid in completion of this examination.

Signature:_____

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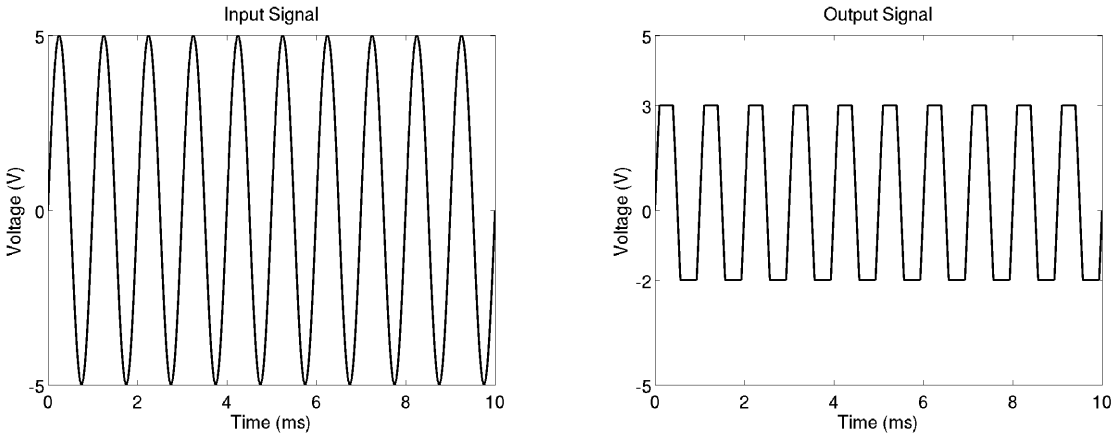
Rectangular waves can be generated from sinusoidal input signals. Figure 1(b) shows a desired rect output signal that has asymmetric positive and negative values (-2 and 3 V).



(a) Input Signal (b) Output Signal

Figure 1: Input and Output Signals

1. Assuming that you have a voltage source (V_{in}) that generates the waveform in Figure 1(a), design a diode-based circuit to generate the output in Figure 1(b). Assume that any diodes that you use in your circuit have forward-bias threshold voltages of 0.7 V. [10 points]

2. Does the output signal have more or less bandwidth than the input signal? Why? [10 points]

3. You can also achieve the output signal from V_{in} by limiting the maximum and minimum voltages represented in the analog-to-digital conversion process (saturating the ADC). Design a 3-bit flash ADC that limits the digital representation of the sinusoidal input to -2:3 V. Please specify all resistor values and, if any, power supplies that you need in your circuit, and assume that any op amps that you use rail at $\pm$ 12 V. For now, you can simply represent your priority encoder for this ADC as a functional block. [15 points]

4. What is the SNR of your digitized output signal, expressed in dB?[1] [5 points]

5. The inputs to your priority encoder are expected to be well-conditioned logic levels (0 or 5 V). Given that your op amps being used in your ADC rail at $\pm$ 12 V, you will need to "level shift" those voltages to 0 and 5 V. Design a level shifting circuit that would be used on the output of each op amp that shifts -12 V $\rightarrow$ 0 and +12 V $\rightarrow$ 5 V. Please specify all relevant component values. [10 points]

6. The priority encoder in your circuit converts your level-shifted op amp outputs to a 3-bit binary number. This can be achieved with simple logic gates (e.g., AND, OR, XOR, etc.). Designing a priority encoder for a 3-bit ADC can be a bit cumbersome during a time-limited exam, so design a priority encoder using simple logic gates that would be used for a 2-bit flash ADC. (*Hint: one simple design could use just 2 OR gates*) [10 points]

7. What is the minimum sampling frequency (fs_{min}) that should be used by your ADC to properly capture the frequency content of the input signal? [5 points]

[1] Remember that in this case, the "noise" is related to the fact that your output signal is now represented by discrete values.

8. Assuming that your input signal runs continuously through time, sketch the power spectrum of your sampled input signal when sampled at fs_{min} for a frequency range of 0–20 kHz. On the same sketch, represent the power spectrum of your input signal when sample at $2 \times fs_{min}$. Make sure that you label which parts of your sketch correspond to each sampling rate. [10 points]

9. The Arduino UNO Rev 3 that you will be using for your final projects has $\sim$32 kB of flash RAM and can sample data at 10,000 samples / second. Given the bit depth of your flash ADC, if you sampled your input signal at this maximum sampling rate of the Arduino, then how many seconds of ADC output could you store in the Arduino's flash RAM? How many more seconds of data can your store if you sample the input signal at fs_{min}? [10 points]

10. Design a DAC that will convert the 3-bit digital representation of the output signal to an analog voltage signal without any phase distortion. You can choose any type of DAC, just be sure to specify all relevant component values. [15 points]

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