Ray Duran, March 16, 2022, BME 690 Spring 2022 Project

Implement a deconvolution of a diffused image in real-time with a Xilinx FPGA

The paper by Antipa and Kuo demonstrate an easy-to-build lens less computational camera for 3-D imaging [1][2]. Here the algorithm makes use of factoring the point spread function into two down sampled matrices achieved by cropping. To solve the inverse problem we make use of solving an optimization problem and rewrite our convolution matrix in an easy way to implement. The convolution theorem allows us to rewrite our PSF and estimate of recovered image in the Fourier domain where we make use of an adjoint matrix. To converge on an optimization solution we use the Fast Iterative Shrinkage Thresholding Algorithm (FISTA) to reconstruct our diffused image.

After we have proven out our algorithm in MATLAB we intent to build our solution in a Ultrascale FPGA development board. The solution architecture will require the use of four 1K 2-dimensional FFTs to take forward and inverse transforms that mix in the PSF and adjoint PSF matrix. Here the deployment of a 2-D FFT in hardware will require some custom digital engineering as the 2-D FFT is not a standard IP module. The entire design will be captured in Simulink, a system modeling tool of the MATLAB family of products. An additional tool that is used in tandem with Simulink is a tool called HDL coder. HDL coder allows a captured design in Simulink to be converted into a hardware description language such as VHDL. With the design represented in VHDL a simulation tool called Modelsim will allow us to simulate the fixed-point design to make sure of the first of several important parameters for implementation. The first is if the design verifies correctly, meaning that the expected output matches our MATLAB model. This first step is important as we iterate the design from model to hardware. Next, is to see if the hardware meets the sample time and speed correctly that we have specified. The combination of logic, DSP and memory blocks must be synthesized and routed onto the fabric of the FPGA and timing must be checked to make sure that setup and hold characteristics of the silicon are met. A third and closely related fourth parameter are to check that the power and resources of are design are met that permit a functional and practical design in an FPGA. As an example, we cannot use all the resources of the FPGA as we must allow a design margin for operation and the addition of extra logic and memory to debug the design in the late stages of development.

**Timeline and milestones:**

1. Specify Tools, intellectual property and development board needed for work 🡪 Completed
2. Write MATLAB code model to represent system 🡪 Completed (Need to Debug) 1-2 weeks
3. Build Simulink system that matches MATLAB model and is synthesizable (fixed point) 🡪 3rd week, and 4th week
4. Simulate in Questa Modelsim HDL of above system 🡪 4th week, 5th week
5. Write up results diagrams🡪 6th and 7th

We estimate that we should be able to process over 30 hz of video frames of a cropped 2048x2592 camera.

Total time for project is 7 weeks to be completed the week of 5/12/22

**References:**

[1] G. Kuo, N. Antipa, et.al., “DiffuserCam: lensless single-exposure 3D imaging,” in Computational Optical Sensing and Imaging (Optical Society of America, 2017), <https://doi.org/10.1364/OPTICA.5.000001>

[2] G. Kuo, N. Antipa, et.al., “DiffuserCam: lensless single-exposure 3D imaging: supplementary material,” in Computational Optical Sensing and Imaging (Optical Society of America, 2017),