



8-bit RISC Processor

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ABOUT PROCESSOR

This is an 8-bit RISC type Processor. Completes each operation in 5 clock cycles.

It contains 4 temporary registers (register file). The memory size is 256 x 8 bit.

Instructions and memory data goes by same address.

WORKING THEORY

Instruction is fetched in 1 clock cycle and stored in Instruction Register (IR).

Immediate value and Decoding instruction are done in second clock cycle.

ALU operation is done in third clock cycle and value is updated in register Rz.

Memory reading or writing is done in fourth clock cycle and value is available at

Multiplexer for writing in Register file.

Register file get updated by new value in fifth clock cycle.

OPERATIONS SUPPORT

The Processor supports the below operations with their respective op-codes.

- ADD 0000
- SUB 0001
- MUL 0010
- AND 0011
- OR 0100
- XOR 0101
- MOV 0110
- HLT 0111
- STA 1000
- JMP 1001
- LDA 1010

INSTRUCTION FORMAT

First four MSB's are for op-codes and the last ones for register address inside the register file.

For STA, JMP and LDA 8 – bit memory address is to be given in the memory block next to the instruction.

Ex.

- ADD R₀ R₁ :- 0000 00 01
- LDA R₁ M :- 1010 01 00 M (8 - bit)
- STA R₁ M :- 1000 00 01 M (8 - bit) Exception (register address is in last 2 bits)
- JMP M :- 1001 00 00 M (8 - bit)
- HLT :- 0111 00 00

PROGRAMS EXECUTED

LDA R0 01H

LDA R1 02H

MUL R0 R1

STA R0 02H

HLT

ASSEMBLY CODE

a0 01

a4 02

21

80 02

70

PROGRAMS EXECUTED

10H LDA R0 00H

LDA R1 01H

ADD R0 R1

JMP 20H

```
20H  LDA R2 02H
      XOR R0 R1
      LDA R3 03H
      AND R0 R3
      JMP 30H
30H  STA R0 04H
      HLT
```

ASSEMBLY CODE

```
10    a0 00
      a4 01
      01
      90 20
20    a8 02
      52
      ac 03
      33
      90 30
30    80 04
      70
```

CONCLUSION

The above programs were executed successfully and respective results were stored in correct memory locations.