Sistemas Digitais Avançados
Universidade Federal de Pelotas – Ciência da Computação
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Tabela de síntese

Implementação	Número de registradores	Total de elementos lógicos usados
Multiplicador Matricial	0	31
Multiplicador Sequencial	19	41

Flow Summary

Flow Status	Successful - Wed May 18 16:49:19 2022
Quartus II 64-Bit Version	13.1.0 Build 162 10/23/2013 SJ Web Edition
Revision Name	MultiSequencial
Top-level Entity Name	multiplicadorSequencial
Family	Cyclone IV GX
Total logic elements	41 / 14,400 (< 1 %)
Total combinational functions	41 / 14,400 (< 1 %)
Dedicated logic registers	19 / 14,400 (< 1 %)
Total registers	19
Total pins	23 / 81 (28 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)
Device	EP4CGX15BF14C6
Timing Models	Final

Flow Summary

Flow Status	Successful - Wed May 18 16:51:45 2022
Quartus II 64-Bit Version	13.1.0 Build 162 10/23/2013 SJ Web Edition
Revision Name	MultiMatricial
Top-level Entity Name	multiplicadorMatricial
Family	Cyclone IV GX
Total logic elements	31 / 14,400 (< 1 %)
Total combinational functions	31 / 14,400 (< 1 %)
Dedicated logic registers	0 / 14,400 (0 %)
Total registers	0
Total pins	16 / 81 (20 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)
Device	EP4CGX15BF14C6
Timing Models	Final