

Wave Digital Filters: Theory and Practice

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Invited Paper

Wave digital filters (WDFs) are modeled after classical filters, preferably in lattice or ladder configurations or generalizations thereof. They have very good properties concerning coefficient accuracy requirements, dynamic range, and especially all aspects of stability under finite-arithmetic conditions. A detailed review of WDF theory is given. For this several goals are set: to offer an introduction for those not familiar with the subject, to stress practical aspects in order to serve as a guide for those wanting to design or apply WDFs, and to give insight into the broad range of aspects of WDF theory and its many relationships with other areas, especially in the signal-processing field. Correspondingly, mathematical analyses are included only if necessary for gaining essential insight, while for all details of more special nature reference is made to existing literature.

I. INTRODUCTION

The importance of digital filters is well established. A vast amount of literature exists on this subject, including many books in various languages, and digital filters are being widely used in a variety of applications. The interested reader may consult a recent tutorial paper, published in the Centennial Issue of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS [1], on the general topic of digital filtering.

Next to nonrecursive digital filters and digital filters composed of simple first- and second-order sections in cascade, wave digital filters (WDFs) represent a class of particular interest. They have first publicly been described in 1970 [2], [3] and a first detailed paper has been published in 1971 [4] (a condensed version thereof being [5] while [6] contains a few added results). Several early papers [4], [7]–[9] on the subject are reprinted in [10], while some other papers bearing a certain relationship to our subject are [11]–[13]. A number of books are now available that give some introductory material [14]–[28]. The purpose of the present paper is to give a brief overview of the state of the art in the field of WDFs.

WDFs represent a class of digital filters that are closely related to *classical filter* networks (see, e.g., [21], [29]–[38]), preferably lossless filters inserted between resistive terminations. Thus to every WDF there corresponds a *reference*

filter from which it is derived. This relationship is the deeper reason for the many interesting properties of WDFs, but also for the somewhat more difficult access to theory and design of these digital filters. Indeed, while the translation of a given reference filter into a WDF is quite straightforward, the selection of a suitable reference structure and its design requires a certain amount of familiarity with classical filter theory, including aspects of microwave filter theory. The analogy between a WDF and its reference filter is based not on the use of voltages and currents as signal parameters, but of so-called *wave quantities* known from *classical circuits* [32], whence the name chosen for the class of digital filters considered in this paper. For sake of clarity, circuits whose topological constraints are the Kirchhoff equations (classical circuits and their multidimensional generalizations) will also be referred to as *Kirchhoff circuits*.

There does not essentially exist just one type of WDFs, but a whole *variety* of quite distinct *subclasses*, each of which can again be divided into various families, etc. This reflects the richness of structures available in classical circuits, and the designer thus should select that one of these reference filter structures that leads to the most appropriate overall solution for the problem at hand. Fortunately, some simple types of WDFs exist which are sufficient to meet most common requirements concerning filter performance, simplicity and modularity of structure, etc., yet such that their design can be accomplished with only very limited knowledge of classical circuits.

Several of the good properties of classical filters are a direct consequence of their *passivity* and, more specifically, the *losslessness* of the filter two-port itself. It is important, therefore, that the relationship between a WDF and a passive reference filter is preserved even after modifying the multiplier coefficients within more or less wide ranges, as is, e.g., required for deriving from the original design a *bit-optimal* version (i.e., a version in which the coefficients are quantized binary numbers selected according to some suitable optimality criterion) by discrete optimization. The most immediate consequences of this are that, for all major WDF structures, the excellent passband sensitivity properties of lossless filters [39]–[41] are preserved, leading to correspondingly reduced *accuracy requirements* for the

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multiplier coefficients and to good *dynamic range* performance (ratio of maximum permitted signal level to roundoff noise level), and also that *stability* under *linear conditions* is automatically ensured.

In fact, even the nonlinearities resulting from the unavoidable rounding and/or truncation operations to which the signals have to be subjected can be carried out, by means of a simple strategy, in such a way that a WDF still behaves like a passive circuit. As a result, if properly designed, a WDF is not only *free of zero-input limit cycles* of either type (granularity and overflow, i.e., small- and large-scale), but does not even exhibit any zero-input parasitic oscillations under the stringent *looped conditions* occurring, e.g., in a long-distance telephone transmission link. Even if a nonzero periodic input is applied, limit cycles, if at all present, remain very small. Furthermore, *forced-response stability* [42]–[44] and related properties can easily be ensured. All these stability aspects are in some respect the most important advantage to be gained from the use of WDFs.

At each port of a WDF there is one input and one output terminal, i.e., for a common two-port filter, thus altogether two input and two output terminals are available. Usually, one will use only one of each of these terminals, but interesting properties can be obtained by not requiring such a restriction. In particular, a WDF derived from a lossless reference filter is inherently a *branching (directional) filter*.

The concept of wave digital filtering can be *extended to any number of dimensions*. All major properties holding in the one-dimensional case are then preserved, independently of degree and the number of dimensions. This includes the low requirements for the coefficient word lengths, good dynamic range, absence of parasitic oscillations (i.e., also of nonperiodic oscillations such as may occur in a multidimensional digital filter due to the fact that such circuits are not finite-state machines), forced-response stability, etc. The computation of the WDF is again easy once a suitable multidimensional reference filter is known. To determine the latter, however, is now the major problem. Important solutions for this problem have already been obtained and further work on this task is in progress [45].

In this paper, we will mainly be dealing with only constant and multirate WDFs. In fact, in view of their excellent stability properties, WDFs are also natural candidates for *adjustable* and *adaptive* filtering. It is thus not surprising that they are intimately related to the most popular types of adaptive digital filters [46], but this subject can only be briefly touched upon. Sections II to X will be devoted exclusively to one-dimensional circuits. Extensions to the multidimensional case are considered in Section XI. As a general rule, we will concentrate on fundamental principles and aspects of immediate importance to the designer. For more advanced theoretical analyses we will refer to the existing literature.

It may be interesting to point out that the first structures for WDFs had actually been obtained by deriving them from structures of *resonant-transfer filters* [47]–[49], to which they are indeed related (and which are also related to so-called *VIS-SC filters* [50]–[52]). No use of this analogy, however, has been made in the original presentations [2]–[6], nor will this be done hereafter. On the other hand, the

entire theory could be developed without explicit recourse to classical circuit theory [55], but this will not be done either since one is then deprived of making immediate use of the many relevant results that have been accumulated over decades and the rigor with which these results have been derived.

Although VIS-SC filters are in some respect the most natural switched-capacitor analogs of WDFs, there are various other ways of establishing a correspondence from WDFs to the *SC-domain* [56]–[64]. Even active filters imitating the WDF principle have been proposed [65], [66]. The term “wave” is often also used to characterize SC or active filters of these types. Finally, it may be mentioned that when approaching the problem of deriving digital filters from classical ones this author had first found an approximate procedure based on the use of voltage and current signals rather than waves. A similar method has been described in the literature [67].

In Part A of the *bibliography* given at the end are listed all papers to which reference is made in the text. Some further papers on WDFs and related subjects are given in Part B. A quite detailed list of references, briefly commented, has also been published in [68], together with a collection of reduced-size copies of more than 170 carefully prepared slides. These slides contain some information which for reasons of space cannot be included in the present paper.

II. BASIC PRINCIPLES

A. Realizability

A digital filter is fully described mathematically by a system of *difference equations*. The implementation of a digital filter requires that the arithmetic operations prescribed by these equations can be ordered *sequentially*, say, inside of a certain time interval of duration T , and that these operations *recur periodically* at a rate

$$F = 1/T. \quad (1)$$

These precedence and periodicity requirements are referred to as the *realizability conditions* [4], [69], the former one alone also as *computability condition* [70].

The mathematical description of a digital filter can equivalently be represented by a *structure* called its *signal-flow diagram*. The latter may thus be called *realizable* or *unrealizable* depending on whether the aforementioned realizability conditions are fulfilled or not. For the more commonly encountered digital filter structures, verification of realizability is rather trivial. For more general structures, however, a more precise theorem is needed.

In order to formulate this, some further terminology is required. Observe first that the delays in a digital filter network do nowhere have to be equal to multiples of T ; they may very well be equal, e.g., to fractions of T , as is already naturally the case if one takes into account the durations inherently associated with carrying out the required arithmetic operations. If all delays are multiples of T we call the circuit *full-synchronous*, otherwise, assuming that the periodicity requirement is fulfilled, *half-synchronous*. We say that the signal-flow diagram of a digital filter is *proper* if it is connected and if it does not contain any branch whose transfer function is zero. A loop is called *directed* (or

else, a feedback loop) if each one of its branches has the same orientation with respect to a given orientation of the loop. The *total delay* of a given loop (with respect to a given orientation) is the sum of the delays in the branches oriented in the same way as the loop minus the sum of the delays in the branches oriented oppositely to the loop. While consideration of negative delays is not without interest for certain theoretical analyses, this is obviously not the case for practical circuits. Thus unless explicitly stated otherwise, we will always assume that there are no negative delays involved. A branch, path, or loop is then called *delay-free* if it does not contain delay elements.

Theorem 1: The signal-flow diagram of a proper digital filter is realizable at a rate $F = 1/T$ if and only if it satisfies the following conditions:

- 1) It does not contain delay-free directed loops.
- 2) The total delay in any loop (directed or not) is equal to a multiple (zero, positive, or negative) of T .

Clearly, for a full-synchronous digital filter the second condition is inherently fulfilled. Necessity of both conditions is quite easy to see. Indeed, if a delay-free directed loop such as, e.g., the one of Fig. 1(a) (comprising two adders and a multiplier of coefficient γ) is present, it would be impossible to give a sequence in which the arithmetic operations required by this loop could be carried out. On the other hand, if there is delay, e.g., $T_1 + T_2$ in the loop of Fig. 1(b), this must be equal to a multiple of T since otherwise the filter could not operate at the rate F . Finally, if there are delays T_1 and T_2 in the paths leading from node P to node Q in Fig. 1(c), the difference $T_1 - (-T_2) = T_1 + T_2$ must, for the same reason, be a multiple (not necessarily a positive one) of T . Sufficiency can be proved quite easily in individual cases; for a complete sufficiency proof we refer to [69].

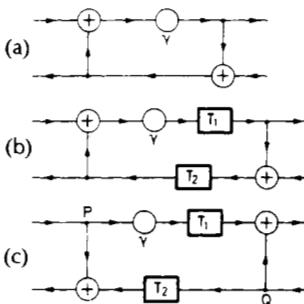


Fig. 1. (a) A delay-free directed loop. (b) A directed loop comprising delays T_1 and T_2 . (c) An undirected loop comprising delays T_1 and T_2 .

B. Choice of Frequency Variable and Signal Parameters (Waves)

In order to establish the correspondence between a WDF and its reference filter we must first observe that this can only be done in the frequency domain, not in the time domain. The latter is indeed discrete for a digital filter, but continuous for a classical filter. However, we cannot simply carry over the complex frequency p from the reference to the digital domain since in the latter, transfer functions are not rational in p . Hence, an appropriate complex frequency variable, say ψ , has to be adopted, and the *reference do-*

main (i.e., the domain of the reference filters) will thus also indifferently be referred to as the ψ -domain. The simplest and most appropriate choice for ψ is the well-known bilinear transform of the z -variable, i.e. [71],

$$\psi = \frac{z - 1}{z + 1} = \tanh(pT/2), \quad z = e^{pT} \quad (2)$$

where p is the actual complex frequency. This variable ψ has the interesting property that real frequencies ω correspond to real frequencies ϕ , according to

$$\phi = \tan(\omega T/2), \quad p = j\omega, \psi = j\phi \quad (3)$$

and that we have

$$\begin{aligned} \text{Re } \psi > 0 &\Leftrightarrow \text{Re } p > 0 \Leftrightarrow |z| > 1 \\ \text{Re } \psi < 0 &\Leftrightarrow \text{Re } p < 0 \Leftrightarrow |z| < 1. \end{aligned} \quad (4)$$

Property (3) implies that real frequencies in the reference filter domain (i.e., imaginary values of ψ) correspond to real frequencies in the digital filter domain (i.e., to imaginary p) and vice versa, and that the Nyquist range $0 < \omega < \pi F$ is precisely mapped, in a one-to-one correspondence, onto the range $0 < \phi < \infty$. Property (4) implies that stable reference filters correspond to stable and causal digital filters and vice versa. In stating this, the term "causal" had to be included since system-function poles at $\psi = 1$, thus at $z = \infty$, have to be excluded not for reasons of stability, but of *causality* (closely related to that of realizability).

Observe that some authors prefer defining ψ by means of $\psi = (2/T)\tanh(pT/2)$, in which case ψ has indeed the dimension of a frequency, and we have $\psi = p$ for small values of p . For our purpose, this does not have any advantage since in filter design one often prefers to use normalized frequencies anyhow and since the approximate relationship mentioned before is of actual use only if all relevant frequencies are far smaller than the Nyquist frequency $F/2$. The latter is almost never the case in properly designed digital filters since it would correspond to a highly oversampled situation.

Next to the frequency variable, the desired correspondence between the digital and analog domains also requires an appropriate selection for the signal variables. For this, one would first think of selecting the voltages and currents in the analog circuit to become signal parameters in the digital domain, but the adoption of ψ as given by (2) can be shown to lead to unrealizable structures [4]. Realizability can be ensured, however, if *wave quantities*, as known from scattering parameter theory [32], are used instead. Actually, it turns out that *voltage* or *current* wave quantities are much more suitable than *power* wave quantities. The choice between the former two is quite irrelevant; it can be shown that passing from one to the other amounts to replacing the original reference filter by its dual [72].

As in all previous literature on WDFs, *voltage* wave quantities are adopted here. Signal-flow diagrams of WDFs will thus interchangeably be referred to as *wave-flow diagrams*. On the other hand, transition from voltage waves to corresponding power waves can always be achieved by including appropriate transformers in the reference circuit. Hence, digital filter structures obtained by using power waves [73], [74] can always be interpreted as WDFs and vice versa (cf. Section IX-H).

In a classical circuit, a *port* is characterized by a *voltage*

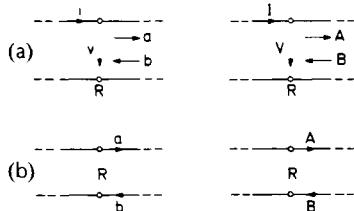


Fig. 2. (a) A port with port resistance R , shown once with instantaneous voltage, current, and waves (left) and once with the corresponding steady-state quantities (right). (b) The corresponding port in a signal-flow representation.

and a *current* (Fig. 2(a)). Furthermore, we can assign to any port a *port resistance* R (indicated underneath the port terminals in Fig. 2(a)). We can do this by choosing for R any arbitrary constant, although in practice one will select that particular value of R which leads to the simplest overall expressions for the problem at hand. In this paper, following the IEC convention, *voltage arrows* will be chosen to point in the *positive direction*, i.e., from the plus to the minus pole.

Assume first *instantaneous* quantities, thus $v = v(t)$ and $i = i(t)$ for voltage and current. The *instantaneous* (voltage) waves (wave quantities, wave signals) are then defined by

$$a = v + Ri \quad b = v - Ri \quad (5)$$

a and b being the waves traveling in the *forward* and the *backward* directions, respectively (or, if the port is in fact the input to a circuit located to its right, the *incident* and *reflected* waves, respectively). Correspondingly, we consider *steady-state* quantities, thus also *steady-state* waves A and B

$$A = V + RI \quad (6a)$$

$$B = V - RI. \quad (6b)$$

At a given complex frequency these are constants.

Clearly, instead of characterizing a port by a voltage and a current, we may just as well use the two wave quantities. In a signal-flow representation (Fig. 2(b)) the term port may thus be used to designate a pair of terminals through which two signals flow in opposite directions, and to such a port may still be assigned a port resistance (or, more generally, port weight [72], [75]). If clarity requires, we may speak in the former case about a *voltage-current port* or a *Kirchhoff port*, in the latter about a *signal port* or a *wave port*. Correspondingly, the terminals in the latter case may also be referred to as *signal terminals* or *wave terminals*. Similarly, a circuit accessible via signal-flow ports or wave ports will also be called a *signal* or *wave one-port*, *two-port*, *multiport*, *n-port*, etc., as the case may be.

Note that the need for the use of wave quantities rather than voltages and currents could be circumvented by defining the relation between ψ and p differently than by (2). Various such possibilities have been examined [67], [76]–[78], but none of these combines the advantages obtainable by adopting (2).

C. Sensitivities to Changes in Multiplier Coefficients

In digital filters, sensitivities to changes in multiplier coefficients are of importance for two reasons. First, they have an important bearing on the accuracy with which

these coefficients have to be implemented [79]. Second, there exists a relationship between noise behavior and sensitivity pointing to the fact that a decrease of sensitivity tends to increase the dynamic range [80]–[83], as has been confirmed numerically and experimentally by a number of authors [85]–[87]. Sensitivity aspects have thus been a major motivation for developing the principle of wave digital filtering.

In Fig. 3 is shown a conventional two-port N inserted between a source of voltage E and resistance R_1 and a load resistance R_2 . The port voltages and currents are V_1 , V_2 , I_1 ,

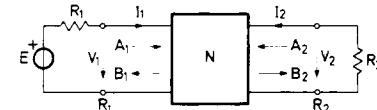


Fig. 3. A two-port N inserted between resistive terminations.

and I_2 . The *transmittance* (transfer function) S_{21} is defined by

$$S_{21} = 2KV_2/E = KB_2/A_1 \quad (7)$$

where

$$K = \sqrt{R_1/R_2} \quad (8a)$$

$$A_1 = V_1 + R_1 I_1 \quad (8b)$$

$$B_2 = V_2 - R_2 I_2. \quad (8c)$$

The equivalence between the two definitions (7) for S_{21} is easily established by means of Fig. 3. Clearly, A_1 is the incident wave at port 1 and B_2 the reflected wave at port 2, defined for port resistances equal to R_1 and R_2 , respectively. The *loss* (attenuation) α corresponding to S_{21} is given by

$$\alpha = -\ln |S_{21}| = (1/2) \ln (P_{\max}/P_2) \quad (9)$$

where $P_{\max} = |E|^2/4R_1$ is the maximum power available from the source and $P_2 = |V_2|^2/R_2$ the power delivered to the load. Hence, if N is *passive* (in which case $P_2 \leq P_{\max}$), we have $\alpha \geq 0$.

Let γ be any circuit parameter (in the case of a filter, usually an inductance or capacitance) inside N . If we indicate explicitly the dependence of S_{21} and α on γ and the frequency ω (or ϕ), we can write

$$\alpha(\omega, \gamma) = -\frac{1}{2} \ln [S_{21}(j\omega, \gamma) S_{21}(-j\omega, \gamma)] \quad (10)$$

and, correspondingly,

$$\alpha(\omega, \gamma) \geq 0. \quad (11)$$

Thus if for a particular value of γ , say γ_0 , we have $\alpha = 0$ at a certain frequency $\omega = \omega_0$, the function of γ , $\alpha(\omega_0, \gamma)$ has a minimum at $\gamma = \gamma_0$. Therefore, since according to (10) this function is differentiable in γ , we have $\partial\alpha(\omega_0, \gamma)/\partial\gamma = 0$ for $\gamma = \gamma_0$, and thus in general

$$\begin{aligned} \partial\alpha/\partial\gamma &= 0, & \text{for } \alpha = 0 \\ \partial\alpha/\partial\gamma &\approx 0, & \text{for } \alpha \approx 0. \end{aligned} \quad (12)$$

This remarkable result [39]–[41] expresses that for a well-designed *lossless* (and thus necessarily passive) filter the sensitivity of the attenuation with respect to any circuit parameter is small all through its passband, and that this

sensitivity is the smaller the closer the attenuation is to its limiting value, zero.

Consider now a digital filter and let γ be any of its multiplier coefficients. The question then arising is how a similarly low sensitivity of attenuation with respect to γ can be achieved. The answer to this is not trivial since only arithmetic operations, but not the transfer of power, are essential to the mechanism of a digital filter, and the concepts of passivity and losslessness thus do not naturally arise. These difficulties are circumvented in WDFs by deriving them from reference structures having the desired properties. This derivation must take into account the terminating resistances R_1 and R_2 since these play an essential role in obtaining (12).

Since wave quantities become the actual signal parameters in WDFs, the relevant transfer function S_{21} and the corresponding attenuation α' are given by

$$S_{21} = B_2/A_1 \quad \alpha' = -\ln|S_{21}| \quad (13)$$

and we have, according to (7) and (9),

$$S_{21} = KS_{21}' \quad (14a)$$

$$\alpha' = \alpha + \alpha_0 \quad (14b)$$

$$\alpha_0 = \ln K \quad (14c)$$

$$\partial\alpha'/\partial\gamma = \partial\alpha/\partial\gamma + \partial\alpha_0/\partial\gamma. \quad (15)$$

As will be seen later (Subsection III-B4, item 5) α_0 may actually depend on γ , whence (12) does not necessarily imply corresponding relations for α' . According to (8a), however, α_0 is independent of ω . Thus due to (14), the loss responses $\alpha(\omega)$ and $\alpha'(\omega)$ differ at most by a constant (i.e., frequency-independent) term, which is irrelevant in practice. Consequently, the distortion due to replacing the original γ by an appropriately quantized number (bit-improved version) is identically the same for $\alpha'(\omega)$ as for $\alpha(\omega)$, and (12) thus ensures equally low distortion for $\alpha'(\omega)$ as for $\alpha(\omega)$.

In fact, the improvement for $\alpha(\omega)$ and $\alpha'(\omega)$ thus obtainable is even substantially better than what might be expected from the first-order theory just discussed. To show this, let $\alpha(\omega, \gamma_0)$ be again the original loss response (Fig. 4(a)), and $\alpha(\omega, \gamma_0 + \Delta\gamma)$ the one obtained after changing γ from γ_0 to $\gamma_0 + \Delta\gamma$ (Fig. 4(b)). The size of $\Delta\gamma$ does not have to be small, but simply such that passivity is preserved, thus according to (11), that $\alpha(\omega, \gamma_0 + \Delta\gamma) \geq 0$ still holds. In this case, the minima can all shift only in the same (upward) direction, albeit by different amounts (indicated in Fig. 4(a) by arrows of different size). The resulting total distortion, $\Delta\alpha$, is thus predominantly determined by the differences of these shifts and is therefore smaller, possibly substantially smaller, than the individual changes of the minima. In other words, the improvement mechanism due to passivity and

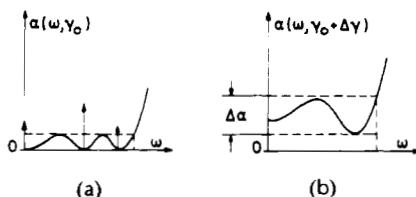


Fig. 4. (a) Loss response of a well-designed lossless filter. (b) Loss response of the same filter after changing the parameter γ by a relatively large amount from γ_0 to $\gamma_0 + \Delta\gamma$.

losslessness ameliorates not only the first-order sensitivities, but even the influence of the higher order sensitivities that must be taken into account in the case of large parameter changes.

It is true that in analog filters this remarkable property does not offer any actual advantage. The reason for this is simply that analog circuits whose actual performance is strongly influenced by higher order sensitivities are usually much too critical to lead to devices sufficiently immune to manufacturing tolerances, temperature variations, and aging. These effects however are irrelevant in digital circuits. For the latter, changes of loss characteristics due to coefficient changes are of relevance only during the design process, but are not relevant once the precise values to be implemented have been decided upon.

For the influence of attenuation sensitivity upon dynamic range (ratio of overflow level to roundoff noise) [80]–[83], the relevant expression is $\partial\alpha'/\partial\gamma$, not $\partial\alpha/\partial\gamma$. The value of the last term in (15), however, is such that it does not endanger the excellent noise properties of WDFs, especially if some other relevant aspects are properly taken into account (cf. Section VII-C). Nevertheless, there is a definite interest in structures for which $\partial\alpha_0/\partial\gamma$ reduces to zero [88].

III. BUILDING BLOCKS

A. Elements and Sources

In order to arrive at the desired structures we first examine how elements and sources are translated from the reference domain to the WDF domain (and vice versa). We first consider one-port, then two-port and multiport elements. Since, as discussed in the beginning of Section II-A, the equivalence can hold only in the ψ -domain, we always use steady-state expressions as point of departure.

In the reference domain, a capacitance and an inductance (Table 1, first two columns) are described by the steady-state equations (cf. second row in Table 1)

$$V = RI/\psi \quad V = \psi RI. \quad (16)$$

Indeed, V must be proportional to I and, since ψ is assuming the role of a complex frequency, proportional to $1/\psi$ and ψ , respectively. The proportionality constant determining the size of the element can always be written in the numerator, in which case it has the dimension of a resistance.

Let us now select for the port resistance the same value R as that appearing in (16). Using (2) and (6), (16) yields

$$B = z^{-1}A \quad \text{and} \quad B = -z^{-1}A \quad (17)$$

respectively. To these expressions correspond the equations

$$b(t_m) = a(t_m - T) \quad (18a)$$

and

$$b(t_m) = -a(t_m - T) \quad (18b)$$

where

$$t_m = t_0 + mT, \quad m = \dots, -1, 0, 1, 2, \dots \quad (19)$$

t_0 being an arbitrary constant. It is indeed easily checked that (18) leads to (17) if we substitute for the steady-state conditions

$$a = a(t) = Ae^{\rho t} \quad b = b(t) = Be^{\rho t} \quad (20)$$

where t takes, in fact, the discrete values t_m given by (19).

Table 1 Major One-Port Elements and Sources and Their Realization in the WDF Domain.

Capacitance	Inductance	Resistance	Short-circuit	Open-circuit	Resistive source	Voltage source
$V = IR/\psi$	$V = \psi RI$	$V = RI$	$V = 0$	$I = 0$	$V = E + RI$	$V = E$
$B = z^{-1}A$	$B = -z^{-1}A$	$B = 0$	$B = -A$	$B = A$	$B = E$	$B = 2E - A$
$b(t_n) = a(t_n - T)$	$b(t_n) = -a(t_n - T)$	$b = 0$	$b = -a$	$b = a$	$b = e$	$b = 2e - a$

These results and the final wave-flow diagrams are included in Table 1.

We can proceed in the same way for the *resistance*, the *short circuit*, the *open circuit*, the *resistive source*, and also (although this is of somewhat lesser importance) the (pure) *voltage source*. The corresponding results are also included in Table 1, the expression corresponding to (20) for the source voltage being $e = e(t_m) = Ee^{pt_m}$ where E is a complex constant. Observe that for the open circuit, the short circuit, and the voltage source (fourth, fifth, and last columns in Table 1) the port resistance may be chosen arbitrarily since, in these three cases, the defining equations do not contain any resistive parameter.

Further one-port elements such as *supercapacitances* and *superinductances* can also be defined [89], but these will not be considered in this paper because they do not have proved to bring true advantages. For a *current source* of source current E/R , selecting the port resistance equal to R amounts to replacing, in the last column of Table 1, B and b by $-B$ and $-b$, respectively.

It is important to notice that the constant t_0 may be different for each signal considered. This is due to the presence of delays (possibly also fractional delays, although these do not appear in Table 1) and must properly be taken into consideration if the relative timing at the various places in the circuit is correctly to be taken into account. As an example, consider the expression (18a) which we can also write in the form $b(t_m) = a(t'_m)$, with t_m given by (19) and t'_m by

$$t'_m = t_0' + mT, \quad m = \dots, -1, 0, 1, 2, \dots$$

thus with $t_0' = t_0 - T$ and $t'_m = t_m - T$. Clearly, t'_m generates the same sequence of time instants as t_m , but this does not have to be the case if the delay involved is not a multiple of T , as will be the case hereafter.

The most important two-port element is the so-called *unit element* (first column in Table 2), which also plays a major role in microwave filter theory [90]–[95]. It can be defined by

$$\begin{aligned} V_1 &= V_2 \cosh(pt/2) - RI_2 \sinh(pt/2) \\ I_1 &= (V_2/R) \sinh(pt/2) - I_2 \cosh(pt/2) \end{aligned} \quad (21)$$

or, equivalently, by its chain matrix, K , listed in Table 2. It corresponds to a transmission line of delay $T/2$ and characteristic impedance R . Recall that for the orientation of the current I_2 as adopted here the chain matrix of a two-port is defined by

Table 2 Realization of a Unit Element, a QUARL, and a Gyrator.

Unit element	QUARL	Gyrator
$K = \frac{1}{\sqrt{1-\psi^2}} \begin{pmatrix} 1 & \psi R \\ \psi R & 1 \end{pmatrix}$	$K = \frac{\psi DA}{\sqrt{1-\psi^2}} \begin{pmatrix} 1 & \psi R \\ \psi R & 1 \end{pmatrix}$	$K = \begin{pmatrix} 0 & -R \\ 1/R & 0 \end{pmatrix}$
$B_1 = e^{-pt/2} A_2, B_2 = e^{-pt/2} A_1$	$B_1 = e^{-pt_{12}} A_2, B_2 = e^{-pt_{21}} A_1$	$B_1 = -A_2, B_2 = A_1$
$b_1(t_{im}) = a_2(t_{im} - T/2)$ $b_2(t_{2m}) = a_1(t_{2m} - T/2)$	$b_1(t_{im}) = a_2(t_{im} - T_{12})$ $b_2(t_{2m}) = a_1(t_{2m} - T_{21})$	$b_1 = -a_2, b_2 = a_1$
$a_1 \rightarrow T/2 \rightarrow a_2$ $b_1 \rightarrow T/2 \rightarrow a_2$	$a_1 \rightarrow T_{12} \rightarrow a_2$ $b_1 \rightarrow T_{21} \rightarrow a_2$	$a_1 \rightarrow a_2$ $b_1 \rightarrow -1 \rightarrow a_2$

$$V_1 = K_{11}V_2 - K_{12}I_2$$

$$I_1 = K_{21}V_2 - K_{22}I_2$$

$$K = \begin{pmatrix} K_{11} & K_{12} \\ K_{21} & K_{22} \end{pmatrix}.$$

Replacing (6) by

$$A_i = V_i + RI_i, \quad B_i = V_i - RI_i, \quad i = 1, 2 \quad (22)$$

and selecting the port resistances (parameters R in (22)) equal to the *characteristic impedance* (parameter R in (21)) we obtain from (21) the equations listed in row 4, column 1, of Table 2. Right underneath these equations are listed two difference equations, which yield the previous equations as steady-state solutions if we write

$$a_i(t) = A_i e^{pt}, \quad b_i(t) = B_i e^{pt}, \quad i = 1, 2 \quad (23)$$

where, in each case, t takes only those discrete values to which the respective one of the four signals a_1, a_2, b_1 , and b_2 refers. (In other words, although t is, in fact, always of the general form (19), the parameter t_0 may be different for each one of the four signals considered.) In particular, if we designate by t_{im} the discrete time instants to which b_i refers, $i = 1, 2$, the difference equations considered can be written as shown in Table 2.

A generalization of the unit element is the *quasi-reciprocal line*, or *QUARL* [49], [96]. It has the same characteristic impedance R , and the same *average delay* $(T_{21} + T_{12})/2 = T/2$, as the unit element, but the individual delays in the right and left directions T_{21} and T_{12} , respectively, do not have to be the same, i.e., the *differential delay*

$$\Delta = (T_{21} - T_{12})/2 \quad (24)$$

does not have to be zero. Proceeding as for the unit element one finds the results listed in the second column of Table 2. Notice the arrow in the representation of the QUARL; it refers to the choice of sign adopted for relating T_{21} and T_{12} to Δ . (Recall that quasi-reciprocity of a two-port refers to the fact that its transfer properties in the two directions differ only by a constant, i.e., frequency-independent delay [48].)

An element that can be implemented very easily is the *gyrator*, as explained in the third column of Table 2. For the *ideal transformer*, several realizations are of interest. One of these is given in the first column of Table 3, and the others will be explained later. Observe that it is essential now that

Table 3 A: Ideal Transformer. B and C: Its Realization for Two Special Choices of R_2 . D: For Arbitrary Choices R_1 , R_2 , and n (cf. Fig. 46).

A	C Choice $R_2=nR_1$
$V_2=nV_1, h=-nI_2$	
Choice $R_2=n^2R_1$: $b_1=\frac{1}{n}a_2, b_2=na_1$	Arbitrary choice of R_1, R_2 , and n

the port resistances at the two ports, R_1 and R_2 , do not have to be the same; hence, (22) has to be replaced by

$$A_i = V_i + R_i I_i, \quad B_i = V_i - R_i I_i, \quad i = 1, 2. \quad (25)$$

Next to the gyrator, a further nonreciprocal element is the *circulator*. It has n ports, with $n \geq 3$ and is best described directly in terms of wave quantities. Thus using (22) but with $i = 1$ to n , we have

$$B_1 = A_n, \quad B_2 = A_1, \dots, B_n = A_{n-1}. \quad (26)$$

The resulting realizations for a three-port and a four-port circulator are shown in Table 4. The extension for $n > 4$ is trivial.

Table 4 Realization of Three-Port and Four-Port Circulators.

$b_1=a_3, \quad b_2=a_1$ $b_3=a_2$	$b_1=a_4, \quad b_2=a_1$ $b_3=a_2, \quad b_4=a_3$

For the elements of Tables 1 and 2, except for the gyrator, passivity requires the resistive parameter R to be positive. For gyrators and circulators one might have $R < 0$, but the same effect can be achieved by inverting the orientation of the arrow appearing in the symbol representing the corresponding element. Hence, we can assume without restriction that $R > 0$ in all cases.

We still want to comment briefly on the principle discussed earlier in relation with the appearance of constants such as t_0 and t'_0 when writing explicitly the time dependence of signals. Failing to observe this principle is the reason why mistakes are sometimes made in analyzing sampled-data systems. Also, in order to avoid pitfalls it is easiest to work systematically with the steady-state concept, as we are doing here, and to use thus, implicitly or explicitly, a z -transform definition that is somewhat different from the one usually adopted. This is why this author has opted for this approach throughout his dealing with sampled-data systems [1]–[6], [48]–[52], and the advantages thus to be gained have also recently been pointed out appropriately and clearly in [97]. Note that a steady-state approach, which in fact is simpler than an approach based on applying z -transformations to time-domain equations, is amply sufficient for dealing with all aspects to be considered in this paper. For this reason, the concept of z -transform (in the standard or the alternative form alluded to before) will hereafter not be used explicitly.

B. Interconnections and Adaptors [4], [8], [98]

1) *Interconnections*: We have seen how it is possible to simulate in the digital domain the main elements and sources, but in order to fully establish an equivalence with classical circuits we must also simulate the *interconnections*, or in other words, the topological rules (Kirchhoff's laws). The most important of these are the *series* and the *parallel* connections. Since interconnections are not frequency-dependent we will, for reasons of simplicity, use throughout hereafter instantaneous rather than steady-state quantities (as, in fact, we could also have done in Section III-A for all frequency-independent elements and the sources). Note that for all cases discussed in Section III-A where a resistive parameter R appeared in the ψ -domain description the final result was independent of R . In fact, R is then always hidden in the defining expressions for the wave quantities. Thus since R will in general be different in each individual case, it is to be expected that the influence of the resistive parameters will reappear when examining the interconnections.

2) *Parallel Adaptors*: Consider first a *parallel* connection of n ports (Table 5A), with port resistances R_1 to R_n . It must be possible for the latter to take arbitrary values since these are usually fixed by whatever element, etc., is connected to the corresponding port. For the wave quantities we thus write

$$a_\nu = v_\nu + R_\nu i_\nu, \quad b_\nu = v_\nu - R_\nu i_\nu, \quad \nu = 1 \text{ to } n. \quad (27)$$

Mathematically, the parallel connection is described by

$$v_1 = v_2 = \dots = v_n \quad i_1 + i_2 + \dots + i_n = 0. \quad (28)$$

Eliminating the v_ν and i_ν from (27) and (28), we obtain

$$b_\nu = (\gamma_1 a_1 + \gamma_2 a_2 + \dots + \gamma_n a_n) - a_\nu, \quad \nu = 1 \text{ to } n \quad (29)$$

where

Table 5 A: Parallel Connection of n Ports. B: n -Port Parallel Adaptor and Corresponding Fundamental Equations. C: n -Port Parallel Adaptor whose Port n is Reflection-Free and Corresponding Fundamental Equations.

A	B	C
$v_1 = v_2 = \dots = v_n$ $i_1 + i_2 + \dots + i_n = 0$ $\gamma_v = \frac{2G_v}{G_1 + G_2 + \dots + G_n}$ $\gamma_1 + \gamma_2 + \dots + \gamma_n = 2$	$a_0 = Y_1 a_1 + Y_2 a_2 + \dots + Y_{n-1} a_n$ $b_0 = a_0 - a_v$, $v = 1 \text{ to } n$, $G_v = 1/R_v$ $\gamma_v = b_v/a_v - a_v$, $b_v = b_n + a_n - a_v$, $\gamma_v = \frac{G_v}{G_n}$, $v = 1 \text{ to } n-1$ $\gamma_1 + \gamma_2 + \dots + \gamma_{n-1} = 1$	$G_n = G_1 + G_2 + \dots + G_{n-1}$ $b_n = Y_1 a_1 + Y_2 a_2 + \dots + Y_{n-1} a_{n-1}$ $a_n = a_n - a_v$, $v = 1 \text{ to } n-1$, $G_v = 1/R_v$ $\gamma_v = b_v/a_v - a_v$, $b_v = b_n + a_n - a_v$, $\gamma_v = \frac{G_v}{G_n}$, $v = 1 \text{ to } n-1$ $\gamma_1 + \gamma_2 + \dots + \gamma_{n-1} = 1$

$$\gamma_v = 2G_v/(G_1 + G_2 + \dots + G_n), \quad G_v = 1/R_v, \quad (30)$$

the G_v , $v = 1$ to n , being the *port conductances*, and we have

$$\gamma_1 + \gamma_2 + \dots + \gamma_n = 2. \quad (31)$$

Clearly, (29) expresses the reflected waves b_v in terms of the incident waves a_v . The mathematical operations involved are additions/subtractions as well as multiplications by constants, thus operations like in any other type of digital filter. We will say that (29) and (30) describe a *parallel adaptor*, and we use for this the graphical representation shown in Table 5B (the symbol inside the box being self-explanatory) together with relations corresponding to (29) to (31).

By making use of (31), the coefficient γ_v of one of the ports, called the *dependent port*, can be eliminated. The elimination process should be carried out in such a way that the number of additions required by the resulting equations is minimized. By choosing port n as dependent port, a suitable way of rewriting (29) is

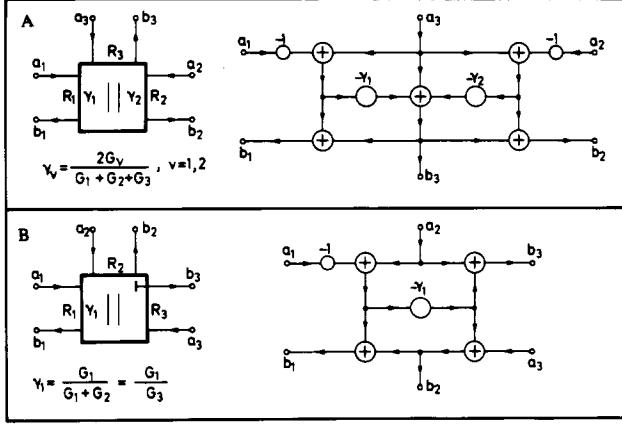
$$b_n = a_n - \sum_{v=1}^{n-1} \gamma_v (a_n - a_v) \quad (32a)$$

$$b_v = b_n + (a_n - a_v), \quad v = 1 \text{ to } n-1. \quad (32b)$$

So far we have not made any particular assumptions concerning the R_v . If we want to make this fact explicit, we may thus call the adaptor under consideration more specifically an *unconstrained parallel adaptor*. According to (32), an unconstrained n -port parallel adaptor requires $n-1$ multiplications and $3n-3$ additions. The number of multiplications is thus far less than the number n^2 which would correspond to a general linear relation between the a_v and the b_v . An unconstrained three-port parallel adaptor together with its signal-flow diagram is shown in Table 6A, port 3 being the dependent port. Observe that this signal-flow diagram, which had already been included in [98], is simpler than the one originally presented [4], but which unfortunately is reproduced in many of the books mentioned above and in many publications by other authors.

Of particular interest are parallel adaptors for which one

Table 6 A: Unconstrained Three-Port Parallel Adaptor and Corresponding Signal-Flow Diagram, Port 3 Being Dependent. B: Constrained Three-Port Parallel Adaptor, with Port 3 Reflection-Free, and Corresponding Signal-Flow Diagram, Port 2 Being Dependent.



of the γ_v is equal to one, and we then say that the corresponding port is *reflection-free*. If this is the case for port n , we thus have

$$\gamma_n = 1 \quad (33a)$$

i.e.,

$$G_n = G_1 + G_2 + \dots + G_{n-1} \quad (33b)$$

$$\gamma_1 + \gamma_2 + \dots + \gamma_{n-1} = 1 \quad (34)$$

$$\gamma_v = G_v/G_n, \quad v = 1 \text{ to } n-1 \quad (35)$$

and according to (29), b_n then becomes independent of a_n . This absence of reflection is represented symbolically in Table 5C by a stroke at the output of port n , and the corresponding adaptor is said to be *constrained*. The fundamental equations now applicable are also summarized in the same column of Table 5. From a physical point of view, (33b) can be interpreted to express that R_n is equal to the input resistance at port n if the other ports are terminated by their respective port resistances.

According to (34), any of the ports other than n may again be chosen as dependent port. If we select, for this, port $n-1$, (32) may be replaced by

$$b_0 = - \sum_{v=1}^{n-2} \gamma_v (a_{n-1} - a_v) \quad (36a)$$

$$b_{n-1} = b_0 + a_n \quad b_n = b_0 + a_{n-1} \quad (36b)$$

$$b_v = b_{n-1} + (a_{n-1} - a_v), \quad v = 1 \text{ to } n-2 \quad (36c)$$

which requires $n-2$ multiplications and $3n-5$ additions. A constrained three-port parallel adaptor, with port 3 reflection-free and port 2 dependent, is shown in Table 6B together with a corresponding signal-flow diagram.

3) Series Adaptors: Consider now a *series* connection of n ports (Table 7A) with port resistances R_1 to R_n . Eliminating the voltages and currents from (27) and the defining equations

$$v_1 + v_2 + \dots + v_n = 0 \quad i_1 = i_2 = \dots = i_n \quad (37)$$

leads to

$$b_v = a_v - \gamma_v (a_1 + a_2 + \dots + a_n), \quad v = 1 \text{ to } n \quad (38)$$

where

Table 7 A: Series Connection of n Ports. B: n -Port Series Adaptor and Corresponding Fundamental Equations. C: n -Port Series Adaptor whose Port n is Reflection-Free and Corresponding Fundamental Equations.

A	B	C
$v_1 + v_2 + \dots + v_n = 0$ $i_1 = i_2 = \dots = i_n$	$a_0 = a_1 + a_2 + \dots + a_n$ $b_v = a_v - v a_0$ $v = 1 \text{ to } n$ $\gamma_v = \frac{2R_v}{R_1 + R_2 + \dots + R_n}$ $\gamma_1 + \gamma_2 + \dots + \gamma_n = 2$	$R_n = R_1 + R_2 + \dots + R_{n-1}$ $b_n = -(a_n + a_{n-1} + \dots + a_1)$ $b_v = a_v - v(a_n - b_n)$ $\gamma_v = \frac{R_v}{R_n}, \quad v = 1 \text{ to } n-1$ $\gamma_1 + \gamma_2 + \dots + \gamma_{n-1} = 1$

$$\gamma_v = 2R_v / (R_1 + R_2 + \dots + R_n) \quad (39)$$

(31) thus holding again. We say that (38) and (39) describe a *series adaptor*, and we use for this the graphical representation shown in Table 7B (the symbol inside the box being again self-explanatory) together with relations corresponding to (31), (38), and (39).

In view of the validity of (31) we may again select one of the ports as *dependent port* and eliminate the corresponding γ_v . If for this, port n is chosen, a suitable way of rewriting (38) is

$$a_0 = a_1 + a_2 + \dots + a_n \quad (40a)$$

$$b_v = a_v - \gamma_v a_0, \quad v = 1 \text{ to } n-1 \quad (40b)$$

$$b_n = -(b_1 + b_2 + \dots + b_{n-1} + a_0). \quad (40c)$$

According to these equations, an *unconstrained* n -port series adaptor requires $n-1$ multiplications and $3n-3$ additions, the same as for an unconstrained n -port parallel adaptor. An unconstrained three-port series adaptor together with its signal-flow diagram is shown in Table 8A.

Of particular interest are series adaptors for which one of the γ_v is equal to one, and we then say that the corre-

Table 8 A: Unconstrained Three-Port Series Adaptor and Corresponding Signal-Flow Diagram, Port 3 Being Dependent. B: Constrained Three-Port Series Adaptor, with Port 3 Reflection-Free, and Corresponding Signal-Flow Diagram, Port 2 Being Dependent.

A	B

sponding port is *reflection-free*. If this is the case for port n , we thus have

$$\gamma_n = 1 \quad (41a)$$

i.e.,

$$R_n = R_1 + R_2 + \dots + R_{n-1} \quad (41b)$$

$$\gamma_v = R_v / R_n, \quad v = 1 \text{ to } n-1 \quad (42)$$

and according to (38), b_n then becomes independent of a_n . This absence of reflection is again represented symbolically in Table 7C by a stroke at the output of port n , and the corresponding adaptor is again said to be *constrained*. The fundamental equations applicable in this case are also summarized in the same column of Table 7. From a physical point of view, (41b) can be interpreted to express that R_n is equal to the input resistance at port n if the other ports are terminated by their respective port resistances.

Since (34) holds again, any of the ports other than n may be chosen as dependent port. If we select, for this, port $n-1$, (40) may be replaced by

$$b_n = -(a_1 + a_2 + \dots + a_{n-1}), \quad a_0 = a_n - b_n \quad (43a)$$

$$b_v = a_v - \gamma_v a_0, \quad v = 1 \text{ to } n-2 \quad (43b)$$

$$b_{n-1} = -(b_1 + b_2 + \dots + b_{n-2} + a_n) \quad (43c)$$

which requires $n-2$ multiplications and $3n-5$ additions, the same as for the corresponding parallel adaptor. A constrained three-port series adaptor, with port 3 reflection-free and port 2 dependent, is shown in Table 8B together with a corresponding signal-flow diagram.

4) *Some General Conclusions:* From the results obtained so far, some general conclusions may be drawn:

1) The building blocks of adaptors are *adders* and *multipliers*, thus they are basic constituents of any digital filter. The other basic constituents, i.e., delays, have been encountered in the description of the frequency-dependent elements.

2) *Port resistances* may be any real numbers. In relation with the passivity properties mentioned in the second last paragraph of Section III-A it must, in general, be expected, however, that these numbers are positive. If this is the case, all multiplier coefficients encountered above are *positive*, but ≤ 2 (cf. (31)).

3) A multiplier coefficient can always be associated with a particular adaptor *port*. If for a given adaptor some or all of the multiplier coefficients should be made explicit without giving details about the inner structure (signal-flow diagram) of the adaptor, this can always be done by writing these coefficients next to the port to which they refer, preferably inside the box representing the adaptor. This will be made use of wherever desirable.

4) No relation between the *port resistances* has to exist except if one of the ports is to be reflection-free. In the latter case, one of the port resistances is fixed by the others.

5) For any two distinct ports μ and ν we have, for a parallel and a series adaptor, respectively,

$$R_\nu / R_\mu = \gamma_\mu / \gamma_\nu \quad (44a)$$

$$R_\nu / R_\mu = \gamma_\nu / \gamma_\mu \quad (44b)$$

Thus if all the γ_v , $v = 1 \text{ to } n$, and one of the R_v , say R_μ , are given, the *remaining* port resistances can be computed by

(44). All the port resistances then turn out positive if R_μ and the γ_v are positive. However, for these port resistances to correspond actually to the given values of the γ_v , (30) and (39), respectively, must be satisfied. Substituting in these equations the R_v computed from (44a) and (44b), respectively, we obtain the original γ_v under condition that (31) holds. Thus imposing positive values for the γ_v , $v = 1$ to n , and for R_μ leads to an acceptable solution of the remaining R_v if and only if (31) holds. The latter is automatically the case if one of the coefficients has been eliminated by choosing the corresponding port as dependent port. This coefficient is in a sense being realized indirectly, and its correct value to be used in (44) is thus the one computed by means of (31). The situation is essentially the same if one of the ports is reflection-free, except that one may then replace (31) by (34) and compute the port resistance at the reflection-free port by expressions such as (33b) and (41b), respectively.

6) For a given type of interconnection (parallel or series) and given port resistances one still has a certain amount of freedom available due to the possibility of freely choosing the *dependent port*, i.e., the port whose corresponding coefficient is to be eliminated by using (31) or (34). Furthermore, if one modifies the other coefficients (e.g., in order to replace them by appropriately quantized numbers) this will implicitly affect the eliminated coefficient through the continued validity of the respective one of the equations just mentioned. If the eliminated coefficient is small it may suffer quite a large relative change and may even become negative, contrary to what is usually permitted.

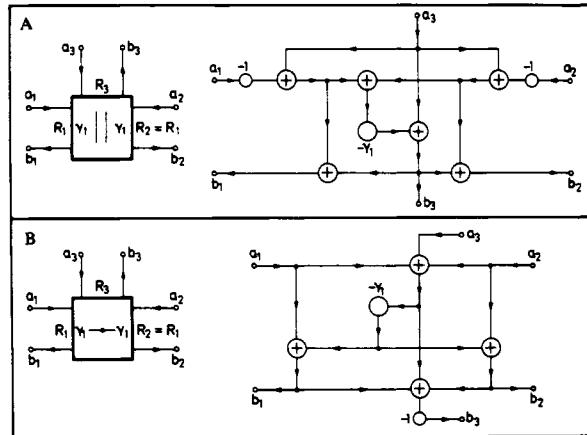
In a conclusion, in order to minimize the relative change of the coefficient realized implicitly, that port should be chosen as the *dependent one* whose corresponding coefficient is the *largest*, or at least not smaller than any of the others. If this choice is made, then according to (31) and (34) none of the coefficients actually to be implemented can exceed 1 in the case of unconstrained adaptor,¹ and 1/2 in the case of a constrained adaptor.

7) It may happen that two of the port resistances, and hence two of the multiplier coefficients turn out to be the same. In this case, the corresponding multipliers can be combined into a single one, thus leading to further simplifications. This may easily be checked by means of equations such as (29), (32), (36), (38), (40), and (43). The resulting simplified signal-flow diagrams for the three-port adaptors of Tables 6A and 8A are shown in Table 9.

8) While it is frequently of interest to reduce to a minimum the number of multipliers, this does not always have to be true, especially for low values of n , say for $n = 2$. This is the case in particular if universal digital signal processors of the type presently available are being used, as will be explained later (cf. Section VIII-D). Nevertheless, even if one would use the maximum number, n^2 , of multiplications, all coefficients then involved could be expressed by means of simple additions/subtractions of $n - 1$ of the γ_v . Thus if these latter γ_v are expressed in terms of a finite number of bits, all the other coefficients are rigorously obtained also with only a finite number of bits.

¹The limit 1 is replaced by 1/2 if one replaces γ_v by $\gamma'_v = 1 - \gamma_v$ in case $\gamma_v > 1/2$; this can be shown by means of (32) and (40) not to require any supplementary addition.

Table 9 A: Unconstrained Three-Port Parallel Adaptor. B: Unconstrained Three-Port Series Adaptor, Both with $R_1 = R_2$, Port 3 Being Dependent. Each one of the Signal-Flow Diagrams Involves only One Multiplier.



C. Two-Port Adaptors

The simplest adaptors are those with $n = 2$. Since two ports connected in parallel can also be considered to be connected in series, one might expect two-port series and parallel adaptors to be the same. This is essentially true, but as can be concluded from the drawings in Tables 5A and 7A, the orientation of voltage and current at one of the ports, say port 2, has to be reversed if one passes from the parallel to the series connection. As a result, the two types of two-port adaptors are related as shown in Fig. 5(a). (Note

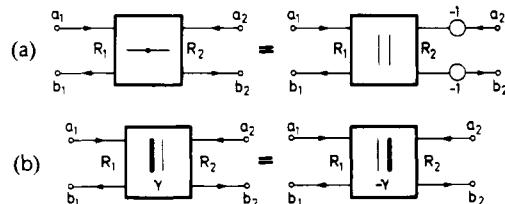


Fig. 5. (a) Equivalence between a two-port series and a two-port parallel adaptor. (b) A simple equivalence between two-port parallel adaptors.

that the two multipliers of coefficients -1 appearing there at one of the ports correspond in fact to an ideal transformer of ratio -1 (cf. Table 3B, i.e., to a crossing of the two leads in the corresponding port of the reference-filter domain). In any case, only one of the two types is usually required, and we will opt here for the two-port parallel adaptor. Note that the separate symbol introduced in [4] for two-port adaptors is thus superfluous and in some respect even confusing.

From (32), we obtain for the two-port parallel adaptor

$$b_2 = a_2 - \gamma_1(a_2 - a_1) \quad (45a)$$

$$b_1 = b_2 + a_2 - a_1 \quad (45b)$$

and, correspondingly, if port 1 is chosen as dependent port

$$b_1 = a_1 - \gamma_2(a_1 - a_2) \quad (46a)$$

$$b_2 = b_1 + a_1 - a_2 \quad (46b)$$

where

$$\gamma_1 = 2R_2/(R_1 + R_2) \quad (47a)$$

$$\gamma_2 = 2R_1/(R_1 + R_2). \quad (47b)$$

A more symmetrical way of writing these equations is

$$b_1 = a_2 + \gamma(a_2 - a_1) \quad (48a)$$

$$b_2 = a_1 + \gamma(a_2 - a_1) \quad (48b)$$

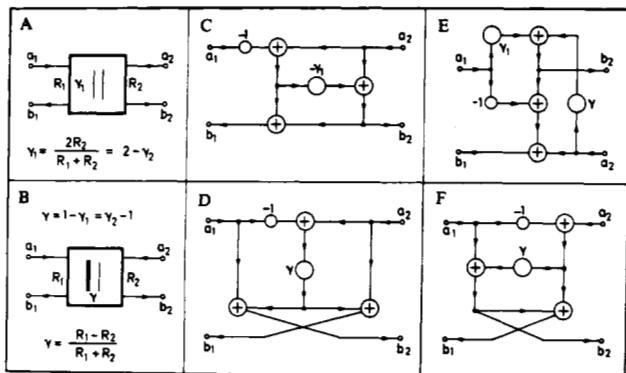
$$\gamma = (R_1 - R_2)/(R_1 + R_2) \quad (49)$$

γ being no longer restricted to be positive, although such that

$$-1 < \gamma < 1. \quad (50)$$

In the symbolic representation of (45) given in Table 10A we have, this time, shown explicitly the parameter γ_1 next to port 1 (cf. item 3 in Subsection III-B4). If we want to indicate explicitly in a similar way the coefficient γ , we will do this as shown in Table 10B. Clearly, an orientation must

Table 10 A and B: Representation of a Two-Port Parallel Adaptor, the Coefficients γ_1 and γ , Respectively, Being Shown Explicitly. C to F: Corresponding signal-flow Diagrams, Three Further Such Diagrams Being Obtainable by Interchanging the Input and Output Ports in C, D, and F with γ_1 and γ replaced by γ_2 and $-\gamma$, respectively.



now be given since according to (49), γ is defined with port 1 appearing first in the difference term $R_1 - R_2$. We have taken this into account by using a heavy line for drawing that of the two bars inside the box which is closest to port 1. (Thus if the right of these two bars were drawn in heavy line this would indicate that γ were defined by $(R_2 - R_1)/(R_1 + R_2)$.)

The signal-flow diagrams corresponding to (45) and (48) are given in Table 10C and 10D, respectively, while the diagram corresponding to (46) is the mirror image of the one in Table 10C with γ_1 replaced by γ_2 . In all three cases available we thus need 1 multiplier and 3 adders. Hence, all three solutions are equally acceptable, and according to the guiding principles given in item 6, Subsection III-B4, we should adopt that one of these solutions for which the corresponding coefficient is smallest in absolute value. Using (50) and

$$\gamma_1 = 1 - \gamma \quad (51a)$$

$$\gamma_2 = 1 + \gamma \quad (51b)$$

it is easily verified that there is always precisely one of the coefficients $\gamma, \gamma_1, \gamma_2$ whose modulus is smaller than $\frac{1}{2}$, except for the simple cases $\gamma_1 = \gamma = \frac{1}{2}$ and $\gamma_2 = -\gamma = \frac{1}{2}$.

The possibility mentioned in item 8 of Subsection III-B4 can be of interest in particular in the case of two-port

adaptors. The corresponding equations are

$$b_1 = -\gamma a_1 + \gamma_2 a_2 \quad (52a)$$

$$b_2 = \gamma_1 a_1 + \gamma a_2 \quad (52b)$$

preferably combined with (46b) and (45b), respectively (cf. Table 10E for the second of these choices). Finally, Table 10F shows an alternative to the signal-flow diagram of Table 10D. It has some advantage in relation to the need for providing shimming delays (cf. Section VIII-B). A further alternative is the mirror image of the structure in Table 10F, with γ replaced by $-\gamma$ (cf. Fig. 5(b)).

IV. REALIZATION OF CIRCUITS

A. General Principles

In Section III we have seen how the various building blocks for WDFs can be realized. When interconnecting them (Fig. 6) to form a digital filter circuit the following principles must be observed:

1) The building blocks must be interconnected in such a way that the grouping of terminals into ports remains respected, i.e., the two wave terminals of one port must be connected to the two wave terminals of precisely one other port.

2) For every two wave terminals which are joined together the two corresponding waves must flow in the same direction. In other words, if the notation used in Section III is maintained throughout and we consider a port 1 connected to a port 2, we must have

$$a_1 = b_2 \quad a_2 = b_1. \quad (53)$$

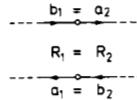


Fig. 6. Compatible interconnection of two wave ports.

3) For any two ports thus combined, the two port resistances must be the same. Thus in Fig. 6 we must have $R_1 = R_2$.

4) The realizability conditions expressed by Theorem 1, Section II-A must be respected.

The requirements imposed by the first three principles are easy to comply with. If they are satisfied we say that the building blocks are *port-wise* interconnected and that two individual ports then merged are *compatibly* connected. The fourth principle, however, has far-reaching consequences. By construction, adaptors do not contain internal directed loops, but usually a directed path from every input terminal to every output terminal. Nevertheless, no delay-free directed loops can be created if a capacitance, an inductance, a resistance, a resistive source, or a unit element (Tables 1 and 2) is connected to an adaptor port. A gyrator (Table 2), a circulator (Table 4), or a transformer realized according to Table 3B is permitted as long as it remains guaranteed that a delay-free directed loop is not created by the termination at the other end(s). A QUARL does not create a delay-free directed loop either except, possibly (although nowhere necessarily), if one of the delays T_{21} and T_{12} is zero; its use does not, in general, violate

the second condition of Theorem 1 either since the sum $T_{21} + T_{12}$ is equal to T .

On the other hand, connection of a short circuit, an open circuit, or a voltage source (Table 1) is, in general, forbidden. Most importantly, the direct interconnection of two adaptor ports (which includes connecting to an adaptor the realization of an ideal transformer according to Table 3C or 3D, see below) will in general create a delay-free directed loop (Fig. 7(a)). Exceptions can only be made if there is an

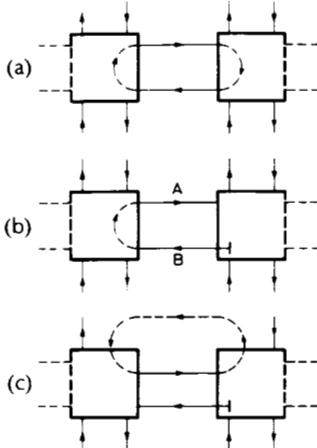


Fig. 7. (a) Creation of a delay-free directed loop by direct interconnection of two adaptor ports. (b) Interruption of this delay-free directed loop by presence of a reflection-free port. (c) Reappearance of a delay-free directed loop via an outer feedback path.

adaptor port that is reflection-free (Tables 5C and 7C). We may always connect to such a port a short circuit, an open circuit, or a voltage source, and even another adaptor (Fig. 7(b)) except if some further delay-free directed loop would be created via some other delay-free path. This latter point is sometimes overlooked and must indeed carefully be checked; as an example it is explained in Fig. 7(c) how a delay-free directed loop may be closed via an outer feedback path. Such a situation can, of course, never occur if the block diagram whose blocks are the elements and sources of Section III-A and the adaptors of Section III-B forms a tree-like structure, although bridged configurations are not excluded by necessity.

An interesting condition can be given that is necessarily satisfied if there is no delay-free directed path from an input to an output terminal at a given port. Consider, e.g., a port interconnection in the reference-filter domain (Fig. 8(a)) and the corresponding interconnection in the WDF domain (Fig. 8(b), cf. also Fig. 7(b)). If there is no delay-free directed path to the right of the interconnecting port in Fig. 8(b) the transmission must become zero if all delays are

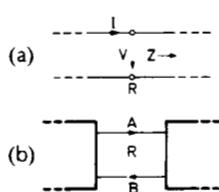


Fig. 8. (a) A port interconnection in the reference domain. (b) The corresponding port interconnection in the WDF domain.

interrupted. In other words, we must have $B = 0$ for $A \neq 0$ and $z = \infty$, thus $\psi = 1$ (cf. (2)). Due to (6b) this implies $V = RI$, thus

$$Z(1) = R \quad (54)$$

or, equivalently, that the corresponding reflectance is zero [99], $Z = Z(\psi) = V/I$ being the input impedance to the right of the interconnecting port in the original circuit (Fig. 8(a)), and R the port resistance of that port. We like to stress, however, that (54) is only necessary, not sufficient, contrary to what is sometimes believed, although in many cases absence of delay-free directed loops is indeed guaranteed by (54). On the other hand, arrangements satisfying (54) have appeared in the literature although it had been overlooked that realizability is not given. In such cases, there is in fact more than one delay-free directed path, but with cancellation of the corresponding transfer functions occurring.

As a first very simple application of the principles exposed above we consider again the realization of an ideal transformer. It is well known that the ideal transformer of Table 3A is equivalent to the chain of gyrators shown in Fig. 9(a), with $n = R_2/R_1$. For the sake of clarity we have repre-

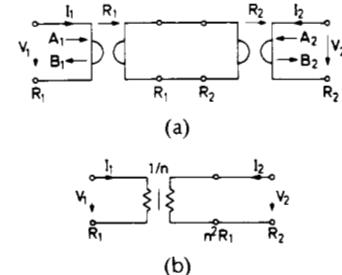


Fig. 9. (a) Equivalent circuit for the ideal transformer of Table 3A, involving two gyrators with $R_2/R_1 = n$. (b) Representation of the same ideal transformer with an auxiliary port of port resistance $n^2 R_1$ inserted, no specific relationship between R_1 , R_2 , and n being assumed.

sented there the interconnection as a two-port with port resistances R_1 and R_2 , respectively, corresponding to what we have done in Table 5A. (We could also simply indicate a single port, with distinct left and right port resistances.) In the wave-flow diagram this interconnection becomes a two-port parallel adaptor, and the two gyrators can be realized as explained in Table 2. The result is the transformer realization of Table 3C. Compared to the one of Table 3B it has the advantage of requiring only one multiplier, and the disadvantage of excluding an interconnection with an adaptor port that is not reflection-free. Finally, for the ideal transformer of Table 3A we can also introduce an auxiliary port of port resistance $n^2 R_1$, as shown in Fig. 9(b), which leads to the realization of Table 3D; it does not require any relationship to exist between R_1 , R_2 , and n .

Notice a principle which we have respected when representing the circuits of Tables 3C and 3D and which we will follow later on: If it is required to indicate port resistances for wave ports we will do this only at those places where this appears to be helpful for proper understanding. Thus in Table 3C, the port resistance at the input port of the overall arrangement has the same value R_1 as that at the input of the two-port adaptor; it is therefore not indicated separately, and the situation is similar at the output port. On

the other hand, in the arrangement of Table 3D there is a change of port resistance from R_1 to $n^2 R_1$, and both these values have therefore been given (although this was not strictly required since the passage from one port resistance to the other is imposed by the multipliers n and $1/n$ appearing in the circuit).

B. Reflectances and Transmittances

Before going into detail about how to realize specific circuits we want to explain a few general aspects about the transfer functions encountered.

Consider first a classical one-port N (Fig. 10(a)), and assume that we have been able to derive from it a wave one-port N' (Fig. 10(b)). We assume N to be fed by a

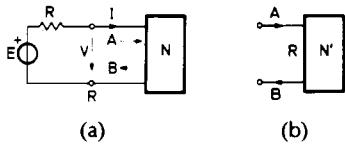


Fig. 10. (a) A classical one-port N fed by a resistive source, the external port resistance being chosen equal to the terminating resistance. (b) The corresponding WDF one-port.

resistive source of source voltage E and resistance R , and we select the *external* port resistance (i.e., the port resistance at the accessible port) to be equal to R . (Observe that since confusion cannot arise, we have chosen in Fig. 10(b) to represent source and sink with the usual symbols for terminals and not the ones shown in Table 1; the same principle will usually be followed hereafter.) For the transfer function

$$H = B/A$$

of N' we obtain in view of (6)

$$H = (V - RI)/(V + RI) = (Z - R)/(Z + R) \quad (55)$$

where $Z = V/I$ is the impedance of N . Thus H is equal to the reflection coefficient, or simpler, the *reflectance* of N (which is obvious in view of our use of wave quantities). Consequently, if N is a *reactance* (lossless circuit), H is an all-pass function. The realization of reactances and that of all-pass functions are thus two equivalent tasks, or else, any realization of a reactance can serve as realization of an all-pass function and *vice versa*.

Consider next a classical two-port N between resistive terminations (Fig. 11(a)). For the sake of generality we assume both these terminations to comprise not only resis-

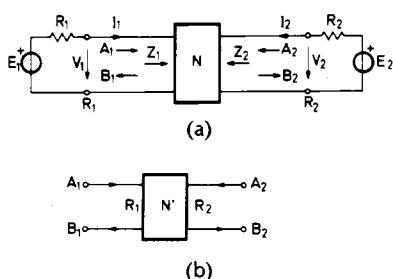


Fig. 11. (a) A classical two-port N inserted between resistive terminations, the external port resistances being chosen equal to the respective terminating resistances. (b) The corresponding WDF two-port.

tances (R_1 and R_2 , respectively) but also voltage sources (E_1 and E_2 , respectively). Let the external port resistances (i.e., the port resistances at the accessible ports) be chosen equal to the respective terminating resistances, and assume that we have derived from N a wave two-port N' (Fig. 11(b)). The entries of the scattering matrix

$$\mathbf{S} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix}$$

are known [32] to be given by

$$S_{11} = (Z_1 - R_1)/(Z_1 + R_1) \quad (56a)$$

$$S_{22} = (Z_2 - R_2)/(Z_2 + R_2) \quad (56b)$$

$$S_{21} = 2\sqrt{R_1/R_2} V_2/E_1|_{E_2=0} \quad (56c)$$

$$S_{12} = 2\sqrt{R_2/R_1} V_1/E_2|_{E_1=0} \quad (56d)$$

where Z_1 and Z_2 are the input impedances at port 1 (for $E_2 = 0$) and port 2 (for $E_1 = 0$), respectively. Clearly, S_{11} and S_{22} are the reflectances at ports 1 and 2, respectively, while S_{21} is the transmittance already considered in (7) and S_{12} is the transmittance for the opposite direction of transmission.

On the other hand, according to (6), we have

$$A_1 = V_1 + R_1 I_1 \quad (57a)$$

$$A_2 = V_2 + R_2 I_2 \quad (57b)$$

$$B_1 = V_1 - R_1 I_1 \quad (57c)$$

$$B_2 = V_2 - R_2 I_2 \quad (57d)$$

and, therefore (cf. Fig. 11(a)),

$$A_1 = E_1$$

$$A_2 = E_2$$

$$B_1|_{E_1=0} = 2V_1$$

$$B_2|_{E_2=0} = 2V_2.$$

Expressing B_1 and B_2 in terms of A_1 and A_2 , we can write general equations of the form

$$B_1 = S_{11} A_1 + S_{12} A_2 \quad (58a)$$

$$B_2 = S_{21} A_1 + S_{22} A_2 \quad (58b)$$

and it can thus be verified that (cf. also (7) and (8))

$$S_{11} = S_{11} \quad S_{22} = S_{22} \quad (59)$$

$$S_{21} = S_{21}/K \quad (60a)$$

$$S_{12} = K S_{12} \quad (60b)$$

$$K = \sqrt{R_1/R_2}. \quad (60c)$$

Between the (power-wave) scattering matrix \mathbf{S} and the voltage-wave scattering matrix

$$\mathbf{S}' = \begin{pmatrix} S'_{11} & S'_{12} \\ S'_{21} & S'_{22} \end{pmatrix} \quad (61)$$

we thus have the well-known relationship

$$\mathbf{S}' = R^{1/2} \mathbf{S} R^{-1/2} \quad (62)$$

where

$$\mathbf{R} = \begin{pmatrix} R_1 & 0 \\ 0 & R_2 \end{pmatrix}. \quad (63)$$

Clearly, according to (61), S'_{21} and S_{21} differ only by a

constant, i.e., frequency-independent factor K (cf. Section II-C), i.e., they correspond to precisely the same general type of filter even if $R_2 \neq R_1$, and the same applies to S_{12} and S_{21} .

As is well known [32], if N is lossless we have, for $p = j\omega$ (thus for $\psi = j\phi$)

$$S^* S = 1 \quad (64)$$

where S^* is obtained from S by transposing it and replacing its entries by their complex conjugate. (This can also be verified by means of above relations, using for the power absorbed by N the expression $P = \text{Re}(V_1 I_1^* + V_2 I_2^*)$.) One consequence of (64) are the relations (also known as Feldtkeller equations)

$$|S_{11}|^2 + |S_{21}|^2 = 1 \quad (65a)$$

$$|S_{22}|^2 + |S_{12}|^2 = 1. \quad (65b)$$

Considering (65a) we see that

$$|S_{21}| = 1 \Leftrightarrow S_{11} = 0 \quad S_{21} = 0 \Leftrightarrow |S_{11}| = 1 \quad (66)$$

and also that $|S_{11}| \leq 1$ for all real frequencies. Thus S_{11} also behaves like a transfer function of a passive circuit and in fact is complementary to S_{21} . Frequencies in the passband of S_{21} fall into the stopband of S_{11} and vice versa. Thus if, e.g., S_{21} corresponds to a low-pass filter then S_{11} corresponds to a high-pass filter and vice versa, and if S_{21} corresponds to a band-pass filter then S_{11} corresponds to a band-stop filter, and vice versa. The situation is similar, of course, for S_{12} and S_{22} .

In classical circuits it is difficult to take advantage of this possibility since reflected signals are not easily accessible in an accurate fashion. For a WDF two-port, however, we conclude from Fig. 11(b) that we actually have available two input signals and two output signals. For a usual filter application we will employ just one of the input signals, say A_1 , and one of the output signals, say B_2 (or alternatively A_2 and B_1). However, we may equally well use, e.g., both input signals and one of the output signals, or one input signal and both output signals, in which case we thus obtain automatically a *branching* (directional filter) [72], [100]–[102]. This can imply considerable savings since in actual systems arrangements branching filters are often required, or else, the arrangements can appropriately be chosen in such a way that branching filters can be accommodated.

It would be wrong, however, to assume that in such cases the second transfer function in a branching filter can be obtained fully without extra cost. Indeed, the usual maximum passband loss tolerated, say for S_{21} , leads according to (65a) to a minimum stopband loss for S_{11} which is far lower than what is commonly needed, while the minimum stopband loss for S_{21} leads in the same way to a maximum passband loss for S_{11} which is far better than required. Or, in classical filter terminology, the minimum return loss required in the passband of a filter is usually much smaller than the minimum forward loss required in the stopband. Thus in order to fulfill both stopband requirements in a WDF branching filter one has to adopt a design for which the passband performances are far better than actually needed.

Observe that for a reciprocal two-port N ($S_{12} = S_{21}$), S_{12} and S_{21} also differ only by a constant factor, while even in the nonreciprocal lossless case it is known [32] that $|S_{12}| =$

$|S_{21}|$, in which case (65) leads to $|S_{22}| = |S_{11}|$. Thus S_{12} can in practice be used just as well as S_{21} , and S_{22} just as well as S_{11} . On the other hand, one can envisage applications [103] where all four input and output terminals of a WDF two-port are actually used.

V. REALIZATION OF REACTANCES AND ALL-PASS FUNCTIONS

A. Richards and Foster Structures

As will be seen, any of the classic canonic structures can be used for selecting the reference structure. The reactance structure which in some respect is the simplest one is the chain connection of unit elements (although this structure is less widely known than the others). According to Richards [90], any reactance function $Z = Z(\psi)$ of degree $n \geq 1$ can be synthesized as a chain of n unit elements (all of delay $T/2$ and positive characteristic impedances R_1 to R_n) terminated at the far end either by an open circuit (if $Z(0) = \infty$, Fig. 12(a)) or by a short circuit (if $Z(0) = 0$, Fig. 12(b)). Choosing port resistances as indicated in Fig. 12(a) and (b), with $R_0 = R_1$, and using the result in the first

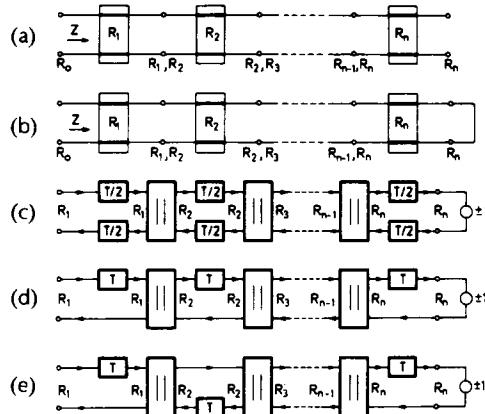


Fig. 12. (a) Realization of a reactance $Z = Z(\psi)$ as chain of unit elements in the case $Z(0) = \infty$. (b) Corresponding realization for $Z(0) = 0$. (c) Resulting WDF structure, the upper sign in ± 1 (terminating branch) having to be chosen for (a), and the lower sign for (b); the structure is obtained by selecting R_0 equal to R_1 . (d) and (e) Two arrangements equivalent to that of (c), obtained either by using appropriate QUARLS instead of unit elements or by applying the equivalence of Fig. 13.

column of Table 2 as well as that of Subsection III-B2, the WDF realization of Fig. 12(c) is immediately obtained, $+1$ having to be adopted in the termination for the arrangement of Fig. 12(a) and -1 , for that of Fig. 12(b). It is easily verified that no forbidden, delay-free directed loops appear in the arrangement of Fig. 12(c) and that this arrangement can be connected to any adaptor port (with port resistance R_1) without creating such forbidden loops. Observe that according to the Richards procedure [90] we have $R_1 = Z(1)$. This is in agreement with the previous discussion concerning (54).

Since the chain matrix of a QUARL (second column in Table 2) differs from that of a unit element only by the factor $e^{j\Delta}$, it is easily verified that in the realizations of Fig. 12(a) and (b) one may replace anyone of the unit elements

by a QUARL of average delay $T/2$ and of unchanged characteristic impedance. In other words, for the pair of branches between any two consecutive adaptors the total delay T may be divided up in an arbitrary fashion. Two extreme such possibilities are shown in Fig. 12(d) (only full delays in the respective forward paths) and in Fig. 12(e) (only full delays, but alternately in the forward and backward path, the drawing being made for n odd). The same result can be obtained if instead of using QUARLs we take advantage of the general equivalence shown in Fig. 13

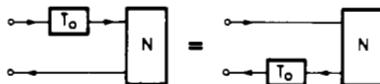


Fig. 13. A simple equivalence involving an arbitrary delay T_0 and an arbitrary circuit N .

where T is an arbitrary delay and N an arbitrary circuit [69]. Indeed, applying this equivalence consecutively to appropriate ports in Fig. 12(c) (with N then corresponding to the entire circuit to the right of the port under consideration) it is easily seen that in particular the arrangements of Fig. 12(d) and (e) can indeed be obtained. Clearly, if we choose R_0 different from R_1 , the structures in Fig. 12(c)–(e) have to be preceded by a further two-port adaptor. Note that the resulting structures could, of course, be obtained directly (thus without first deriving the structures of Fig. 12(a) or (b)) simply after replacing ψ by z . In that sense, the Richards algorithm is equivalent to a Schur parametrization [104]–[107].

It is important to notice that the total delay in all realizations such as those of Fig. 12(c), (d), and (e) is the same, i.e., equal to nT . Concerning the *total amount of storage* to be provided, all such realizations are thus equivalent (contrary to a frequently expressed opinion that Fig. 12(c) implies double the amount of storage since it contains double the number of delay elements; one may indeed use the same storage location alternately for a delay $T/2$ in the forward path and the corresponding delay in the backward path, respectively). In fact, there are frequently good reasons for preferring a structure such as that of Fig. 12(c) over those of Fig. 12(d) and (e). To understand this, let us consider in any given signal-flow diagram all delay-free directed paths leading from an input terminal or the output of a delay element to an output terminal or the input of a delay element. We call a *critical path* any one of the paths just considered which involves the largest number of multipliers [108]. Clearly, in Fig. 12(d) the critical path traverses n multipliers, in Fig. 12(e) it traverses 2, but in Fig. 12(c) only 1 (although it should be mentioned that only half as much time is available for carrying out the computations in a critical path of Fig. 12(c) compared to Fig. 12(e)).

Observe that the input impedance seen from the left in the last element in Fig. 12(a) and (b) is equal to R_n/ψ and ψR_n , respectively, i.e., this last element may be replaced by an inductance and a capacitance, respectively. This is what we have done for the equivalences, shown in Tables 11B and 12B, of the parallel and series resonant circuits of Tables 11A and 12A, respectively. Applying to these circuits the same principles as before and making again use of the equivalence of Fig. 13, the WDF realizations given in Tables 11D and 12D, respectively, are obtained.

Table 11 A: A Parallel Resonant Circuit. B: An Equivalent Circuit Involving a Unit Element of Delay $T/2$. C and D: Two Corresponding WDF Realizations Without Delay-Free Directed Path from Input to Output Terminal, C Being Derived from A, and D from B.

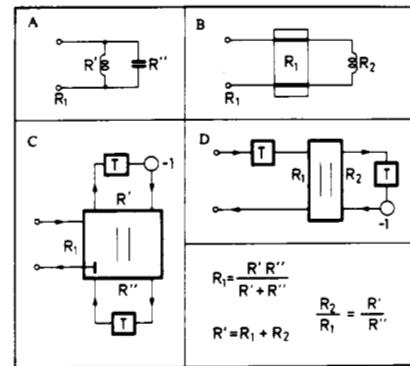
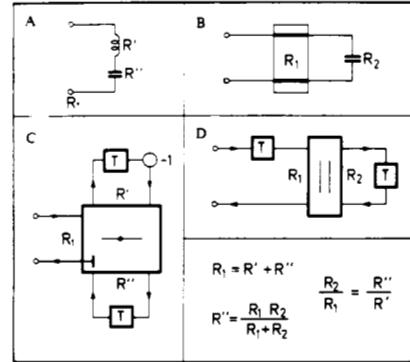


Table 12 A: A Series Resonant Circuit. B: An Equivalent Circuit Involving a Unit Element of Delay $T/2$. C and D: Two Corresponding WDF Realizations Without Delay-Free Directed Path from Input to Output Terminal, C Being Derived from A, and D from B.



We may also consider the parallel resonant circuit of Table 11A as a parallel connection of the input port with two ports terminated by a capacitance and an inductance, respectively. Thus making use of a three-port parallel adaptor, the WDF realization of Table 11C is easily derived, and, using a three-port series adaptor, the same holds true for the WDF realization of Table 12C in the case of the series resonant circuit of Table 12A. In both instances, the external port resistance has been chosen in such a way that in the corresponding adaptor the external port becomes reflection-free, i.e., that no delay-free directed path is present leading from the input to the output terminal, just as for the other realizations discussed before. All WDF realizations of Tables 11 and 12 can thus be connected to any adaptor port without creating delay-free directed loops. (This assumes, of course, that the external port resistance is not imposed by some other constraint; examples of how this aspect can be handled will be seen later.)

The equations listed in Tables 11 and 12 are easily verified. The realizations in Tables 11C and 12C require four adders (cf. Tables 6B and 8B), while those of Tables 11D and 12D require only three. On the other hand, all realizations involve only one multiplier, in particular either γ' or γ'' for Tables 11C and 12C, and either γ_1 , γ_2 , or γ for Tables 11D and 12D. For these coefficients we have, for Tables 11C and 12C, respectively,

$$\gamma' = R_1/R' \quad \gamma'' = R_1/R''$$

and

$$\gamma' = R'/R_1 \quad \gamma'' = R''/R_1$$

and for Tables 11D and 12D

$$\gamma_1 = 2R_2/(R_1 + R_2)$$

$$\gamma_2 = 2R_1/(R_1 + R_2)$$

$$\gamma = (R_1 - R_2)/(R_1 + R_2).$$

The following relationships can thus be shown to hold for Tables 11 and 12:

$$\gamma_1 = 2\gamma'' = 1 - \gamma \quad \gamma_2 = 2\gamma' = 1 + \gamma. \quad (67)$$

Since γ_1 and γ_2 are thus twice γ'' and γ' , respectively, a realization by means of one of the former two coefficients requires a shorter wordlength. For the resonant frequency, we find for Tables 11A and 12A

$$\phi_0^2 = R''/R'.$$

For any of the choices available the multiplier coefficient is thus uniquely determined by ϕ_0 ; we obtain for Table 11

$$\gamma' = \gamma_2/2 = \phi_0^2/(\phi_0^2 + 1) \quad (68a)$$

$$\gamma'' = \gamma_1/2 = 1/(\phi_0^2 + 1) \quad (68b)$$

$$\gamma = (\phi_0^2 - 1)/(\phi_0^2 + 1) \quad (68c)$$

and for Table 12

$$\gamma' = \gamma_2/2 = 1/(1 + \phi_0^2) \quad (69a)$$

$$\gamma'' = \gamma_1/2 = \phi_0^2/(1 + \phi_0^2) \quad (69b)$$

$$\gamma = (1 - \phi_0^2)/(1 + \phi_0^2). \quad (69c)$$

So far we have always assumed that at the external port no delay-free directed path from the input to the output terminal was allowed. There are important situations in which such a restriction does not exist, but where the value of the port resistance, R_0 , at the external port is imposed by some other requirement. Clearly, it is then sufficient to make the transition from R_0 to R_1 by having the WDF realizations in Fig. 12 and Tables 11 and 12 be preceded by a corresponding two-port adaptor (Table 10, with R_1 and R_2 replaced by R_0 and R_1 , respectively). This does not create any immediate delay-free directed loop, not even for the arrangements of Tables 11C and 12C (although one has to make sure that such loops do not appear in conjunction with the remaining part of the circuit to which the arrangement under consideration will be connected, cf. Fig. 7(c)).

In view of their particular importance, the resulting complete arrangements for a capacitance (Table 13A) and an inductance (Table 13D) are shown in Table 13B and E, respectively. In Table 13C is given a further realization of the capacitance of Table 13A; it can be obtained by means of the equivalence explained in Fig. 14, or by means of those given in Figs. 43 and 44(a) to be discussed in Subsection VI-E1. A corresponding WDF realization of the inductance of Table 13D is given in Table 13F. The advantage of having thus in each case two WDF realizations available will be discussed in Sections VII-C and VII-D.

For the sake of later usage let us still consider the signals A_b , A_c , A_e , and A_f that are being multiplied by γ in the arrangements of Table 13B, C, E, and F, respectively. The

following expressions can be shown to hold:

$$A_b = A_0(z - 1)/(\gamma - z) \quad (70a)$$

$$A_c = A_0(z + 1)/(z - \gamma) \quad (70b)$$

$$A_e = -A_0(z + 1)/(z + \gamma) \quad (71a)$$

$$A_f = A_0(z - 1)/(z + \gamma) \quad (71b)$$

thus, in view of (2),

$$A_b/A_c = A_f/A_e = -\psi. \quad (72)$$

It can be verified that for real frequencies, i.e., for $|z| = 1$, we obtain from (70) and (71), taking into account (49),

$$|A_b/A_0| < 2/(1 + \gamma) \quad |A_c/A_0| < 2/(1 - \gamma)$$

$$|A_e/A_0| < 2/(1 + \gamma) \quad |A_f/A_0| < 2/(1 - \gamma)$$

and thus, for $\gamma > 0$, i.e., for $\gamma_1 < 1$

$$|A_b/A_0| < 2 \quad |A_e/A_0| < 2 \quad (73)$$

while for $\gamma < 0$, i.e., for $\gamma_2 < 1$

$$|A_c/A_0| < 2 \quad |A_f/A_0| < 2. \quad (74)$$

These expressions are also of relevance if the two-port adaptor is realized according to Table 10C (or the corresponding realization involving γ_2). Indeed, except possibly for a change of sign, the signal to be multiplied by γ_1 or γ_2 is also given by A_b , A_c , A_e , or A_f depending on whether Table 13B, C, E, or F is used. In particular, by making the appropriate choice it is thus always possible to make sure that the modulus of the signal at the multiplier input is ≤ 2 [109], [110].

Observe also that for $\gamma > 0$, thus for $\gamma_1 < 1$, the choice

Table 13 A and D: Capacitance and Inductance, Respectively, with Resistive Parameter R_1 Different from Port Resistance R_0 . B and E: Corresponding Directly Obtained WDF Realizations. C: Realization of A Obtained by Applying to A the Transformation of Fig. 14 (or to B those of Figs. 43 and 44(a)). F: Corresponding Realization of D.

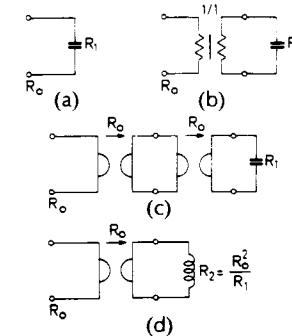
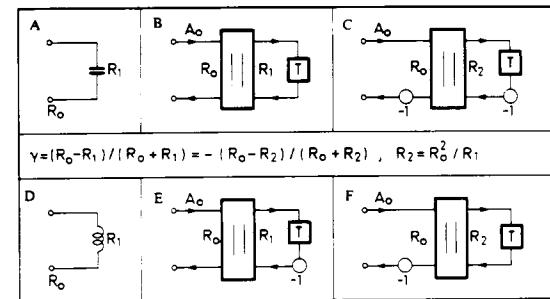


Fig. 14. (a) to (d) A capacitance and three consecutive equivalent arrangements, (d) serving for deriving Table 13C.

between γ and γ_1 can always be made in such a way that the coefficient actually used does not exceed the value $\frac{1}{2}$ (cf. (67)). The same conclusion holds for the choice between γ and γ_2 if $\gamma < 0$, thus $\gamma_2 < 1$, except that it now applies to the modulus of the coefficient actually used. Hence, if we designate by A_b , A_c , A_e , and A_f , the signals immediately after carrying out the multiplication involving A_b , A_c , A_e , and A_f , respectively, the appropriate choice of the multiplier coefficient leads, for $\gamma > 0$, to

$$|A_b/A_0| < 1 \quad |A_e/A_0| < 1 \quad (75)$$

and, for $\gamma < 0$, to

$$|A_c/A_0| < 1 \quad |A_f/A_0| < 1. \quad (76)$$

Such aspects are obviously of interest for scaling considerations. They will further be examined in Section VII.

For the arrangements of Tables 11C and 12C, rather than proceeding as explained four paragraphs earlier, we may just as well replace R_1 in the three-port adaptors by R_0 . In that case, one has, of course, to use unconstrained adaptors instead of constrained ones, and one is then, in fact, dealing with a special case of the general method described hereafter.

A second possibility of realizing a general reactance function is indeed by means of either the first or the second *canonic structure of Foster* (Fig. 15(a), (b)). In the first case,

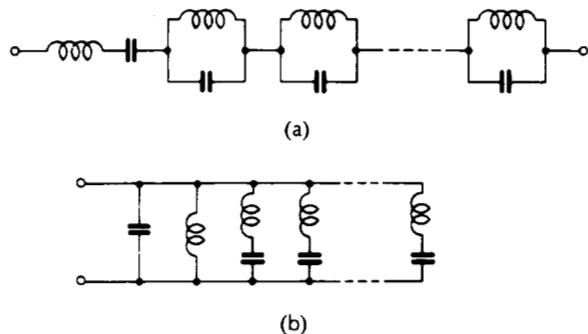


Fig. 15. (a) and (b) First and second canonic structure of Foster for realizing general reactances.

one needs a series adaptor, in the second, a parallel adaptor. In particular, the parallel resonant circuits in Fig. 15(a) can be realized according to Table 11 and the series resonant circuits in Fig. 15(b), according to Table 12. An example of a simple circuit according to Fig. 15(b) is given in Fig. 16(a). The corresponding WDF realization, which in some respect is the simplest one available, is shown in Fig. 16(b), R_1 and R_2 being as given in Table 12. No particular specification has been indicated for R_0 , but if one chooses

$$1/R_0 = 1/R'_0 + 1/R''_0 + 1/R_1$$

there will be no delay-free directed path from the input to the output terminal of the external port. It should be clear how Fig. 16(b) generalizes if there is an arbitrary number of shunt branches consisting of series resonant circuits in Fig. 16(a).

One of a quite large number of realization alternatives to that of Fig. 16(b) is shown in Fig. 16(c), its realizability being ensured by the left port in the series adaptor being reflection-free. As explained in relation to Table 12C and D, it requires one more adder and slightly less convenient multiplier coefficients. Furthermore, as explained earlier in rela-

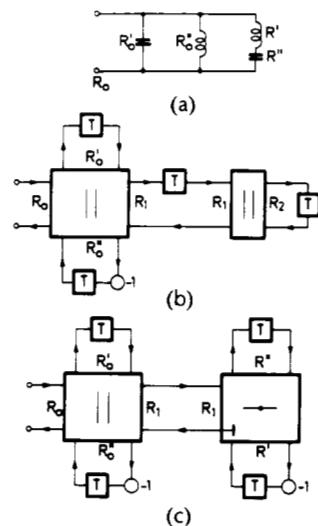


Fig. 16. (a) A simple structure according to Fig. 15. (b) and (c) Two corresponding WDF realizations, with (b) usually to be preferred.

tion to Fig. 12, we can divide up the delay T located between the two adaptors in Fig. 16(b), using the equivalence of Fig. 13, into, e.g., two delays $T/2$, one in the upper and one in the lower branch. In this case, there is no critical path involving more than one multiplier, while in Fig. 16(c) there is unavoidably such a path traversing two multipliers.

B. Cauer Canonic Structures and Corresponding Structures Using Unit Elements

There exist essentially two types of *Cauer canonic structures*, shown in Fig. 17(a) and (b), respectively, both being in fact *ladder* structures. Notice that the first inductance is

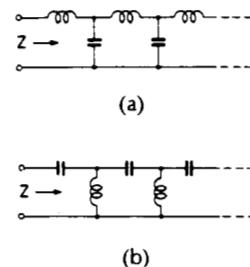


Fig. 17. The two types of Cauer canonic structures; (a) is drawn for Z having a pole at infinity and (b) is drawn for Z having a pole at zero.

missing in Fig. 17(a) if the impedance Z has no pole at infinite, and the first capacitance is missing in Fig. 17(b) if Z has no pole at zero, but this is of no relevance for our purpose.

As an example of how one can proceed we consider the fifth-order Cauer structure shown in Fig. 18(a). Two corresponding WDF realizations are given in Fig. 18(b) and (c), the former having at the external port no delay-free directed path from the input to the output terminal while the latter allowing one to have an arbitrary port resistance R_0 at the input port. No further explanation will be given at this point, but the procedure to be followed for arriving at Fig. 18(b) and (c) will be apparent after we have discussed the

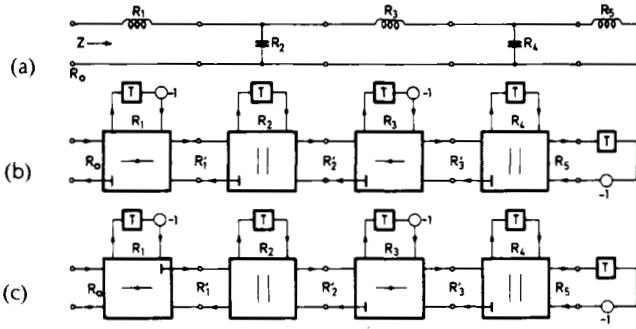


Fig. 18. (a) A fifth-order Cauer reactance structure. (b), (c) Two corresponding WDF realizations; in (b) there is no delay-free directed path from input to output terminal at the external port while in (c) R_0 may be chosen arbitrarily.

realization of ladder WDFs in Section VI-B, where some further aspects of such structures will also be examined. It will then be clear that for Fig. 18(b) we must have

$$R'_3 = R_4 R_5 / (R_4 + R_5) \quad R'_2 = R_3 + R'_3 \quad (77a)$$

$$R'_1 = R_2 R'_2 / (R_2 + R'_2) \quad R_0 = R_1 + R'_1 \quad (77b)$$

while for Fig. 18(c), (77b) has to be replaced by

$$R'_1 = R_0 + R_1. \quad (77c)$$

Two canonic reactance structures that in some respect are intermediary to the Richards and Cauer structures are shown in Fig. 19(a) and (c). (If for the input impedance $Z = Z(\psi)$ one has $Z(\infty) = 0$, Fig. 19(a) applies as it stands while Fig. 19(c) can be used with the first inductance omitted, and if $Z(\infty) = \infty$, Fig. 19(c) applies as it stands while Fig. 19(a) can be used with the first capacitance omitted.) Corresponding realizations are shown in Fig. 19(b) and (d), respectively, where no restriction on the port resistance R_0 of the external port has been assumed. One

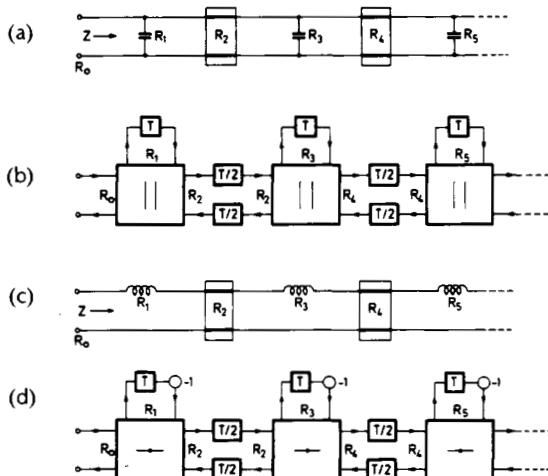


Fig. 19. (a) and (c) Two canonic structures for realizing general reactance functions. (b) and (d) Two corresponding WDF realizations; by appropriate choice of the port resistance R_0 , delay-free directed paths from the input to the output terminal of the external ports can be avoided.

can again ensure no delay-free directed path to lead at that port from the input to the output terminal by choosing $R_0 = R_1 R_2 / (R_1 + R_2)$ or $R_0 = R_1 + R_2$, respectively. For the realizations given in Fig. 19(b) and (d), the critical paths

involve each only one multiplier, just as for the structure of Fig. 12(c). The number of multipliers and the number of adders are also the same in both cases.

C. Chain of Circulator-Type All-Pass Sections

As discussed in Section IV-B, realizing reactances or all-pass functions amounts to the same thing. We may thus also investigate classical realization procedures for functions of the latter type. Mathematically speaking, the simplest such procedure is the chain connection of all-pass sections of degree 1 and 2. Such sections can be obtained by means of three-port circulators terminated at one port by a capacitance or an inductance or by a parallel- or series-resonant circuit. The resulting all-pass structure is as shown in Fig. 20(a) where each of the impedances Z_1 to Z_n is thus of one of the four types just mentioned. In fact, except for a possible sign inversion, one only needs, e.g., impedances corresponding to a capacitance or a parallel-resonant circuit. The corresponding two sections are shown in Fig. 21(a) and (b) and two possible resulting WDF realizations, in Fig. 21(c) and (d), respectively (cf. Tables 4, 11, and 13).

The all-pass two-port in Fig. 20(a) is shown inserted

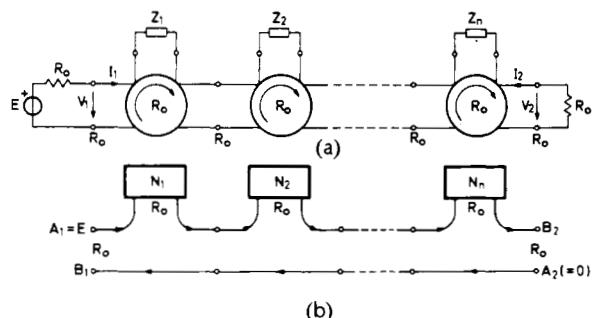


Fig. 20. (a) An all-pass two-port inserted between resistive terminations Z_1 to Z_n being impedances corresponding to a capacitance, an inductance, a parallel resonant circuit, or a series resonant circuit. (b) General structure of the resulting WDF realization, N_1 to N_n corresponding to realizations (not represented in detail) of Z_1 to Z_n , respectively.

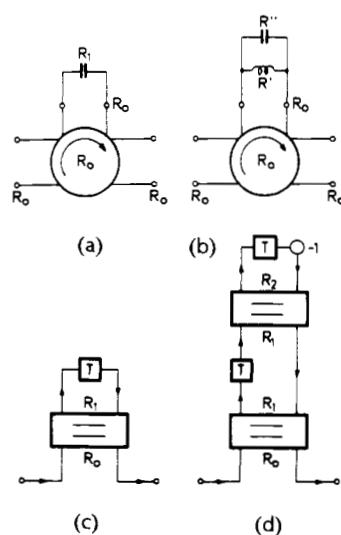


Fig. 21. (a), (b) Basic first- and second-degree all-pass sections. (c), (d) Possible corresponding WDF realizations.

between resistive terminations as discussed in Section IV-B. The corresponding WDF realization is given in Fig. 20(b). The blocks N_1 to N_n represent realizations of Z_1 to Z_n , all details being omitted. Individual blocks may thus become as shown in Fig. 21(c) and (d). In Fig. 20(b) the transmission from A_1 to B_2 corresponds to the desired all-pass transfer function. The through connection from $A_2 (= 0)$ to B_1 is, of course, irrelevant; it has been shown only for the sake of completeness. Note that one may also use impedances Z_1 to Z_n of degree higher than 1 or 2, but this may not be of much advantage. Note also that we have written ($= 0$) next to the input terminal of port 2 in Fig. 20(b); this has been done because there is no source drawn at the termination of port 2 in Fig. 20(a). We proceed similarly in corresponding later situations.

With reference to Fig. 11(a), observe that in Fig. 20(a) we have $R_1 = R_2 = R_0$. This is obviously not altered if we modify any of the element values in Z_1 to Z_n , thus any of the multiplier coefficients in the adaptors contained inside of N_1 to N_n (Fig. 20(b)).

D. Some General Conclusions

We have seen that quite an impressive range of possibilities exists for realizing general reactances, or equivalently, all-pass functions, and further possibilities become available by combining in any suitable fashion the approaches described. Among the choices available, those corresponding to Figs. 12, 19, and 20 are usually the most attractive ones. They offer indeed a very high degree of modularity and parallelism. Other advantages will be seen later in relation with procedures for suppressing parasitic oscillations, etc.

The result mentioned in the last paragraph of Section V-C, applied to the realization of an all-pass transfer function, implies that in the analysis of Section II-C we may set for any multiplier coefficient γ , $\partial a_0 / \partial \gamma = 0$. The same conclusion holds if an all-pass function is realized via any of the reactance structures discussed in Sections V-A and V-B.

VI. MAJOR APPROACHES FOR THE REALIZATION OF FILTERS

A. Lattice Reference Filters

1) Basic Properties of Lattice Wave Digital Filters: WDFs derived from lattice reference filters, are in some respect the most attractive structures available [109]–[133]. A classical lattice two-port inserted between terminations with equal resistances R_0 ($R_1 = R_2 = R_0$, cf. Fig. 11) is represented in Fig. 22, Z' and Z'' being the lattice (or canonic) impedances. In view of (62) and (63), we have $S' = S$, i.e., we do not have to distinguish between the two types of scattering matrices. One finds

$$S_{11} = S_{22} = (S' + S'')/2 \quad (78a)$$

$$S_{21} = S_{12} = (S'' - S')/2 \quad (78b)$$

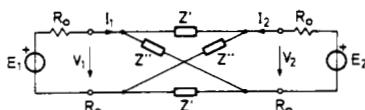


Fig. 22. A symmetrical lattice filter inserted between terminations having equal resistances R_0 .

where

$$S' = (Z' - R_0)/(Z' + R_0) \quad (79a)$$

$$S'' = (Z'' - R_0)/(Z'' + R_0) \quad (79b)$$

S' and S'' being thus the (canonic) reflectances corresponding to Z' and Z'' , respectively. If Z' and Z'' are reactances, as will be assumed unless otherwise stated, S' and S'' are all-pass functions.

A lattice two-port, clearly, is *symmetrical*. On the other hand, if a two-port is symmetrical (in which case $S_{11} = S_{22}$ and $S_{21} = S_{12}$), we can define functions S' and S'' by means of (78). The losslessness requirement (64) can then be shown to imply that S' and S'' are all-pass functions.

Using (78), the scattering equations (58) can be written as

$$2B_1 = S'(A_1 - A_2) + S''(A_1 + A_2) \quad (80)$$

$$2B_2 = S''(A_2 - A_1) + S'(A_1 + A_2) \quad (81)$$

which leads immediately to the WDF realization shown in Fig. 23(a). For $A_2 = 0$, (81) reduces to

$$2B_2 = (S'' - S')A_1 \quad (82)$$

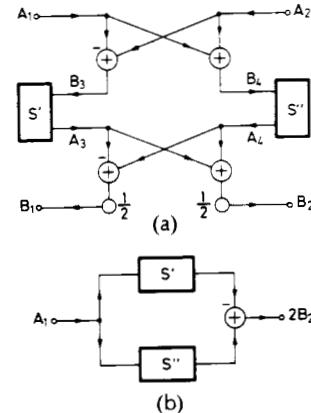


Fig. 23. (a) Wave-flow diagram corresponding to the lattice filter of Fig. 22. (b) simplified wave-flow diagram resulting for $A_2 = 0$. (Signals to be subtracted are marked by a minus sign at the respective adder input.)

and the corresponding simplified realization is given in Fig. 23(b). The structures thus obtained are remarkably simple. For the WDF realization of S' and S'' themselves, any of the methods described in Section V can be used, with the structures of Figs. 12, 19, and 20 to be preferred as explained in Section V-D.

The structure of Fig. 23(a) can also be redrawn as shown in Fig. 24(b). The four-port appearing there will be called a *lattice adaptor*; it is defined by the equations (written for instantaneous quantities)

$$b_3 = a_2 - a_1 \quad b_4 = a_1 + a_2 \quad (83)$$

$$b_1 = (a_4 - a_3)/2 \quad b_2 = (a_3 + a_4)/2 \quad (84)$$

and its symbolic representation as well as its structure are shown in Fig. 25(a) and (b), respectively. Between the interpretation of Fig. 23(a) thus obtained and the original structure there exists a discrepancy in so far as each of the impedances Z' and Z'' appears twice in Fig. 22, but S' and S'' appear only once in Fig. 24(b). A more immediate interpretation is gained if one uses for the lattice structure

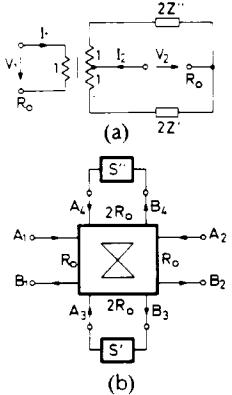


Fig. 24. (a) Jaumann equivalent of the lattice two-port in Fig. 22. (b) Equivalent representation of the arrangement of Fig. 23 (a), using a lattice adaptor.

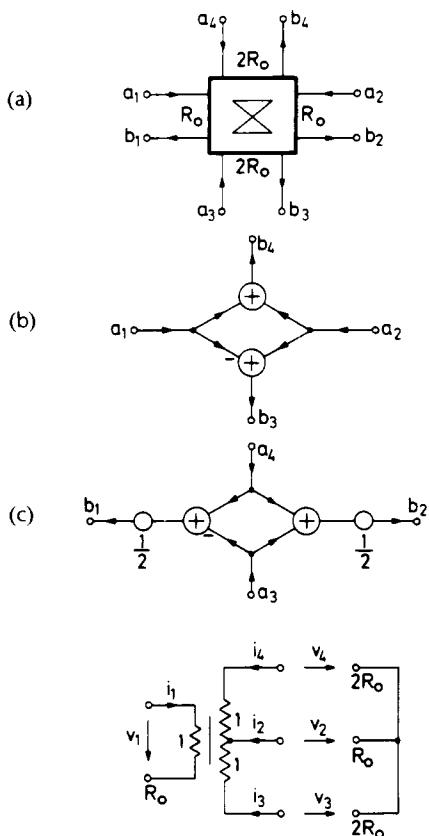


Fig. 25. (a) Representation of a lattice adaptor; (b) its wave-flow diagram. (c) Interconnecting four-port from which the lattice adaptor is obtained as WDF equivalent.

in Fig. 22 its Jaumann equivalent shown in Fig. 24(a). The four-port of Fig. 25(c) is indeed described by the equations

$$v_3 = v_2 - v_1 \quad i_3 = (i_1 - i_2)/2 \\ v_4 = v_1 + v_2 \quad i_4 = -(i_1 + i_2)/2.$$

From these, the relations (83) and (84) are easily obtained if one uses in the defining equations (27) (with $n = 4$) the equalities

$$R_1 = R_2 = R_o \quad R_3 = R_4 = 2R_o.$$

Observe that this way the reflectances of $2Z''$ and $2Z'''$ (cf.

Fig. 24(a)) with respect to $2R_o$ are indeed equal to S' and S'' , respectively, and that it is thus also appropriate to indicate $2R_o$ as port resistances of ports 3 and 4, as we have done in Figs. 24(b) and 25(a) and (c).

Obviously, the input-output relationships in the structures of Fig. 23 do not change if the all-pass functions S' and S'' are realized not by one of the procedures explained in Section V, but by any other one available. In particular, one can also consider using any existing procedure not obtainable via the WDF approach. It is thus not surprising that the structure of Fig. 23(b), first published in 1974, has also recently been examined outside the WDF context [134]. However, the full benefits inherent to the structures of Fig. 23 can only be obtained if the WDF approach is also used for realizing S' and S'' .

2) Computation of a Lattice Wave Digital Filter: Here, we recall briefly the essential steps needed for obtaining S' and S'' . Proofs will be omitted, but these can be found in standard textbooks such as those mentioned earlier [21], [29]–[38].

For the loss α defined by (9) one finds that, for real frequencies (cf. (3)), it is given by an expression of the form

$$\alpha = \frac{1}{2} \ln [1 + |\Psi(j\phi)|^2] \quad (85)$$

where $\Psi = \Psi(\psi)$ is a real odd rational function in ψ . The first step in the design is, therefore, to determine real polynomials $h = h(\psi)$ and $f = f(\psi)$, one of them being even in ψ and the other odd, such that the rational function

$$\Psi = h/f$$

gives rise, via (85), to a function $\alpha = \alpha(\omega)$ that satisfies the loss requirements for the filter. We may assume h and f to be relatively prime.

From h and f , one determines Hurwitz polynomials $g' = g'(\psi)$ and $g'' = g''(\psi)$ such that

$$h + f = g'g'' \quad (86)$$

the $g''*$ notation meaning the paraconjugate of g'' , i.e., since we are dealing with real functions, the function (here: the polynomial) defined by $g''* = g''(-\psi)$, etc. (The factorization of $h + f$ in the form (86) is always feasible.) The reflectances S' and S'' are then given, for h even and f odd, by

$$S' = g'_*/g' \quad S'' = g''*/g'' \quad (87)$$

and, for h odd and f even, by

$$S' = -g'_*/g' \quad S'' = g''*/g''. \quad (88)$$

(Alternatively, S' and S'' may be replaced by $-S'$ and $-S''$, respectively, but this is irrelevant for our purpose.)

The above mentioned determination of h and f amounts to solving a standard filter approximation problem. It is examined in many standard textbooks, in particular in specialized books such as [135], [136]. Simple numerical procedures that are frequently applicable are described in [110], and a very efficient computer program (written in Fortran 77 and adapted to VAX, Cyber, and HP computers) based on this procedure is available [137]. Note that Ψ is, in fact, the so-called characteristic function defined by

$$\Psi = S_{11}/S_{21} \quad (89)$$

for which we obtain, in the case of a symmetrical filter (cf. (78)),

$$\Psi = (S' + S'')/(S'' - S'). \quad (90)$$

3) *Lattice Filters with Bireciprocal Characteristic Function:* A particularly simple situation arises if Ψ is bireciprocal, i.e., such that [116], [124]

$$\Psi(1/\psi) = 1/\Psi(\psi) \quad (91)$$

thus, in view of (90), if

$$S(\psi)S''(1/\psi) = -S(1/\psi)S''(\psi). \quad (92)$$

This is satisfied if

$$S(1/\psi) = \pm S(\psi) \text{ and } S''(1/\psi) = \mp S''(\psi) \quad (93)$$

hold, where either both upper signs or both lower signs have to be chosen. On the other hand, it can be shown that for Ψ satisfying (91) the computational process explained in Subsection VI-A2 leads automatically to reflectances S' and S'' that satisfy (93).

The condition (91) implies that

$$|\Psi(1/j\phi)| = 1/|\Psi(j\phi)|$$

and thus in view of (65a) and (89)

$$1/|S_{11}(j\phi)|^2 = 1 + |\Psi(1/j\phi)|^2.$$

Hence, writing α_{21} for the loss defined by (9) and introducing a further loss parameter α_{11} , defined by

$$\alpha_{11} = -\ln |S_{11}| \quad (94)$$

we can finally conclude that

$$e^{-2\alpha_{21}} + e^{-2\alpha_{11}} = 1 \quad (95)$$

$$\alpha_{11}(\omega) = \alpha_{21}[(\Omega/2) - \omega]$$

$$\alpha_{21}(\omega) = \alpha_{11}[(\Omega/2) - \omega] \quad (96)$$

where

$$\Omega = 2\pi F. \quad (97)$$

The resulting loss curves are thus perfectly complementary as sketched in Fig. 26. In particular, for $\omega = \Omega/4$ we obtain

$$|S_{11}| = |S_{21}| = 1/\sqrt{2}$$

thus corresponding to a loss of 3 dB for α_{21} as well as α_{11} .

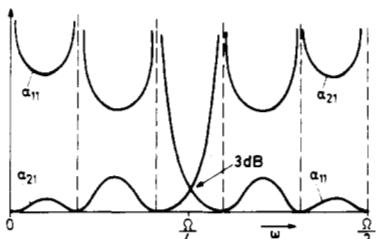


Fig. 26. Illustration of the complementary behavior of the loss responses α_{21} and α_{11} . (Note that the passband maxima should have been drawn lower than the 3-dB crossover point.)

Due to (2), replacing ψ by $1/\psi$ amounts to replacing z by $-z$. Hence, (93) expresses that one of the functions S' and S'' is even in z and the other is odd. Assuming the first of these alternatives (the other is precisely similar), we may write

$$S'(\psi) = \hat{S}(z^2) \quad S''(\psi) = z^{-1}\hat{S}'(z^2)$$

where $\hat{S}'(\cdot)$ and $\hat{S}''(\cdot)$ are real rational functions. Conse-

quently, if one expresses S' and S'' in terms of z , half the coefficients of S' and more than half those of S'' are zero, which amounts to a drastic saving (in addition to that already obtainable by using the circuit as a directional filter). This saving is further doubled if, as is frequently the case in practice [109], [124], [125], [130], [138]–[141], the use of the filter is combined with a doubling or halving of the sampling rate. In this case, S' and S'' are in fact operating at only half the sampling rate first expected, thus at the lower of the two rates involved (cf. Section X-A).

In practice, directional filters are usually of low-pass/high-pass type. It can be shown [103] that if this is the case, all zeros and poles of \hat{S}' and \hat{S}'' turn out to be real and, in fact, negative. If then one uses realizations according to the method explained in Section V-C, only first-order sections are needed, thus structures as those listed in Table 13, and one finds $\gamma < 0$ in the case of Table 13A–C and $\gamma > 0$ in the case of Table 13D–F. In view of the discussion involving (70)–(76), structures according to Table 13C or E should preferably be selected (cf. also Section VII-D). (Observe that at sinusoidal steady state the input signal amplitude is the same for each of the cascaded all-pass sections.) The particular simplicity of the presently discussed filters makes it even possible to compile for these detailed tables from which discretely optimized solutions can directly be obtained [412].

A certain polyphase arrangement, used in particular for an important method of realizing transmultiplexers [142], [143], can be reduced, for two channels, to the general structure of Fig. 23(a) if either only one output (send side) or only one input (receive side) is used. In this sense, the global structure of a lattice WDF with bireciprocal characteristic functions is a special case of a polyphase arrangement for which the branch transfer functions are of all-pass type. It is thus not surprising that it is again advantageous to realize the individual branch transfer functions in a polyphase arrangement by means of WDFs, preferably of all-pass type [144]–[146].

B. LC Ladder Reference Filters

WDFs derived from LC ladder reference filters have first been described in [8]. Two earlier review papers on this subject are [147], [148].

Fig. 27(a) shows a part of a ladder structure, the small rectangles representing the consecutive series and shunt impedances. These may consist of individual one-port elements or, e.g., reactances, as explained in Section V. The arrangement of Fig. 27(a) is redrawn in Fig. 27(b) in order to make apparent the consecutive series and shunt connections (surrounded by dashed squares) of which the structure consists. The impedances referred to before are now shown only in dashed line since we are at present primarily interested in the interconnections themselves. Note that if an orientation has been chosen for one of the ports (e.g., for the one at the extreme left) the orientations of all other ports are fixed by the requirement to be consistent with the conventions adopted in Tables 5A and 7A.

From Fig. 27(b), adaptor arrangements such as those of Fig. 27(c)–(e) are immediately derived. The realizability requirement at adaptor interconnections is satisfied by properly selecting the port resistances of those ports in Fig.

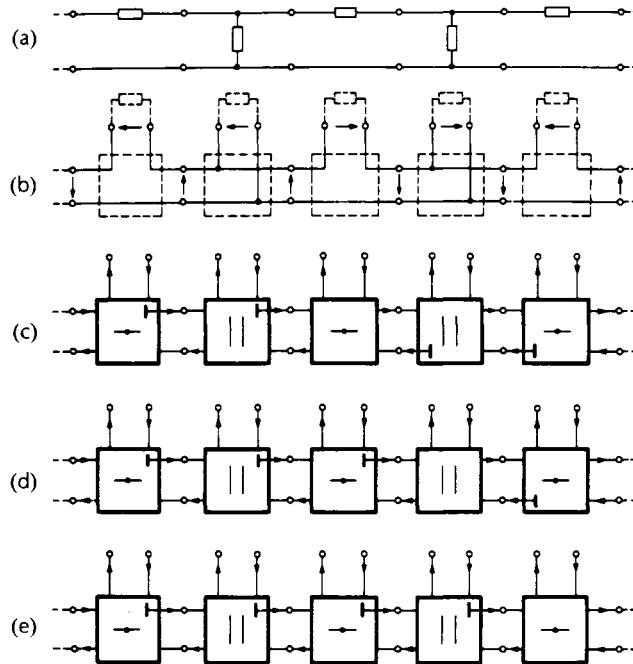


Fig. 27. (a) Part of a ladder structure. (b) The same structure redrawn in order to make apparent the consecutive series and shunt connections. (c) to (e) Three choices for the adaptor arrangement corresponding to the series and shunt connections in (b); the arrangements differ by the location chosen for the unconstrained adaptor.

27(b) which serve to join a series and a parallel interconnection. These ports are not connected to an element or, more generally, an impedance, and thus do not have a port resistance imposed by element values, etc. For those ports,

however, to which an element or an impedance is connected, the port resistance results from the analysis given in Section III-A or, e.g., that in Section V. For such ports, the port resistance is indeed imposed either directly or indirectly by element values if the requirement is respected that there may be no delay-free directed path from the input to the output terminal of the input port in the WDF realization of the reactance under consideration.

In all three structures of Fig. 27(c)–(e) there is precisely one adaptor that is unconstrained, but the structures differ by its selected location. Clearly, more choices are available than the three given, and their total number is dependent on the length of the ladder chain. However, in order to minimize the length of the critical path (cf. Section V-A) the unconstrained adaptor should be located as much as possible in the center of the overall arrangement.

The principles just explained are illustrated in Fig. 28 for a seventh-order low-pass filter. The original *LC* structure is shown in Fig. 28(a), and two resulting WDF structures in Fig. 28(b) and (c). In both cases, the unconstrained adaptor has been placed in the center, thus minimizing the length of the critical path. A further advantage to this, however, is a less asymmetrical impedance level, resulting in a better natural scaling of the filter. These aspects have been overlooked in various publications and, therefore, cannot be overemphasized. Note that the arrangement of Fig. 28(c) may frequently be preferred over that of Fig. 28(b) for the reasons explained in relation with the earlier comparison of the structures in Table 11C and D (and those in Table 12C and D).

In Fig. 28(b) and (c), the resistances R_{i1} and R_{i2} , with $i = 4, 6$, and 8 , are related to R'_i and R''_i in the same way as R_1 and R_2 are related to R' and R'' in Table 11. For R_{10} to R_{15} we obtain, making also use of the notation $G_i = 1/R_i$

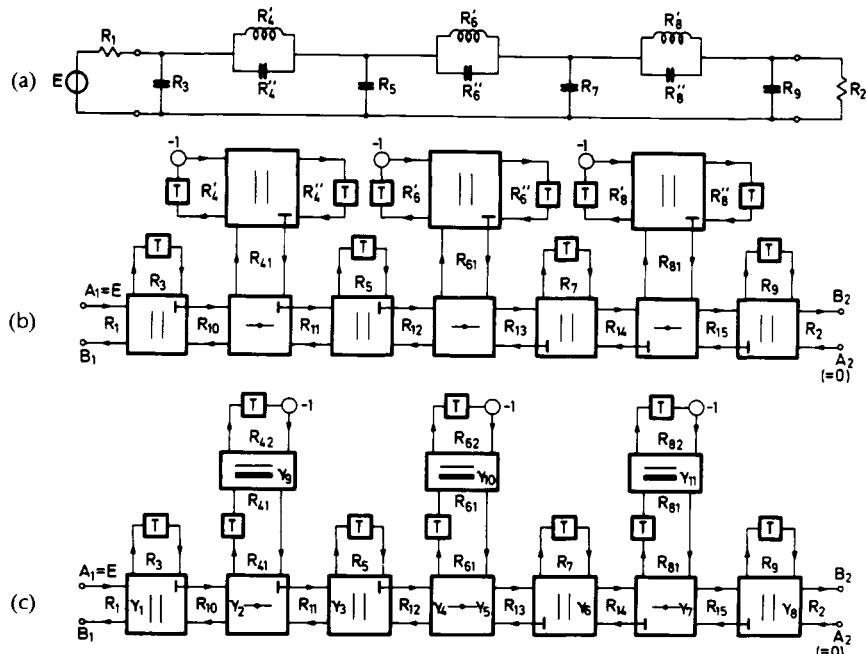


Fig. 28. (a) A seventh-order low-pass ladder filter between resistive terminations. (b) and (c) Two corresponding WDF structures based on the use of Table 11C and D, respectively, the latter being frequently preferred; in both cases the unconstrained adaptor is placed in the center, thus minimizing the length of the most critical path and making the structure as homogeneous as possible.

for any of the i involved,

$$\begin{aligned} G_{10} &= G_1 + G_3 \quad R_{11} = R_{10} + R_{41} \quad G_{12} = G_{11} + G_5 \\ G_{15} &= G_2 + G_9 \quad R_{14} = R_{15} + R_{81} \quad G_{13} = G_7 + G_{14}. \end{aligned}$$

A particularly simple example is that of the third-order low-pass filter shown in Fig. 29. For an optimal design, the reference structure is symmetrical as shown in Fig. 29(a). Now there appears a further advantage of placing the unconstrained adaptor in the center (as has been done in Fig. 29(b)): This unconstrained adaptor has indeed the same

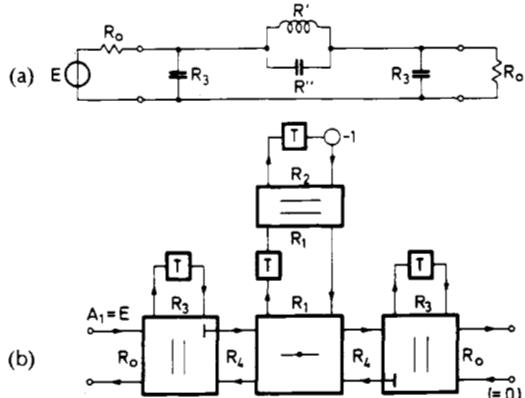


Fig. 29. (a) A symmetrical third-order low-pass filter. (b) The corresponding WDF structure requiring only four multipliers.

port resistance at the left and at the right and can thus be realized in the simplified manner explained in Table 9B. The following relations hold:

$$R_1 = R'R''/(R' + R'')$$

$$R_2 = R_1 R'/R''$$

$$R_4 = R_0 R_3/(R_0 + R_3).$$

Although in the above examples we have considered only low-pass filters, the approach is applicable to any type of ladder structure. The design of the reference ladder filter can, of course, be carried out by any existing approach. If we are dealing with a low-pass filter or a filter reducible (by frequency transformation) to a low-pass filter and if the loss requirements are of common simple type, existing tables (e.g., [37], [149]–[152]) may be used [153].

It should be clear how the principles explained in this section are applicable to structures such as those discussed in relation to Fig. 18. However, while in a filter resistively terminated at both ends there is always one unconstrained adaptor, this is not necessarily the case in Fig. 18. If the left port of the first adaptor in Fig. 18(b) is to be reflection-free, all other adaptors must also have a reflection-free port at their left, and the critical path then has maximal length. A similar situation arises in some other special cases. One of these is the realization of WDFs from ladder reference filters that are resistively terminated at only one end [154], [155] (cf. Section IX-D). Another one is the realization of ladder filters for sampling rate alteration [156] (cf. Section X-A).

For deriving WDFs from ladder reference filters one may also use an approach avoiding the use of adaptors [157]–

[164]. In this case, however, one loses the ease of representing even complicated structures by means of simple block diagrams, of generating the many equivalent structures, of selecting among these the most appropriate one, of making use of transformations such as those that will be explained in Section VI-E, and of ensuring that stability is guaranteed also under finite-arithmetic conditions (cf. Section VII).

C. Some Examples

We first consider WDFs derived from ladder reference filters. The first example of a structure according to Fig. 28, specially designed for a specific application in communications, had been described in [165]. It had been found there that tight specifications could be satisfied by using multiplier coefficients which all, with the exception of one, comprise just 1 nonzero bit, the remaining coefficient comprising 2 nonzero bits.

Frequently, a band-pass filter is required that can be derived from a low-pass filter by the well-known frequency transformation. It is advantageous in this case to make the systems arrangement in such a way that the center frequency becomes equal to one quarter the sampling rate. It is easily verified that application of the corresponding frequency transformation to the LC reference filter amounts to the same as applying the well-known z to $-z^2$ transformation [166] directly to the WDF low-pass structure. Channel band-pass filters for use in a transmultiplexer [124], [139], [140] have been designed according to this principle, adopting the structure of Fig. 28(a) as a low-pass equivalent [117], [167] and realizing the WDF band-pass filter according to Fig. 28(c). The resulting loss responses are shown in Fig. 30(a)–(c), respectively. The loss requirements for the stopband had consecutively been raised as indicated, while for the passband the so-called (1/20)th CCITT requirement [168] had been striven for. The latter is very closely met in all cases despite the remarkably simple coefficient values which had been obtained by discrete optimization. These coefficient values are listed in Table 14; they are given in binary representation or, wherever this leads to a smaller number of nonzero bits, in canonic signed digit (CSD) code [169]. The loss at the reference frequency of 7.2 kHz (corresponding to the CCITT reference frequency of 800 Hz) is equal to 0.1242, 0.1634, and 0.1715 dB, respectively, and the ratios R_2/R_1 are equal to 1, 0.875, and 1.0714, respectively. Note that in all three cases, we have $\gamma_4 = \gamma_5$, i.e., the unconstrained adaptor can be realized according to Table 9B, hence, with just one multiplier. Note also the values $\gamma_{10} = \gamma_{11} = 0$ for Fig. 30(a); as can be concluded from (48), the corresponding adaptors thus reduce to simple through connections.

The extreme simplicity at which we have arrived for the

Table 14 Values of the Coefficients in Fig. 28(c) for which the Transformation $z \rightarrow -z^2$ Gives Rise to the Loss Responses Shown in Figs. 30(a)–(c), Respectively. For Case (a), γ_1 and γ_2 Refer to the Coefficients Complementary to those Indicated in Fig. 28(c).

	γ_1	γ_2	γ_3	$\gamma_4 = \gamma_5$	γ_6	γ_7	γ_8	γ_9	γ_{10}	γ_{11}
a	0.01	0.01	0.01	0.01	0.001	0.01	0.1	0.1	0	0
b	0.01	0.001	0.0001	0.1	0.01	0.100-1	0.1	-0.01	0.100-1	0.01
c	0.0101	0.01	0.0011	0.0011	0.01	0.1	0.100-1	0.01	-0.01	0.100-1

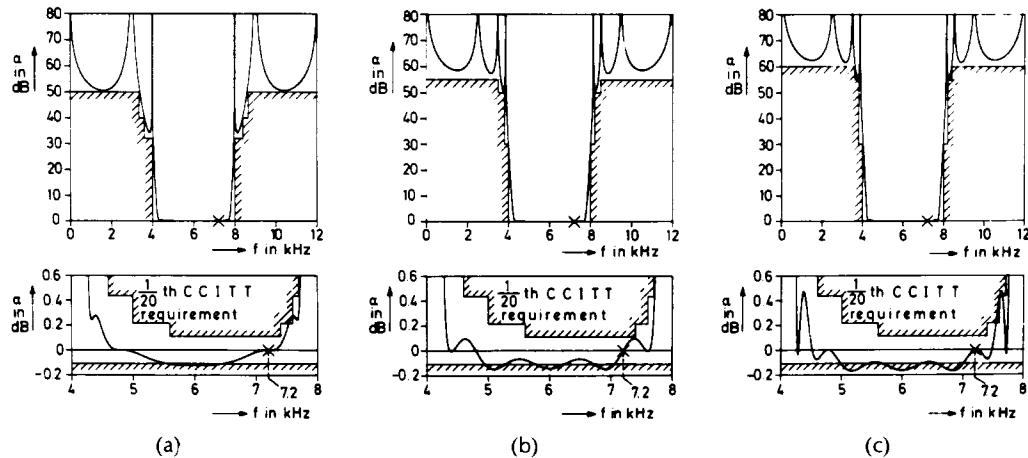


Fig. 30. (a) to (c) Loss responses of band-pass filter derived from Fig. 28(c), with coefficients as listed in Table 14.

coefficients is, of course, only due to the fact that the sensitivity improvement obtainable in the passband goes well beyond what might be expected from a first-order analysis, as has been pointed out in Section II-C. In the stopband, the sensitivity is similarly low as for classical ladder structures. For such structures, each ladder section does indeed contribute only part of the total loss, while the influence of parameter changes upon the loss contributed by a section decreases rapidly if the loss in that section becomes smaller.

In order to obtain best results it is paramount, however, not to ignore the specific WDF realization when computing the reference filter. Thus for the resonant circuits determining the attenuation poles one should not simply adopt those resonant frequencies obtained by the usual optimization procedure. The actual resonant frequencies should indeed be chosen in such a way that coefficients as simple as possible would result. As has been discussed in relation to Tables 11 and 12 (Section V-A) several choices for this are available. The final optimum design of the reference filter should thus be carried out only after the coefficients determining the attenuation poles have been chosen (which usually excludes using tables, but requires procedures more general than those involving, say, elliptic functions, upon which tables are indeed mainly based). After converting the reference filter to a WDF the subsequent discrete optimization will only involve the coefficients appearing, say, in the main chain of adaptors (cf. Fig. 28(b) and (c)). Failure to observe such design principles can be a reason for erroneous conclusions [170].

The situation is somewhat different for *lattice* filters. Due to their high stopband sensitivity such structures are quite useless in the analog domain except if highly stable components, such as quartz crystals, are used or if the attenuation to be achieved is small (equalizers) or even zero (all-pass circuits). The effects due to manufacturing tolerances, temperature changes, and aging would indeed quickly cause intolerable deviations of the stopband loss response. These three types of effects, however, do not play any role in the digital domain (i.e., as long as the proper digital behavior is not affected). Lattice structures are, therefore, perfectly suitable for realizing digital filters. Nevertheless, the dominant sensitivity is now that in the stopband, and the passband

insensitivity may even be better than for ladder structures. The reasons for this are that a lattice filter is automatically symmetrical, i.e., its characteristic function (cf. Section VI-A) is necessarily odd, and that small changes of the multiplier coefficients, therefore, will not prevent the attenuation zeros from actually occurring at real frequencies, contrary to what is almost unavoidably the case for ladder filters. As a consequence, for lattice filters it may hardly be necessary to verify the passband performance during the process of discrete optimization since this performance may remain very satisfactory for all coefficient changes that will not violate the stopband specification.

Altogether, in order to satisfy all loss specifications a lattice WDF will need higher accuracy for its multiplier coefficients. This is compensated for by the fact that the number of multipliers does not exceed the degree of the filter and is thus substantially lower than for an equivalent ladder configuration (except if we are dealing with a so-called polynomial filter, i.e., in the low-pass case, if all attenuation poles are at $\phi = \infty$). The number of adders is also much lower, and a further advantage is due to the possibility of realizing the lattice branches by means of structures offering high degrees of modularity and parallelism as discussed in Section V-D. For the multiplier coefficients themselves, a CSD representation is usually to be preferred.

We first consider a filter with the same requirements as for Fig. 30. Thus the equivalent low-pass filter should be of the same degree as before, i.e., of degree 7, which leads to lattice branches of degree 3 and 4, respectively. The corresponding WDF structures to be used for S' and S'' in Fig. 23 become, after applying the $z \rightarrow -z^2$ transformation, as shown in Fig. 31(a). Clearly, S' has been realized according to Fig. 12, and S'' according to Figs. 20 and 21(d); this had turned out to lead to the most advantageous results. The structure requires only seven multipliers. The CSD multiplier coefficients obtained after optimization are [117]

$$\gamma_1 = 0.1001 \quad \gamma_2 = \gamma_3 = 0.0100 - 1 \quad \gamma_4 = 0.1 \quad (98a)$$

$$\gamma_5 = 0.010 - 101$$

$$\gamma_6 = 0.00100 - 1$$

$$\gamma_7 = 0.10 - 101. \quad (98b)$$

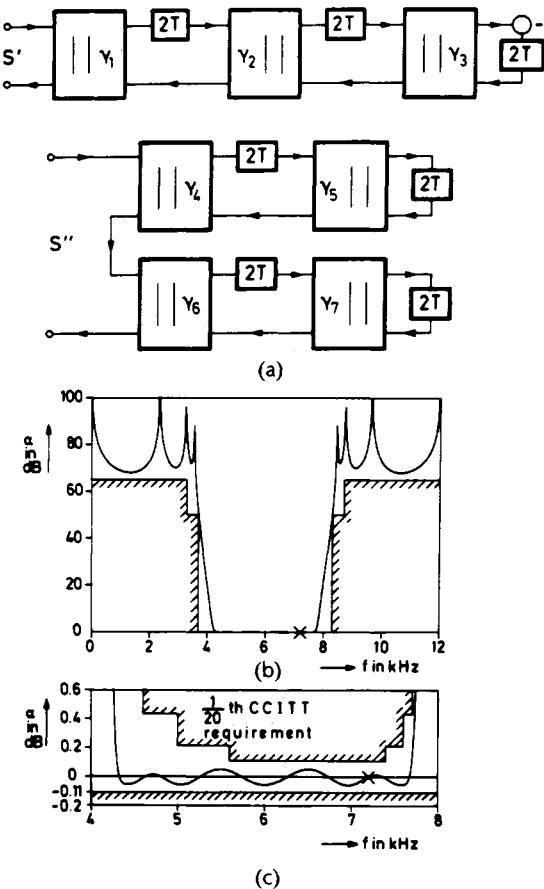


Fig. 31. (a) Realization of the transfer functions S' and S'' (cf. Fig. 23) for a frequency-symmetric lattice band-pass filter designed for a communications application. (b) and (c) Corresponding stopband and passband loss response for coefficient values according to (98). (Note that an error has slipped into the drawing of (a). In order to obtain the result shown in (b) and (c), the transformation $z^2 \rightarrow -z^2$ has still to be carried out, i.e., to all seven delays $2T$ a sign inverter has still to be added in cascade.)

These are still remarkably simple, yet the resulting loss response (Fig. 31(b) and (c)) is very satisfactory.

A second, although particularly simple, example is a low-pass filter of degree 3, for which S' and S'' (cf. Fig. 23) are as shown in Fig. 32(a). This filter had been designed for use in a certain 12-channel transmultiplexer [140]. It had been possible to satisfy the loss requirements (except for very small violations) by means of the very simple coefficients [117]

$$\gamma_1 = 0.1 \quad \gamma_2 = 0.001 \quad \gamma_3 = 0.01. \quad (99a)$$

This filter has been successfully implemented as a custom integrated circuit in NMOS technology using a bit-serial approach [128], [132]. A photomicrograph of this chip is shown in Fig. 33. For further details, including measured results, we refer to [128], [132]. In fact, an even better solution [127] for the given task is

$$\gamma_1 = 0.1000 - 1 \quad \gamma_2 = 0 \quad \gamma_3 = 0.00101. \quad (99b)$$

With these values, there is strictly no violation of the requirements (Fig. 32(b) and (c)). On the other hand, the number of explicit (see below) adders is reduced by 3 (due to $\gamma_2 = 0$) while two implicit (see below) adders are now needed, altogether one adder less than for (99a). Further-

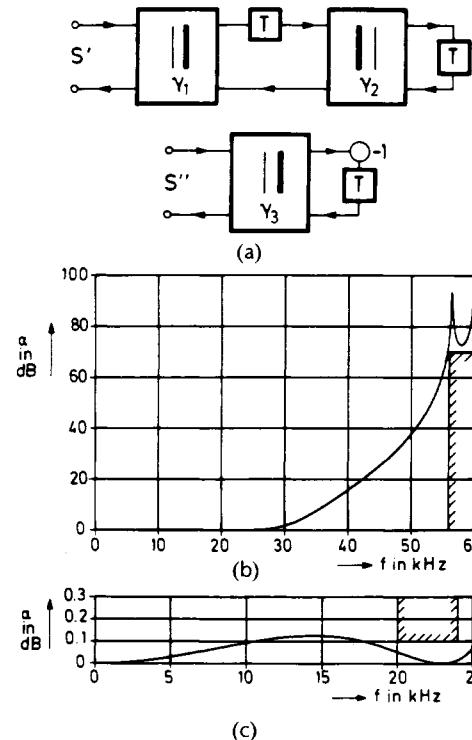


Fig. 32. (a) Realization of the transfer functions S' and S'' (cf. Fig. 23) for a low-pass lattice filter designed for a communications application. (b) and (c) Corresponding stopband and passband loss response for coefficient values according to (99b).

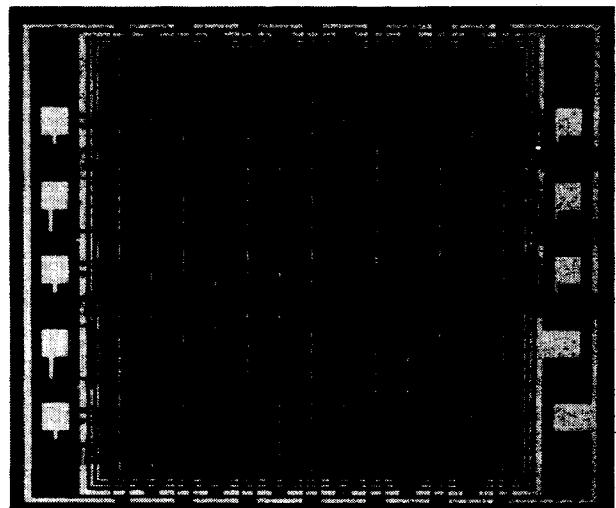


Fig. 33. Photomicrograph of an operational NMOS integrated circuit implementing a filter according to Figs. 23(b) and 32(a), with coefficients given by (99a). (Reproduced with permission of the authors [128], [132].)

more, S' is now of first degree in z^2 , hence the advantages to be explained in Section VII-D become fully available.

Finally, we consider a lattice filter with a bireciprocal characteristic function. It has been designed to be used repeatedly as a branching filter in the same transmultiplexer already mentioned in relation to Figs. 30 and 31 [124], [139], [140]. Its block diagram structure is given in Fig. 34(a), a corresponding detailed signal-flow diagram in Fig. 34(b), and in Fig. 35(a) and (b) are given the stopband and passband

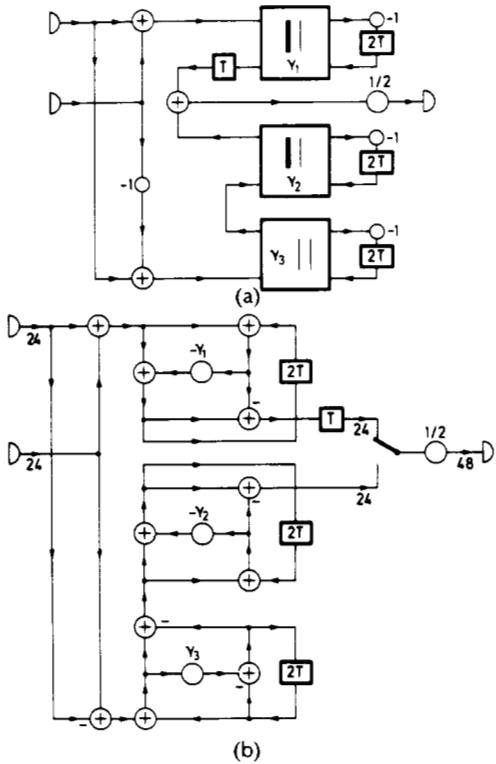


Fig. 34. (a) Block diagram of a branching filter needed repeatedly in a transmultiplexer. (b) Corresponding detailed signal-flow diagram; the numbers 24 and 48 correspond to the respective sampling rates (in kilohertz) as mentioned in the first paragraph of Section X-A.

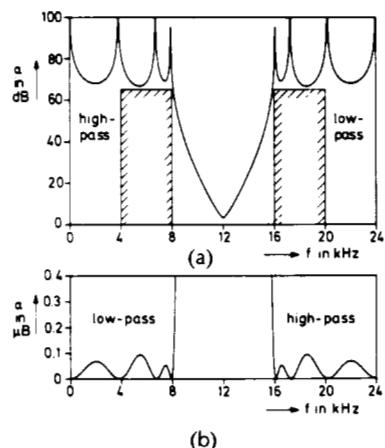


Fig. 35. Loss response of branching filter according to Fig. 34, with multiplier coefficients given by (100). (a) Stopbands. (b) Passbands.

loss responses resulting for

$$\gamma_1 = 0.01011001 \quad \gamma_2 = 0.00011 \quad \gamma_3 = 0.010001. \quad (100)$$

The frequencies indicated in Fig. 35(a) and (b) correspond to the lowest rate at which this filter is to be used in the application mentioned. Note that in Fig. 34(b) the adder appearing near the output in Fig. 34(a) has been replaced by a switch which alternately takes a sample from the upper and lower branch, thus creating effectively a doubling of the sampling rate (cf. third last paragraph of Subsection VI-A3 as well as Section X-A). The delay T in Fig. 34 corresponds to this higher rate.

The structure of Fig. 34(b) comprises 11 adders. We will refer to adders thus appearing explicitly in the signal-flow diagram as *explicit* or *algorithmic adders*. If the multiplications required are implemented by shift and add rather than by use of specific multipliers, additional adders will be needed, which we call *implicit* or *coefficient adders* (short: *co-adders*). For realizing the coefficients given by (100), five implicit adders are needed. Thus for a multiplier-free realization of the complete branching filter the total number of adders is $11 + 5 = 16$. Observe that the passband loss in Fig. 35(b) is indeed given in microbel (μB), 1 μB being thus 10^{-5} dB. The extreme smallness of the passband loss is, of course, not of real practical significance, but is due to what has been discussed in the second last paragraph of Section IV-B.

In addition to the examples presented in this section, many further ones have been published in [117] as well as in various other places [119], [127], [171]–[173], [412]. To carry out discrete optimizations required to arrive at such results any of the existing general methods can be used. However, due to the considerable insensitivity with respect to coefficient changes application of these methods can, in practice, be much easier than for other types of digital filters, and even methods otherwise not very attractive may become feasible [115]–[117], [127], [165], [167], [171]–[176]. Very efficient methods for computing the sensitivities needed, e.g., in optimization procedures for WDFs [177] as well as other aspects concerning sensitivity computations have been also published [178]–[180].

D. Reference Filters Involving Unit Elements

The type of WDF that is in several respects the simplest of all is that obtained from a reference filter consisting of a chain of unit elements (Fig. 36(a)). Such reference filters are well-known from microwave filter theory, and the resulting WDF is shown in Fig. 36(b).

Instead of unit elements we could just as well have used QUARLs in Fig. 36(a). The transmittances of the resulting modified reference filters differ from those of the original one at most by constant delays. These are due to the factors $e^{\Delta t_i}$, $i = 3$ to n , that occur in the corresponding chain matrices (cf. second column of Table 2). Two examples of resulting WDF structures are given in Fig. 36(c) and (d). For these, similar comments hold true as for the reactance realizations of Fig. 12(d) and (e). Alternatively, we may again derive the structures of Fig. 36(c) and (d) from that of Fig. 36(b). However, instead of the equivalence of Fig. 13 we now must make use of the more general ones shown in Fig. 37 [1], [69]. Indeed, it can be verified that the structures of Fig. 36(b)–(d) are *essentially equivalent*, i.e., such that by repeated application of the equivalences of Fig. 37 they can be transformed into one another except, possibly, for constant (positive or negative) delays appearing in cascade of input and/or output terminals [69]. Note that delays of these latter types are indeed irrelevant from a transmission point of view so that the concept of essential equivalence does usually cover all needs encountered in practice (i.e., a stricter form of equivalence is usually of no avail). Note also that the equivalences of Fig. 37 also hold if N_0 is nonlinear and that they can even easily be extended to the time-varying case [1]. Clearly, the comments given in Section V-A concerning the total amount of storage required and the

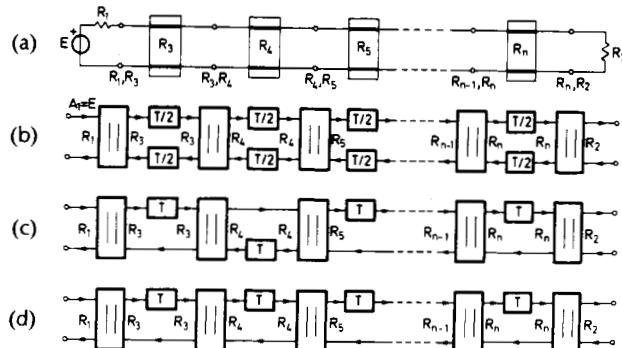


Fig. 36. (a) Filter consisting of a cascade of unit elements. (b) Corresponding WDF structure. (c) Structure essentially equivalent to (b); it comprises only full delays, and these appear alternately in the forward and backward path. (d) Structure essentially equivalent to (b), as in (c), but the delays now appear all in the forward paths.

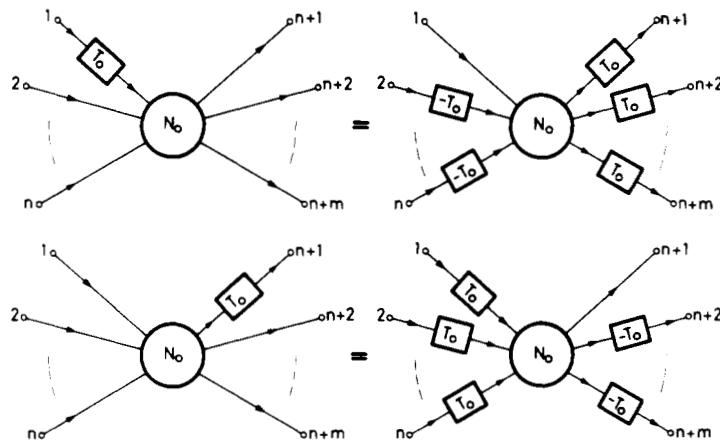


Fig. 37. Two simple equivalences holding for an arbitrary delay T_0 and an arbitrary signal-flow multipole N_0 (which may even be nonlinear).

number of multipliers in a critical path also hold for Fig. 36 in the same way as for Fig. 12.

More generally, we can consider reference filters that are composed of ladder sections alternating with unit elements (or QUARLs). Examples of such reference low-pass filters are given in Figs. 38(a), 39(a), and 40(a). In Fig. 38(a), shunt capacitances are alternating with unit elements, and the resulting WDF is shown in Fig. 38(b). In the structure of Fig. 39(a) every second shunt capacitance is replaced by a resonant circuit, hence this structure can realize attenuation poles at the finite frequencies $\phi_5 = \sqrt{R'_5/R''_5}$ and $\phi_9 = \sqrt{R'_9/R''_9}$. Fig. 39(a) has been drawn in such a way that even for the WDF realization of the series resonant circuits the unit element of Table 12B is realized by two delays $T/2$ rather than, equivalently, by a single delay T , as in Table 12D. Thus in the realizations of Figs. 38(b) and 39(b) any critical path involves only one multiplier.

This, however, is no longer true in the case of the low-pass reference filter of Fig. 40(a), although even then the critical paths comprise only two multipliers, as can be seen in the WDF realization of Fig. 40(b). Obviously, by appropriately introducing unit elements one can always reduce the number of multipliers in a critical path. In a sense, a unit element produces a decoupling of the timing requirements for those parts of the circuit that precede the unit element and those following it. Note that we could also have chosen, e.g., the outer two parallel adaptors to be

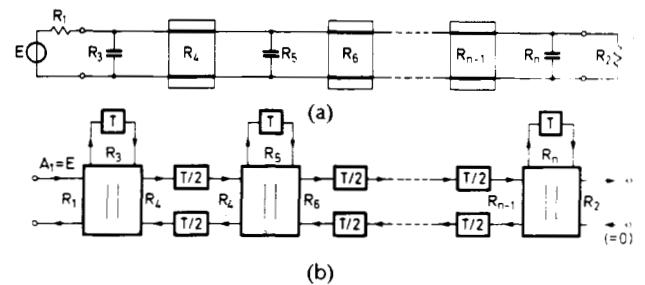


Fig. 38. (a) A reference low-pass filter consisting of a sequence of shunt capacitances and unit elements in alternating order. (b) Corresponding WDF.

unconstrained, thus the two subsequent series adaptors to be constrained; it would have to be checked in a practical situation which choice leads to better overall results.

Theory and design of reference filters involving unit elements follow essentially the same principles as for the usual ladder filters except for some simple generalizations. The corresponding procedures to follow are amply described in the literature, including the case of Chebyshev passband behavior and the arbitrary choice of those transmission zeros whose location is (contrary to the zeros at $\psi = 0$, $\psi = \infty$, and $\psi = \pm 1$) not imposed by the structure [91]–[95], [171], [181]–[185].

A unit element appearing as a section in the overall chain

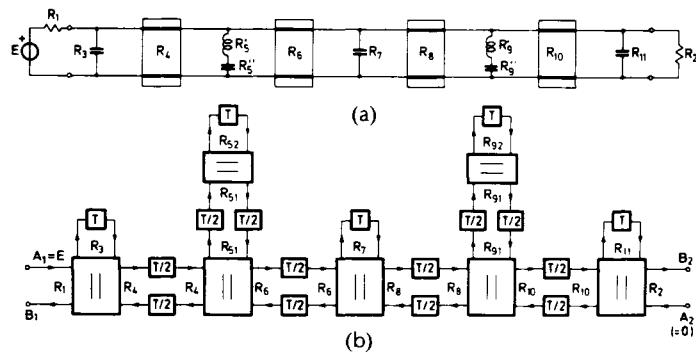


Fig. 39. (a) A reference low-pass filter consisting of a sequence of shunt branches and unit elements in alternating order; it has attenuation poles at the resonant frequencies of the series resonant circuits. (b) Corresponding WDF.

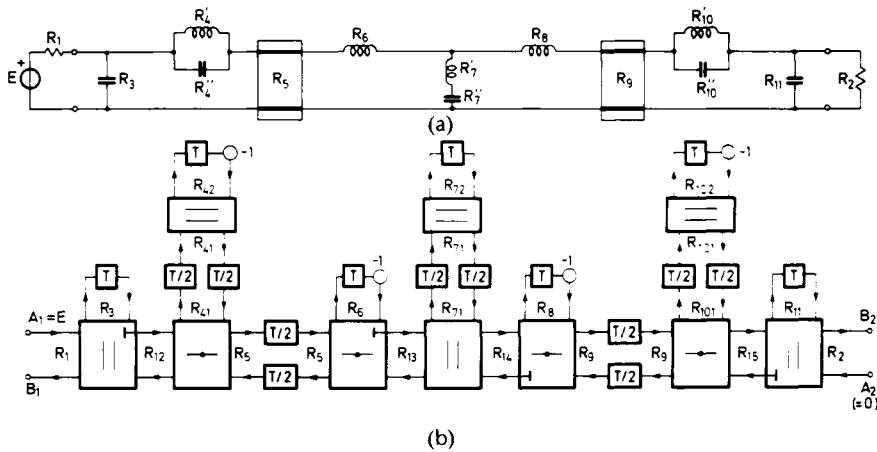


Fig. 40. (a) A reference low-pass filter consisting of ladder sections alternating with unit elements. (b) Corresponding WDF.

constituting the filter does indeed inherently impose a zero at $\psi = \pm 1$ (in the form of the factor $\sqrt{1 - \psi^2}$). Since such a zero does not occur at real frequencies, the contribution of the corresponding unit element to the passband loss is less than for other types of reactive elements, although the requirement in number of multipliers is the same. Hence, if sufficient freedom is available, one should use only as many decoupling unit elements as are needed in order to meet the requirements concerning parallelism and speed.

Structures such as those of Figs. 38(a), 39(a), and 40(a) can also be computed by starting from a suitable conventional ladder design obtained by any existing approach (possibly even by using tables [37], [149]–[152]). The required number of unit elements is then inserted between the input and/or output port and the corresponding resistive termination, the characteristic impedances of these unit elements being all chosen equal to the respective terminating resistance. This does not affect the original transfer functions except, obviously, for constant delays, which are usually irrelevant. The unit elements are then shifted to the desired location by using Kuroda's and Levy's transformations [91], [93], [186]–[188]. In this case, however, the filtering capability of the unit elements thus introduced is totally lost. Such an approach may thus be acceptable only if a quick design is needed, i.e., if it is not of major importance how complex the solution finally obtained will be. However, whenever algorithmic simplicity or amount of hardware required is of

importance, as is almost always the case for circuits to be put into production, the more efficient design approaches referred to before should be employed.

Although a design according to Fig. 36 is less efficient than one according to, say, Figs. 38–40, it has, in view of its simplicity, drawn particular attention [184], [189]–[194]. It requires indeed only two-port adaptors, just as the most attractive structures for lattice WDFs.

On the other hand, structures such as those of Figs. 38 and 39 can be simplified considerably if one imposes conditions such as

$$R_4 = R_6 = R_8 = \dots = R_{n-1}. \quad (101)$$

In this case, all internal three-port adaptors can be realized in the simplified way shown in Table 9A. Clearly, one cannot then use standard filter design methods, and it becomes unavoidable to use a direct optimization in which the constraint (101) is explicitly taken into account. Such an approach is not that easy, but remarkably efficient. It has indeed been found that the degradation of attenuation performance compared to that obtained with an unconstrained optimal design is astonishingly small, although this degradation is substantially larger if the terminating resistances \$R_1\$ and \$R_2\$ are also included in the equalities (101) [171], [173], [195].

A structure such as that of Fig. 38 has also been designed with equalized group delay [196]. It has been found that the

group-delay behavior is also remarkably insensitive to multiplier changes. This is understandable since one can expect also an improvement in group-delay sensitivity if the loss sensitivity is small. Indeed, phase can be expressed in terms of attenuation if the transfer function is minimum phase, and the same holds true if its only zeros in the right half-plane are due to factors of the form $(1 - \psi)$ originating from unit elements or QUARLs occurring as chain-connected two-ports in the overall reference structure, as is the case in Fig. 38(a).

E. Equivalence Transformations

Adaptors of one type can be transformed into those of the opposite type in mainly two ways. First, one can apply to an adaptor the principle of flow reversal. It is known [197] that flow reversal applied to a linear signal-flow diagram reproduces the original transfer function, but for the opposite direction of transmission. Thus if originally 1 is an input and 2 an output node and if the corresponding transfer function is H_{21} , then after flow reversal, 2 is an input and 1 an output node, and for the new transfer function H_{12} , $H_{12} = H_{21}$.

It can be shown [72] that flow reversal combined with sign inversion at each output terminal (or, equivalently, at each input terminal) transforms a parallel adaptor into a series adaptor and vice versa. The multiplier coefficients then remain unchanged, and the result just stated may thus be expressed as shown in Fig. 41 (compare also Tables 6 and

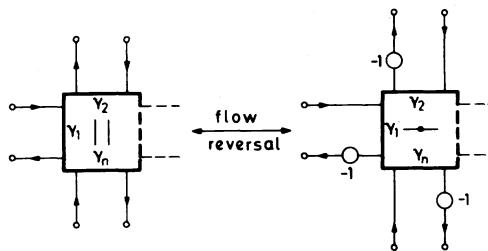


Fig. 41. Representing the transformation of an adaptor by flow reversal.

9A with Tables 8 and 9B, respectively). The proof of this property can easily be given by writing the adaptor equations in matrix form

$$\mathbf{b} = \mathbf{S}\mathbf{a}$$

where \mathbf{a} and \mathbf{b} are the vectors of the n -input and n -output waves, respectively, and \mathbf{S} the (voltage scattering) matrix describing the adaptor; due to the afore-mentioned property of the signal-flow diagrams, flow reversal amounts to replacing \mathbf{S} by \mathbf{S}^T . On the other hand, writing more specifically $\mathbf{S} = \mathbf{S}_p$ for the parallel adaptor and $\mathbf{S} = \mathbf{S}_s$ for the series adaptor, we have indeed

$$\mathbf{S}_p = \mathbf{e}\boldsymbol{\gamma}^T - \mathbf{1} \quad \mathbf{S}_s = \mathbf{1} - \boldsymbol{\gamma}\mathbf{e}^T \quad (102)$$

where \mathbf{e} and $\boldsymbol{\gamma}$ are the n -dimensional vectors

$$\mathbf{e} = (1, 1, \dots, 1)^T \quad \boldsymbol{\gamma} = (\gamma_1, \gamma_2, \dots, \gamma_n)^T \quad (103)$$

and $\mathbf{1}$ is the unit matrix of order n . It may be mentioned that we also have

$$\mathbf{e}^T \boldsymbol{\gamma} = 2 \quad \mathbf{S}^2 = \mathbf{1} \quad \mathbf{G}\mathbf{S} = \mathbf{S}^T \mathbf{G}$$

where \mathbf{G} is the diagonal matrix of the port conductances G_i to G_n ; these relationships also hold if \mathbf{S} is the (voltage scattering) matrix describing not just one adaptor, but an n -port composed of any number of adaptors.

A second type of relationship between series and parallel adaptors is explained in Fig. 42; it can also be easily verified [98]. In the case of two-port adaptors, the series adaptor involved can again be replaced by a parallel adaptor, making use of Fig. 5; this leads to the equivalence of Fig. 43, where all three coefficients, γ , γ_1 , and γ_2 (of which however only one will usually be employed in any specific case) are indicated.

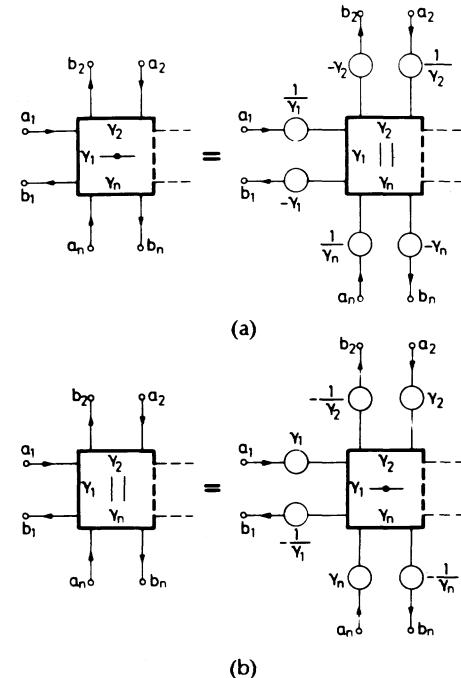


Fig. 42. (a) Transformation of a series adaptor into an arrangement involving a parallel adaptor. (b) Transformation of a parallel adaptor into an arrangement involving a series adaptor.

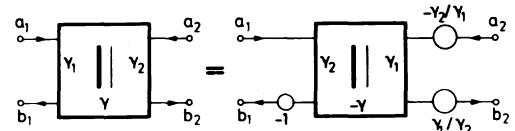


Fig. 43. An equivalence between two-port parallel adaptors.

Using the transformations of Figs. 42 and 43 and combining these with the simple equivalences given in Fig. 44 one can derive for any of the WDF realizations described in Sections V and VI-A-VI-D a whole variety of new realizations. A simple example for this is explained in Fig. 45 [98]. (The alternative structures in Table 13C and F can also be derived this way from those in Table 13B and E, respectively.) For the structures of Fig. 28(b) and (c), e.g., which comprise each a total of 10 adaptors, one already obtains this way $2^{10} = 1024$ choices, each of which may furthermore be operated either in the forward or in the backward direction. If all adaptors in a given WDF are replaced this way by their respective counterparts and if all the superfluous pairs of multipliers with values -1 then appearing are

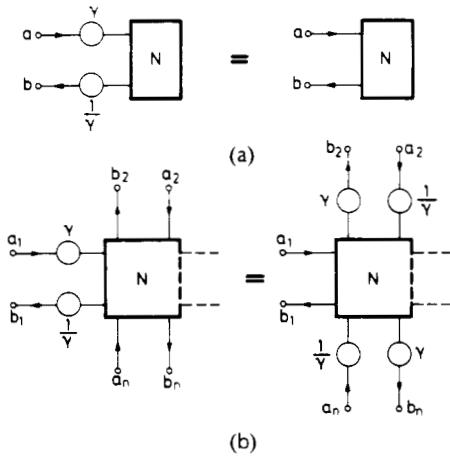


Fig. 44. Two simple equivalences valid for (a) a linear signal-flow one-port N and (b) a linear signal-flow n -port N .

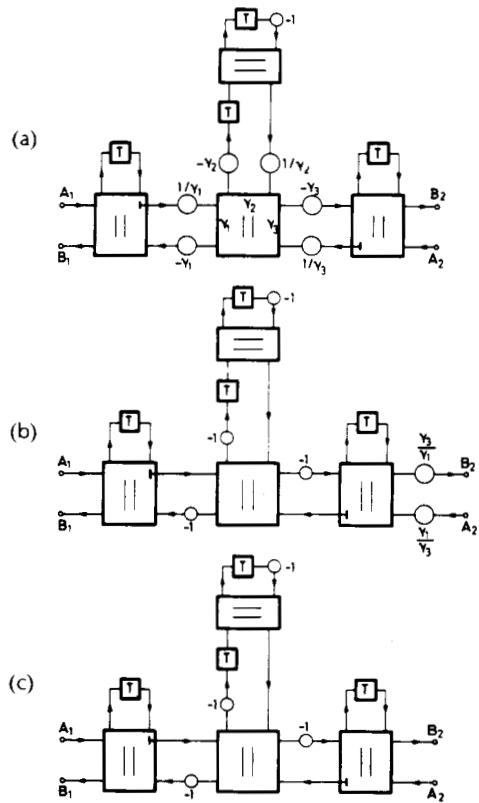


Fig. 45. (a) Structure obtained by applying to the series adaptor in Fig. 29(b) the transformation of Fig. 42(a). (b) Structure obtained by applying to (a) twice the transformation of Fig. 44(b) and once that of Fig. 44(a). (c) Structure whose external properties differ from those of Fig. 42(a) at most by constant factors in the two transmittances.

eliminated (cf. Fig. 44), the resulting structure corresponds to that which would be derived from the dual of the original reference filter.

Finally, some further equivalences, which are sometimes of use, are explained in Fig. 46 (cf. Table 3D). Additional such equivalences, valid for adaptors with more than two ports, can be found in [98]. In the same paper it is also explained how adaptors with more than one multiplier can be decomposed into *elementary adaptors*, i.e., each adap-

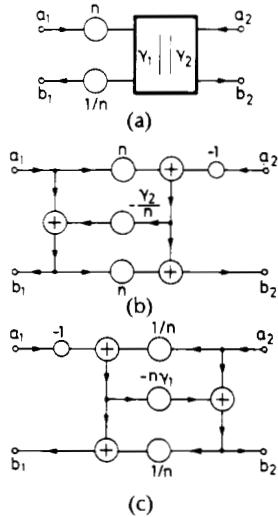


Fig. 46. (a) A two-port parallel adaptor with a pair of reciprocal multipliers. (b) and (c) Two corresponding realizations involving either no multiplier of coefficient $1/n$ or no multiplier of coefficient n , respectively.

tor comprising only one multiplier. A disadvantage of such decompositions is added complexity of the critical paths.

F. Some Conclusions

A variety of families for realizing WDFs have already been discussed, and combinations of such families are also possible. (For further examples of families cf. Section IX.) For each family, a large number of choices is available by making use of equivalence transformations. These do not produce any changes in the values of the multiplier coefficients, except in the case of transformations such as those of Fig. 46. It is easily verified that in all cases the realizability conditions of Theorem 1 (Section II-A) are satisfied.

For any realization selected, the multiplier coefficients may be simplified by applying discrete optimization. It can easily be checked, however, that in all cases discussed so far one can always return from the structure whose coefficients have thus been modified to a reference filter having exactly the same structure as the original one, although with modified element values. These remain positive as long as in each adaptor all multiplier coefficients referring to specific ports (such as γ_1 to γ_n in Tables 5 and 7, thus including those realized indirectly via the choice of dependent ports) remain positive. In particular, the reference filter thus remains passive. This implies not only that the sensitivity arguments of Section II-C remain valid, but more importantly that the same holds true for the stability arguments to be discussed in Section VII.

In addition to the equivalence options referred to before, other options may be obtained by selecting the reflection-free ports and/or the dependent ports in a different fashion. As we have seen, however, certain general rules can be given according to which selections should preferably be made so that this aspect does not give in practice any or at least not much freedom. On the other hand, even for a given reference filter structure such as the one of Fig. 28, complete freedom still exists in choosing the order in which the transmission zeros are distributed among the resonant circuits by which these zeros are being realized.

It is important to stress that among the WDF families

discussed there are several which present a particularly pronounced *homogeneity* and/or offer a high degree of *parallelism*. Furthermore, so-called *multiplexing* can be applied to WDFs just as easily as to any other digital filter structure. Consequently, contrary to what is frequently believed [198]–[200], WDFs can satisfy even the most stringent requirements concerning simplicity of structure, pipelineability, and multiplexability that can possibly be achieved by any other type of digital filter structure.

The WDF structures we have examined can realize all transfer functions that can be achieved by the families of reference filters considered so far. This includes not only those achievable as transmittance, but also others achievable as reflectance (cf. Section IV-B) [201]. This encompasses almost all transfer functions encountered in practice, although not strictly all, and we will see later (Section IX-A) how this slight restriction can completely be lifted. It should be pointed out, however, that for common filter applications it is almost never required to have recourse to such additional possibilities. Indeed, filter requirements are usually prescribed not in terms of transfer functions, but in terms of loss and, possibly, phase or group delay that must be located within certain limits imposed by so-called tolerance plots. The WDF structures examined so far are amply sufficient to satisfy any such requirement. In fact, the situation bears a certain resemblance to that for nonrecursive filters. For these, the restrictions on the type of transfer functions are by far more severe, yet they can be used to satisfy any actual filter needs (although usually at an added expense, contrary to what is the case for WDFs).

VII. STABILITY AND EFFECTS DUE TO SIGNAL QUANTIZATION

A. Passivity and Losslessness; Stored Pseudoenergy

WDFs are composed of building blocks (elements, adaptors) that have 1, 2, or more ports and a *port resistance* assigned to each port; its reciprocal is the *port conductance*. It is convenient to define the *instantaneous pseudopower* $p(t_m)$ absorbed at t_m (cf. (19)) by an n -port building block N by means of

$$p(t_m) = \sum_{v=1}^n [a_v^2(t_m) - b_v^2(t_m)] G_v \quad (104)$$

where a_v , b_v , and G_v are the input signal, the output signal, and the port conductance, respectively, at port v . Corresponding to (104), the *steady-state pseudopower* absorbed by N is defined by

$$P = \sum_{v=1}^n (|A_v|^2 - |B_v|^2) G_v. \quad (104')$$

If we always have $P \geq 0$ for $\text{Re } \psi \geq 0$ then N is said to be *pseudopassive* (or simply, *passive*), if in addition we have $P = 0$ for $\text{Re } \psi = 0$ it is said to be *pseudolossless* (or simply, *lossless*), and if $P = 0$ for all ψ it is said to be *nonenergetic*. Note that we may, in the case of a delay-free building block, equivalently replace the requirements for pseudopassivity and nonenergicity by the corresponding requirements that for all t_m we have $p(t_m) \geq 0$ and $p(t_m) = 0$, respectively; the resulting definitions clearly also apply if the building block is nonlinear.

It can be shown that all adaptors (parallel, series, and

lattice), ideal transformers, gyrators, and circulators are non-energic; that capacitances, inductances, unit elements, and QUARLS are pseudolossless; and that resistances are pseudopassive. Using these results, direct proofs of the pseudopassivity and pseudolosslessness properties of complete WDFs under linear operating conditions can be given [7], [100]. (Indirect, although equally rigorous proofs of the same properties, clearly follow automatically by considering the reference filter.)

A full-synchronous WDF may be considered to comprise only delays of value T . The pseudoenergy stored in these delays during the interval (t_m, t_{m+1}) is defined by

$$T \sum_v G_v a_v^2(t_m) \quad (105)$$

where the sum has to be extended over all delays just mentioned, a_v being the signal incident to the v th delay, and G_v the port conductance of the port to which this delay is connected. For half-synchronous WDFs the same concepts may be used after transforming the original WDF into an essentially equivalent full-synchronous WDF structure [202]. Indeed, such a transformation can always be carried out by making use of the equivalences of Fig. 37, as can be seen by observing that for a half-synchronous WDF the requirements of Theorem 1 (Section II-A) are necessarily fulfilled and that Theorem 2 of [69] is therefore applicable.

B. Suppression of Parasitic Oscillations

It is known that under zero-input conditions parasitic oscillations can occur in a digital filter; these are in fact periodic *limit cycles*. One usually distinguishes between two types of such oscillations, i.e., *granularity* (*small-scale*) and *overflow* (*large-scale*) limit cycles. Of these, the latter are much more severe since they run across the entire number range in the filter.

Using (105) as a *Lyapunov function* it can be shown [9], [202] that a WDF is output stable (thus cannot have overflow or granularity limit cycles appearing at the output) if all building blocks remain pseudopassive also under the nonlinear conditions due to the quantization operations applied to the signals. In practice, this pseudopassivity is satisfied if inside all of the adaptors and ideal transformers the arithmetic operations are carried out exactly and if at each output terminal of each adaptor magnitude truncation is applied for signals not exceeding the overflow limit, while if this limit is exceeded any arbitrary type of overflow correction is permitted. Furthermore, a WDF is *completely stable* (i.e., has no unobservable limit cycles) if it cannot sustain unobservable periodical oscillations under ideal linear conditions and if the rule adopted for overflow correction is such that a simple sign inversion (as would naturally appear in two's-complement arithmetic if the signal hits the upper limit +1) is excluded. Note that these conditions also exclude the appearance of any small- and large-scale oscillations combined.

In fact, under the conditions mentioned before WDFs are not only free of limit cycles, but exhibit even *discrete asymptotic stability*. By the latter concept we mean an extension of the classical concept of asymptotic stability to value-discrete systems, i.e., to systems in which the signals can only take discrete values. Recall, that asymptotic stability requires not only attractivity, but also stability (in the

sense of Lyapunov) [203]. For the latter, the usual definition should now be modified by requiring that for any $\epsilon > 0$ there exists not only a $\delta > 0$, but also an $\eta > 0$ such that the trajectories remain within a cylinder of radius ϵ as long as the initial state does not deviate by more than δ and the quantization step available for representing the signals is at most equal to η .

All these considerations hold for any kind of number representation. However, for the case of two's-complement arithmetic, simple rules have been given [9] by means of which the requirement for exact computation inside the adaptors can partly be lifted. It should be stressed, however, that signals at inputs of multipliers have to be computed exactly and that thus in particular no overflow correction may be applied *before* a multiplication is carried out. Failure to observe such requirements are the reasons why limit cycles in WDFs have sometimes been reported to have been observed [204]. On the other hand, since multiplier coefficients can always be chosen to be smaller than 1 in modulus (in fact even smaller than 1/2) extra bits provided in order to accommodate, before a multiplication, signal values exceeding the adopted range may often be dropped again as soon as the multiplication has been carried out. Some special considerations for floating-point arithmetic are given in [205].

Clearly, the rules mentioned before are only sufficient, not necessary, and definitely not necessary for ensuring suppression of all small-scale limit cycles. It turns out in practice that oscillations of the latter type are usually absent as soon as the rule for suppressing them (thus the use of magnitude truncation) is applied only to those adaptor outputs that lead straight into delays; a sufficient amount of dissipation is indeed introduced this way. Furthermore, even if no specific means are used to suppress small-scale limit cycles, those that do appear have only very small amplitudes and may thus frequently not be disturbing at all. Moreover, the known means of introducing randomness into the quantization operations in order to spread the limit cycle energy uniformly over the entire frequency range [206]–[208] may be particularly easy to apply in the case of WDFs. Most of these indeed consist of just one or at most (in the case of lattice WDFs) two individual blocks with high degree of internal coupling so that the required pseudorandomness may be introduced at just one, or at most two, properly chosen locations.

The situation is more complex if *periodic inputs* are considered. Except for some very simple situations such signals cannot be, e.g., strictly equal to sinusoids since these involve, in general, irrational numbers and thus cannot be represented exactly by a finite number of bits. Hence, the output signal will differ unavoidably from the desired one by some superimposed periodic oscillation. In WDFs, however, such oscillations are very small. Indeed, if pseudopassivity is observed the total energy appearing, actually or virtually, in such oscillations at the various filter output terminals (say those corresponding to S_{21} and S_{11} , even if, e.g., only the former is actually provided) cannot exceed the energy lost in the desired signal due to the presence of the superimposed parasitic oscillation. Furthermore, for the simplest cases (constant input as well as input of period 2) elimination of such oscillations is possible in certain WDFs by means of *controlled rounding* [209], [210].

Another problem is that of ensuring *stability under looped conditions*, as is encountered, e.g., due to the two-wire/four-wire transitions (hybrids) in a long-distance telephone link (Fig. 47(a)) [1], [124], [211]–[213]. Ideally, the transmission around the loop then appearing is interrupted

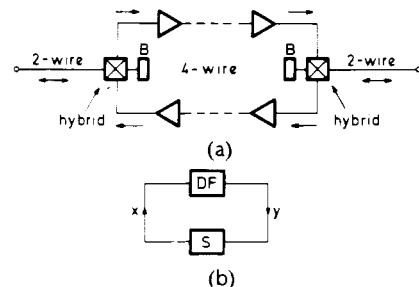


Fig. 47. (a) Creation of a feedback loop in a transmission link due to the hybrids used in the two-wire/four-wire transitions (B = balancing network). (b) Simplified representation of a digital filter DF thus appearing in a loop closed via the external system S .

due to the balancing networks (marked B), but the balancing impedances can at best be compromises between the different types needed, and under unfavorable or faulty conditions no reduction at all of the loop transmission may be produced. Hence, a digital filter used in the four-wire part of the link will in fact be looped via an external feedback path (comprising the system S , with usually high phase shift (Fig. 47(b)), and, in view of the transmission levels conventionally adopted in a telephone plant, stability (thus also the absence of parasitic oscillations) must remain ensured even if the loss in this path approaches zero. While no solution to this problem is known for other types of recursive digital filters, it can be shown [211] that WDFs remain stable if the pseudopassivity requirements discussed above are satisfied, i.e., for very general assumptions concerning S and in particular its nonlinear behavior. (It is true that one of these assumptions is that S is constant, contrary to what is the case due to the unavoidable presence of stages for modulation and sampling rate alteration. However, arguments can be forwarded that explain why this can hardly aggravate the problem in any serious fashion, as is also not the case for loops of the type of Fig. 47(a) in conventional analog transmission systems.)

The relationship of the various stability aspects discussed above with problems in control engineering has been pointed out in [214], [215] and other aspects related to finite-arithmetic stability are considered in [216]–[218].

It should finally be stressed that all sufficiency proofs for the stability properties discussed in Section VII-B depend essentially on the fact that the adaptors are pseudopassive (even in the presence of signal quantization) and that this pseudopassivity is assumed to hold if all ports of the individual adaptors are accessible, thus also the ports terminated, say, by delays. This requirement is no longer fulfilled if certain equivalence transformations are used which, contrary to those described in Section VI-E, involve also the delays. Transformations of this type have, e.g., been proposed for saving an adder [219] or may implicitly be present in WDF approaches avoiding the use of adaptors [157]–[164]. Care has to be taken in such cases since absence of parasitic oscillations is then no longer ensured.

C. Dynamic Range and Scaling Techniques

We call *dynamic range* the distance (usually expressed in decibels) from output quantization noise to that output signal for which overflow is reached inside the circuit [1]. In order to achieve good dynamic range it is advisable to start, at least in the case of ladder-type or related structures (cf. Sections VI-B and VI-D) from reference filters presenting from input to output as little change of impedance level as possible. Furthermore, as explained before, an unconstrained adaptor appearing in a chain of adaptors should be located as centrally as possible.

Frequently, the dynamic range is already very good if these precautions are taken. In some cases, however, it can be improved more or less substantially (sometimes very substantially) by making use of adaptor transformations (cf. Figs. 41–45). This can easily be made understandable by means of the analysis carried out in Section V-A for the case of the simple arrangements of Table 13B, C, E, and F, in particular the results (72)–(74) as well as the subsequent discussion. Observe that the number of choices available when using adaptor transformations can be quite large.

Scaling is also possible, but in order to preserve passivity and losslessness it should be done by inserting ideal transformers into the reference filter, i.e., pairs of reciprocal multipliers into the WDF itself [9], [117], [220]–[223]. Indeed, while we have formerly used the equivalences of Fig. 44 in order to eliminate such pairs of multipliers that had appeared after making use of the transformations of Figs. 42 and 43, we may apply Fig. 44 just as well to introduce pairs of reciprocal multipliers at appropriate locations. The values of such scaling multipliers should however be chosen equal to powers of 2. This is true not only for reasons of economy, but also since a number n and its reciprocal, $1/n$, can both be represented exactly in a binary number system only if n is of the form 2^r where r is an integer. Note that for a structure such as that of Fig. 29(b) the corresponding structure with a maximum number of pairs of internal scaling multipliers is as shown in Fig. 48; clearly, an additional single scaling multiplier may be placed at the input terminal of the filter.

The scaling itself can be done according to any convenient criterion. The simplest is to require that no overflow occurs for sinusoidal signals. Applying this (assuming that two's-complement arithmetic is used) amounts to determining, as a function of frequency and for a constant amplitude of the filter input signal, the maximum signal amplitude appearing at any multiplier input. The corre-

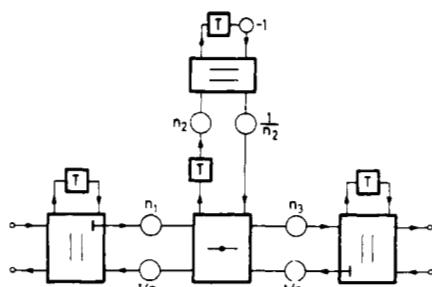


Fig. 48. Structure derived from that of Fig. 29(b), but comprising the maximum number of internal pairs of scaling multipliers.

sponding curve follows approximately the shape of the group-delay response, as can be justified at least qualitatively from a general relationship between stored pseudo-energy and group delay [224]. Consequently, this curve has a pronounced peak in any transition region between a passband and a stopband, i.e., in a region where for input signals encountered in practice the energy density is frequently very small. If the latter is the case, such peaks may be ignored.

At the extreme, scaling could be done in such a way that overflow would never occur, at least not under the assumption that the filter operates with zero initial conditions and that no faults occur. Such a scaling criterion is known to be too severe in practice, although for WDFs the gap between the requirements following from this criterion and the more common ones may be substantially smaller than for other types of recursive digital filters [225]. On the other hand, the assumption that faults never occur may be rather unrealistic, especially for circuits remaining in prolonged operation such as is the case for transmission equipment. Altogether, a more appropriate approach may therefore be to impose a more conventional scaling criterion and to require that the circuit is actually *forced-response stable* [42]–[44]. Roughly speaking, the latter implies that the effects due to overflow die out once the input signal has decreased to a level for which, under linear conditions, the signal values inside the circuit would at no point exceed the available range.

While for conventional recursive digital filters it is not known how to ensure forced-response stability, the problem is completely solved for WDFs [43], [226], [227]. The simplest approach for this is to use the concept of incremental pseudopassivity [226], [227]. It has been found that incremental pseudopassivity is guaranteed (neglecting effects due to granularity) as long as at the various output terminals of the adaptors the required overflow correction is carried out by a continuous curve whose slope does not exceed the range between $\pm 45^\circ$. In particular, simple saturation or $\pm 45^\circ$ triangular characteristics are permitted (Fig. 49). Again, such requirements are only sufficient, but

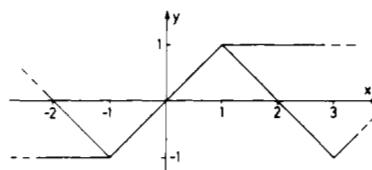


Fig. 49. Two simple types of overflow characteristics that ensure incremental pseudopassivity (thus in particular, forced-response stability) if applied at the output terminals of the adaptors.

not necessary, and a WDF may be forced-response stable even with two's-complement overflow behavior (cf. Section VII-D).

Incremental pseudopassivity not only guarantees forced-response stability, but also various other useful properties [226], [227]. Among these we cite that, even if overflows keep occurring, small changes of the input signal cause only small changes of the output signal and arbitrary changes in initial conditions cause no lasting change of the output signal.

Experience shows that properly designed WDFs exhibit excellent dynamic range performance (cf., e.g., [117], [125], [225], [228]). This is not surprising, especially in view of the relationship between dynamic range and sensitivity mentioned at the beginning of Section II-C as well as the optimality result to be discussed in Section IX-E. Observe also that the added noise appearing if magnitude truncation is used instead of rounding (cf. Section VII-B) is much smaller in practice [229]–[232] than what is frequently believed. For many types of signals, including, e.g., speech signals, the error samples due to magnitude truncation are indeed correlated to the signal itself in such a way that the major contribution amounts simply to a slight change of the loss response of the filter, thus not to actual noise.

A number of additional papers on noise and dynamic range in WDFs have been published [233]–[240]. In order to arrive at truly meaningful comparisons, care must be taken however in interpreting these and other results. This concerns not only the necessity of properly determining overflow limits [241], but also of using the WDF structure most suitable for the application in mind, of making the most appropriate choice for the location of the reflection-free and the dependent ports, of making proper use of adaptor transformations, and of applying proper scaling.

D. Properties of Arrangements Involving Two-Port Adaptors

We have seen that two-port adaptors can be realized in different ways (cf. Section III-E) and that arrangements involving two-port adaptors can be transformed into similar ones by using the equivalences of Figs. 43 and 44. By appropriately using the choices thus available it is possible not only to carry out scaling (cf. Section VII-C), but also, in certain cases, to exclude automatically the appearance of any small- or large-scale limit cycles [109], [110] and even to guarantee forced-response stability without any special expenditure [242].

To illustrate this, consider first the first-degree arrangements of Table 13B and C, but for instantaneous signals, and assume the input to be zero. A signal circulating through the loop closed via T is then, in addition to being delayed, multiplied by γ at each cycle. Thus if $\gamma < 0$ it changes sign at each cycle (unless it is zero). Consequently, since $|\gamma| < 1$, the natural two's-complement truncation will, if applied at the appropriate location, reduce the magnitude each time the signal has become positive, yet will at least never increase it each time the signal has become negative. This implies, that the signal must become zero after a finite number of steps, i.e., it is not required to apply magnitude truncation for ensuring zero-input stability. In other words, for the sections of Table 13B and C no precaution other than properly applying two's-complement truncation is required for avoiding any small- or large-scale limit cycles if $\gamma < 0$. The situation is exactly the same for the sections of Table 13E and F if $\gamma > 0$.

Consider next the possibility of overflow occurring. We may identify the two-port adaptor in Table 13B or E with that in Table 10B, but with γ as given in Table 13. From (48b) we obtain first

$$b_2 = (1 - \gamma)a_1 + \gamma a_2 \quad (106)$$

then for $\gamma \geq 0$, since $\gamma < 1$

$$|b_2| \leq (1 - \gamma)|a_1| + \gamma|a_2|$$

and thus, if $|a_1| \leq M$ and $|a_2| \leq M$ (M being the permitted bound, usually $M = 1$), also $|b_2| \leq M$. The same result is obtained for the circuits of Table 13C and F if $\gamma < 0$; for these circuits, indeed, γ has to be replaced by $-\gamma$, hence (106) by

$$b_2 = (1 + \gamma)a_1 - \gamma a_2 = (1 - |\gamma|)a_1 + |\gamma|a_2.$$

Consequently, overflow can never occur in the circuits of Table 13B and E if $\gamma > 0$ and in the circuits of Table 13C and F if $\gamma < 0$, assuming, of course, that the input signals and the initial values are bounded in magnitude by the same number M . For this conclusion to hold it is necessary, of course, that the computations for obtaining b_2 are carried out exactly, i.e., if flow diagrams such as those of Table 10C, D, or F are used, that the input signal to the respective multiplier is determined exactly. This in turn implies that an extra front bit is provided for ensuring an error-free representation of $\pm(a_2 - a_1)$. In the case of two's-complement arithmetic, this extra bit may be dropped immediately after a multiplication, while the need for providing an extra bit does not even arise if the signal-flow diagram of Table 10E is adopted (cf. Section VIII-D).

These results are important in particular for lattice WDFs with bireciprocal characteristic function (cf. Subsection VI-A3). We have seen that the two branches of such filters can usually be realized as cascades of sections as in Table 13, with $\gamma < 0$ for Table 13A–C and $\gamma > 0$ for Table 13D–F. As a conclusion, if Table 13C or E is chosen for realizing these sections, the natural two's-complement truncation and overflow correction is already sufficient to ensure not only the absence of all small- and large-scale limit cycles, but also forced-response stability, provided of course that the requirement concerning an extra front bit mentioned in the preceding paragraph is taken into account. This result is in agreement with the preferred choice at which we had already arrived in Subsection VI-A3. For further properties cf. also Section VIII-D.

VIII. SOME ASPECTS CONCERNING REALIZATION AND IMPLEMENTATION OF WAVE DIGITAL FILTERS

A. Canonic Realization of Wave Digital Ladder Filters and Related Structures

In a WDF structure such as the one of Fig. 28(b) the number of delays T (i.e., 10) is larger than the degree of the filter (i.e., 7). This may be a disadvantage, especially if the filter is to be time-shared among many channels (since delays, i.e., storage elements, cannot be time-shared). It can be shown [243] that for any loop of either only capacitances or only inductances a delay can be eliminated, and the same holds true for any cutset of either only capacitances or only inductances [226]. One possible structure thus resulting from that of Fig. 28(b) is shown in Fig. 50. This approach can be extended to structures involving unit elements [244], e.g., by making use of the equivalences of Fig. 51. Fig. 51(a) shows a QUARL (cf. Table 2) with $\Delta = T/2$, Fig. 51(b) a simplified representation of the same QUARL, and Fig. 51(c) and (d) two equivalent realizations of that QUARL. This way, any of the structures discussed in Section VI can be transformed into a canonic structure, i.e., into a

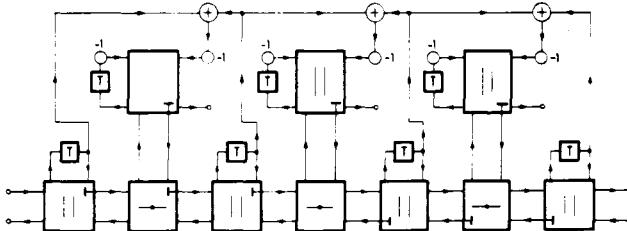


Fig. 50. Example of a canonic version of the circuit of Fig. 28(b).

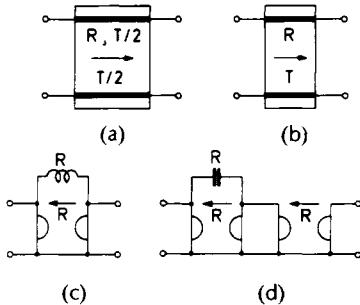


Fig. 51. (a) and (b) A QUARL with $\Delta = T/2$ and its simplified representation. (c) and (d) Two equivalent realizations of that QUARL.

structure for which the total delay involved is equal to the filter degree times T .

For WDFs thus made canonic no overflow limit cycles can occur if, at all adaptor outputs, the overflow correction inherent to two's-complement representation is simply kept as it is. Although a complete and simple theory for other types of parasitic oscillations may not be feasible, possibilities for ensuring stability have been published [245], [246]. Furthermore, experience seems to indicate that the means for suppressing parasitic oscillations discussed in Section VII-B are even more effective in canonic versions of structures than in the original noncanonic ones.

Clearly, none of these various considerations applies to lattice WDFs since these are inherently canonic.

B. Determination of Shimming Delays

Shimming delays are those additional delays that have to be introduced into certain signal paths in order to make up for delays invariably associated with adders and multipliers in other paths. Determining the required shimming delays is quite immediate in structures for which the critical paths traverse only one multiplier, as is the case, e.g., for most realizations of lattice WDFs, but can be less trivial, e.g., in ladder WDFs (cf. Fig. 28). A simple way for solving the problem in such cases is as follows [1].

Let us number in some appropriate fashion the various arithmetic operations taking place during one cycle (period) and let τ_i be the duration needed for carrying out the i th operation. At the location in the signal-flow diagram where this duration is needed we introduce a positive delay τ_i followed by a negative delay $-\tau_i$, which does not alter the overall behavior. The delays $-\tau_i$ are then shifted through the structure by applying repeatedly the equivalences of Fig. 37 until the structure becomes essentially equivalent to one involving only positive delays. It is indeed known [69] that such a transformation can be achieved if the realizable

ity conditions of Theorem 1 (Section II-A) are satisfied, as is always the case for WDFs, and if the operating rate $F = 1/T$ is not higher than a certain maximum rate $F_{\max} = 1/T_{\min}$. The value of T_{\min} can be determined as follows: Ignore the delays τ_i just introduced, but maintain the delays $-\tau_i$. Then T_{\min} is that value of T for which in any directed loop the total delay, counted positively in the direction in which the branches of the loop are oriented, remains ≥ 0 , but reaches zero for at least one such loop [247], [248].

Clearly, the transformation for arriving at an essentially equivalent structure with only positive delays is not unique. Another interesting aspect is therefore that of *delay management*, i.e., of determining a structure involving the minimum amount of shimming delay that can possibly be achieved [249], [250]. The Petri net approach can also be used for solving shimming delay problems [251].

For two-port adaptors the realization according to Table 10F is more advantageous, from the point of view of shimming delays, than that of Table 10D. The reason for this is that the upper input signal of the adder in the lower right of Table 10F is the same as that of the multiplier. Hence, one can simply make use of the delay inherent in the multiplier and derive from there the signal to be fed to the adder.

C. General Aspects of Implementing Wave Digital Filters

WDFs can be implemented in the same way as any other digital filter, thus in particular by using either *general-purpose computers* or any form of *specific hardware* available. The particular choice to be made in a given situation will depend on the type of hardware available and especially on the nature of the given application, thus on requirements concerning ease of design, speed, power consumption, flexibility and programmability, on desirability of using time sharing and multiplexing, on volume of production, etc.

Although multiplier coefficients are frequently already very simple, further simplifications are obtained by using the *canonic signed digit* (CSD) representation [115]–[117]. For the signals, *two's-complement representation* is usually preferred, but *floating-point* (e.g., in the case of general-purpose computers) or even residue number [252] representations are also feasible. *Parallel* or *serial arithmetic* can be adopted.

While *distributed arithmetic* is not as efficient as for more conventional digital filters it can also be used [253], and methods have been investigated for making such an approach more effective [118], [119], [121], [226], [253]–[256]. It is particularly advantageous in this case to start from the coefficients as they have been determined by the approaches discussed in Section VI, possibly combined with reduction of the original structure to a form with the canonic number of delays (cf. Section VIII-A). The coefficients are then numbers with reasonably short binary wordlengths, but pseudolosslessness under linear conditions is rigorously satisfied, and this remains the case for the resulting realization by distributed arithmetic without requiring excessive length of the numbers to be stored in the ROM [118], [119], [254]–[256].

There also exists a restricted class of WDFs for which the appearance of sign inverters can completely be avoided [114], [257].

D. Hardware Implementation

While early WDFs were implemented using a *minicomputer* [258] the first WDF built using specific hardware was completed in 1973 [259]. For this, *discrete (LSI) TTL components* (for parallel arithmetic) had been used. The structure realized was that of Fig. 29, with adjustable multiplier coefficients. Other designs reported using discrete components include a 14th-degree ladder band-pass filter as discussed in Section VI-C [260], a programmable multprocessor hardware machine suitable for a variety of WDF structures [261], realizations on general digital signal processors [262], [263], an implementation of a structure according to Fig. 36 [194], high-performance filters for use in a transmultiplexer (serial arithmetic TTL components) [125], and others [264], [265]. Various papers describe aspects of hardware design [108], [266]–[273] and testing of WDFs [274], [275].

WDFs can obviously be implemented using monolithic general-purpose *digital signal processors* (DSPs). Since in a WDF the multiplier coefficients are very simple, DSPs realizing multiplications by shift and add rather than by means of a full multiplier are particularly advantageous [126], [276]. However, other general-purpose DSPs [277]–[279] can also be used [280], [281]. Such DSPs are known to combine usually one multiplication with one addition. Hence, it may be just as simple, in the case of a two-port adaptor, to adopt, e.g., the scheme of Table 10E rather than one of the others given in Table 10. An interesting advantage to be gained this way is that no precautions whatsoever for suppressing overflow limit cycles have to be taken if two's-complement arithmetic is employed, while b_1 and b_2 can both be computed in altogether four cycles, using the accumulator of the DSP. Due to this, the use of general-purpose DSPs may altogether lead to simpler realizations in the case of WDFs than for conventional types of digital filters, and this despite the fact that a WDF employs only a fraction of the capability inherent in the multiplier of the DSP [281].

Clearly, the structure of Table 10E is not the only one that meets the objectives explained before, but there is an important reason why the specific structure shown has been selected [242]. In a DSP such as the TMS 320 [278] there exists indeed an option to apply saturation (i.e., to replace the signal by +1 if it is > 1, and by -1 if it is < -1, assuming the usual signal range from -1 to +1) each time that overflow occurs at the completion of an accumulation step. Assume first that $\gamma > 0$. As explained in Section VII-D we have $|b_2| \leq 1$, and according to Table 10E no overflow can occur during the computation of b_2 , i.e., b_2 is always calculated correctly. Next, one has to compute $b_0 = b_2 - a_1$, which is equal to $\gamma(a_2 - a_1)$, and then $b_1 = b_0 + a_2$. Let us designate by b'_0 and b'_1 the values actually appearing for b_0 and b_1 , respectively, in the accumulator after saturation. If $|b_0| \leq 1$ we have $b'_0 = b_0$; b_1 is then calculated correctly, and so is b'_1 . If $b_0 > 1$, we have not only $b'_0 = 1$, but also necessarily $a_2 > 0$ (since $\gamma < 1$), thus $b'_1 = 1$; this result is not affected if b_1 is determined as $b'_0 + a_2$. The situation is analogous if $b_0 < -1$, since this implies $a_2 < 0$. Finally, if $\gamma < 0$ one can reduce the case to that for $\gamma > 0$ by simply inverting the roles of ports 1 and 2 (cf. Fig. 5(b)). As a conclusion, making proper use of the option mentioned above ensures that proper saturation at

the output terminals is achieved, i.e., according to what we have seen in Section VII-C, that overflow correction is automatically done in a way guaranteeing forced-response stability and related properties if the complete WDF is built using only two-port adaptors.

It can also be shown that multiprocessor realizations are particularly advantageous in relation with WDFs [282], [283]. This is due to the fact that a WDF is subdivided into adaptors and delays and that time and space conflicts are therefore inherently avoided.

Clearly, most preferably would be to have available an *adder-based DSP* specifically designed towards the needs of WDFs [122], [284]. Such a DSP, called PROFI, is now in an advanced stage of development [285]–[289] (Fig. 52). The same is true for a *custom-designed processor* intended for a PCM codec application (SICOFI), which has a limited programming flexibility and is indeed used with a WDF implemented on the chip [290], [291] (Fig. 53). In specialized DSPs, products may advantageously be computed by using *nested multiplication* [284].

Various approaches to direct VLSI implementation of WDFs have also been reported. These concern a single-chip realization of an individual WDF (Fig. 33) [128], [132], an

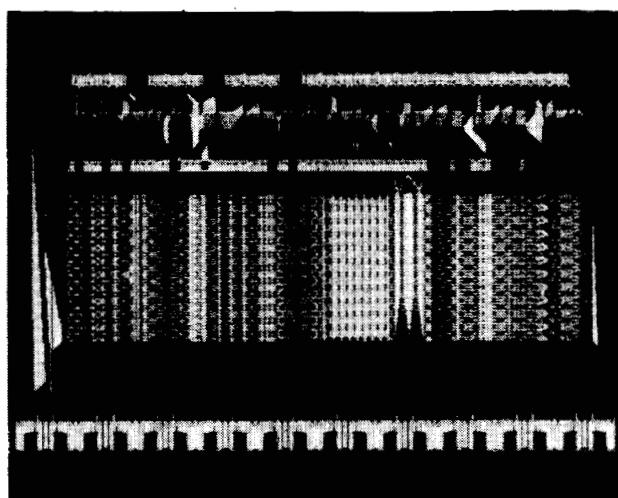


Fig. 52. Photomicrograph of the execution unit used on the adder-based digital signal processor PROFI, which is particularly suitable for implementing WDFs (reproduced with permission of Siemens, Munich).

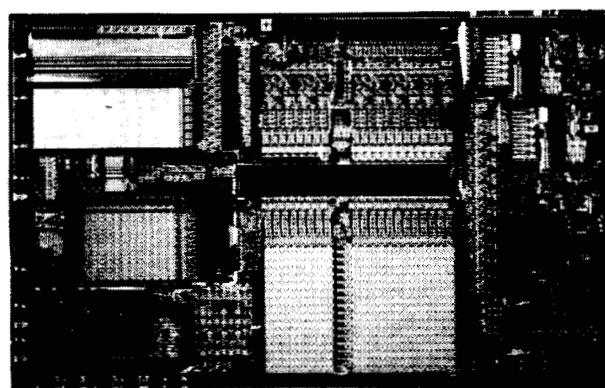


Fig. 53. Photomicrograph of the PCM codec chip SICOFI that comprises a WDF (reproduced with permission of Siemens, Munich).

implementation of a WDF on a custom-designed PCM codec chip [292], a realization by means of a universal adaptor [293], [294], considerations on the realization of WDFs by means of a more general custom design approach [295], and the development of appropriate silicon compilers [296]–[299].

IX. FURTHER TYPES OF WAVE DIGITAL FILTERS AND RELATED STRUCTURES

A. General Transfer Functions

The methods discussed in Section VI do not allow us to realize directly a so-called general Brune section [32] (Fig. 54(a)), sometimes also referred to as type-C section [300]. In structures in which such a section is needed one may practically always replace it by a structure in which the Brune section itself is followed by an ideal transformer of arbitrary ratio (Fig. 54(b)). An arrangement of the latter type can equivalently be replaced by one as given in Fig. 54(c), where, compared to the structure of Fig. 54(a), a degree of freedom exists in the choice of the ratios n_1 and n_2 of the

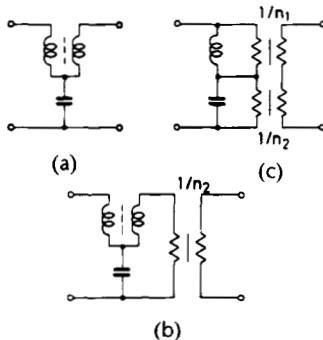


Fig. 54. (a) A Brune section in conventional representation; it comprises a pair of tightly coupled coils. (b) A Brune section with an additional ideal transformer. (c) A structure equivalent to (b).

two ideal transformers. It can be shown that by making appropriately use of this freedom, the arrangement of Fig. 54(c) is equivalent to that of Fig. 55(a) [301]. Note that the term Brune section is sometimes reserved for the case when the turns ratio of the coupled coils in Fig. 54(a) is positive, and the term type-C section for the case when this ratio is negative. Correspondingly, the search for WDF realizations has been based on distinct approaches for these two separate cases [302]–[304]. No such distinction is made in the present approach, i.e., the turns ratios in Fig. 54 may have any positive or negative values.

From Fig. 55(a) we derive immediately the arrangement of Fig. 55(b) and thus, using the equivalences of Fig. 37, that of Fig. 55(c). We have assumed here that the port resistance R_1 is imposed and that R_2 is chosen in such a way that at port 2 no delay-free path is created from the input to the output terminal, which requires

$$R_5 = R_1 + R_3 \quad R_2 = R_4 R_5 / (R_4 + R_5).$$

Similarly, we may also derive from Fig. 55(a) the arrangement of Fig. 55(d), where R_2 may be assumed to be imposed and where R_1 is chosen such that at port 1 no delay-free path is created from the input to the output terminal, requiring

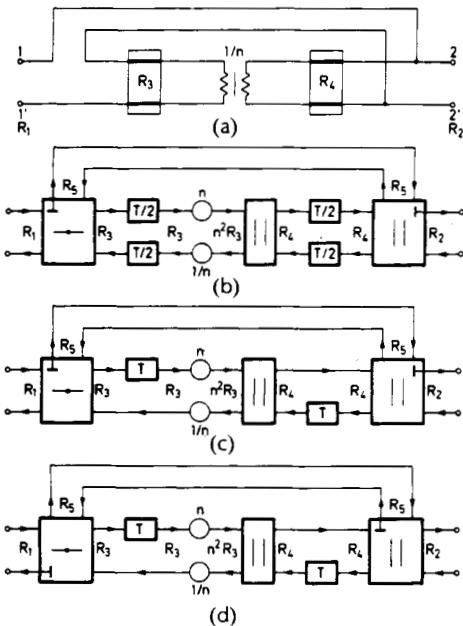


Fig. 55. (a) An alternative realization of a Brune-type section. (b) A corresponding WDF realization. (c) A structure derived from (b) by applying an equivalence of Fig. 37. (d) An alternative WDF realization of (a).

$$R_5 = R_2 R_4 / (R_2 + R_4) \quad R_1 = R_3 + R_5.$$

It is easily verified that there is no delay-free directed loop in any of the circuits of Fig. 55(b)–(d). Furthermore, these arrangements may be used in a chain with structures such as those discussed in Section VI.

Each one of the circuits of Fig. 55(b)–(d) requires five multipliers, while the circuit of Fig. 55(a) comprises only 3 degrees of freedom. Hence, two relations exist between the various multiplier coefficients. One of these is that two of the multipliers have reciprocal coefficients (which could even be replaced by two equal ones if use were made of the equivalence of Fig. 46). The other one is of more complicated nature. In any case, after quantization of the multiplier coefficients these relations will usually be satisfied only with some more or less pronounced error.

Thus starting from the given R_1 and taking into account the principles explained in item 5 of Subsection III-B4 one can, e.g., consecutively determine new resistances R'_3 , R'_5 , R'_2 , R'_4 , and R'_6 that differ somewhat from the original resistances R_3 , R_5 , R_2 , R_4 , and $n^2 R_3$, respectively. With n and $1/n$ actually taking the quantized values n' and $1/n''$, respectively, the pair of reciprocal multipliers in Fig. 55(b)–(d) is thus to be replaced in the way shown in Fig. 56. With $G_3 = 1/R'_3$ and $G_6 = 1/R'_6$, the instantaneous pseudopower absorbed by this arrangement is

$$(a_1^2 - b_1^2) G_3 + (a_2^2 - b_2^2) G_6 = a_1^2 (G_3 - n'^2 G_6) + a_2^2 (G_6 - G_3/n''^2)$$

which is guaranteed to be nonnegative if

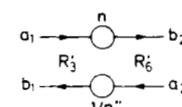


Fig. 56. Arrangement corresponding to the pair of reciprocal multipliers in Fig. 55(b)–(d) after coefficient quantization.

$$n' \leq \sqrt{R'_6/R'_3} \leq n''. \quad (107)$$

Hence, if the quantization of all multiplier coefficients is done in such a way that (107) is fulfilled, pseudopassivity remains satisfied [114], [305] and hence also all stability properties discussed in Section VII. However, since one cannot always return from the structures of Fig. 55(b)–(d) to that of Fig. 55(a) if all multiplier coefficients are chosen freely, the arguments used for guaranteeing that at the attenuation zeros the loss sensitivity is zero with respect to any coefficient do no longer strictly hold, but this aspect is not of such decisive importance as that of stability, especially as sensitivity will usually remain quite satisfactory.

By means of the well-known Brune process, any positive-real function $Z(\psi)$ can be realized by means of a structure that is a chain of shunt and series branches (composed of inductances, capacitances, resistances, parallel resonant circuits, and series resonant circuits) and of Brune sections. Hence, applying the principles for realizing WDF ladder structures, any positive-real function $Z(\psi)$ can be realized by making use, if required, also of the method explained with respect to Fig. 55 [306]. Furthermore, since realizing $Z = Z(\psi)$ amounts in fact to realizing a reflectance $(Z - R)/(Z + R)$ and since any stable real transfer function $H(\psi)$, with $|H(j\phi)| \leq 1$ for all ϕ (cf. (3)), can be realized in the form of such a reflectance, with Z a positive-real function, any restriction concerning the nature of the transfer function to be realized as a WDF structure can be overcome this way [306]. The resulting structures are canonically in number of delays.

While the approach just explained is based on the use of reflectances, one may also extend the realization of transmittances (cf. Section VI) by including general zeroth-, first-, and second-order sections. A section of order zero consists either of an ideal transformer or a gyrator and thus poses no problem. Using results on the factorization of the scattering transfer matrix [183] and the scattering hybrid matrix of a lossless two-port [307] it can be shown [301] that lossless first- and second-order sections of the most general type required can be synthesized in the way shown in Figs. 57(a) and 58(a), respectively (where the symbol for the QUARLs corresponds to that used in Fig. 51(b)). From these, the WDF realizations of, respectively, Figs. 57(b) and 58(b),

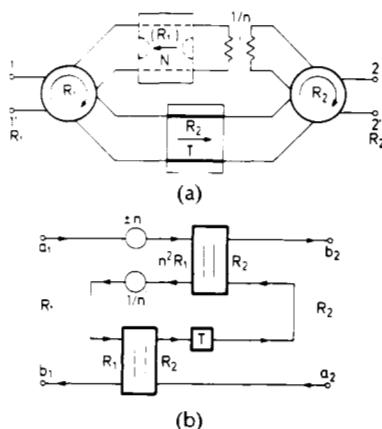


Fig. 57. (a) A general first-order section (reference filter domain), N being either a simple through-connection or a gyrator of gyration constant R_1 . (b) Corresponding WDF structure without delay-free path from input to output terminal of port 2, the upper and lower sign in $\pm n$ corresponding to the first and second possibility for N , respectively.

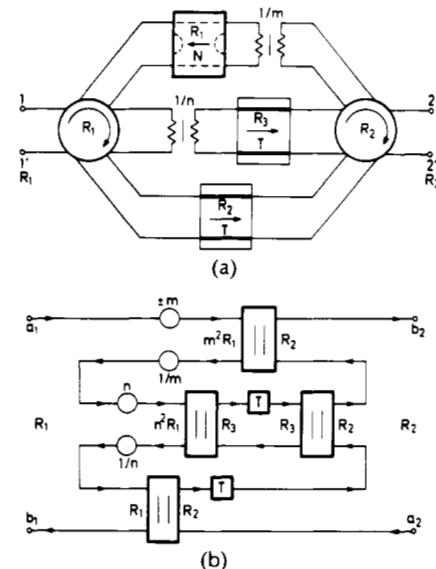


Fig. 58. (a) A general second-order section (reference filter domain), N being either a simple through-connection or a gyrator of gyration constant R_1 . (b) Corresponding WDF structure without delay-free path from input to output terminal of port 2, the upper and lower sign in $\pm m$ corresponding to the first and second possibility for N , respectively.

which are canonically in the number of delays, are immediately obtained. For each pair of multipliers in these realizations the same considerations as those given above (cf. Fig. 56 and the related discussion) apply for ensuring pseudopassivity and thus all aspects of stability.

In the structures of Figs. 57(a) and 58(a), one of the port resistances, say R_1 , may be imposed arbitrarily. The parameter R_2 occurs at several places, in particular in such a way that in the resulting WDF two-ports no delay-free path is created from the input to the output terminal of the respective port 2. This way the problem of realizing as WDFs general reference lossless two-ports (thus, in particular, general transfer functions) by means of a chain (cascade) synthesis approach is fully solved in a way that fits into the theory explained in Section VI.

Note that many further structures in addition to those of Figs. 57 and 58 can be given. In particular (and a similar comment holds for Fig. 55), abandoning the requirement just discussed concerning delay-free paths one can give structures for which the port resistances may be chosen freely not only at port 1, but also at port 2. (The simplest, although not necessarily the best, way for doing this is to provide a suitable two-port adaptor to the right of ports 2.) The structure of Fig. 57(b) is closely related to that of Type II in Fig. 3 of [308], and a reference filter interpretation of Type III in that same figure can also be given (cf. also Section IX-I). In fact, these two figures in [308] have directly inspired the search for the solutions given in Figs. 57 and 58.

A quite different approach to the problem of realizing general transfer functions has previously been published [114], [305]. In this approach, however, a sufficient number of unit elements (or QUARLs) must appear in the chain structure of the reference domain. These unit elements could be chosen in such a way that they alter the original transfer function only by a constant delay, but it is preferable to take advantage of their inherent filtering capability (as explained in a similar context in Section VI-D).

Various other approaches to solving the problem of realizing more general transfer functions have also become known. Some of these deal with reciprocal sections [302]–[304], [309]–[311], others use generalized-adaptor concepts [226], [254], [312]–[314].

B. Realization of Wave Digital Filters by Factorization of the Scattering Matrix

A lossless two-port in the reference filter domain N can also be synthesized by factorization of the scattering matrix [32], [307]. The resulting structure is shown in Fig. 59(a)

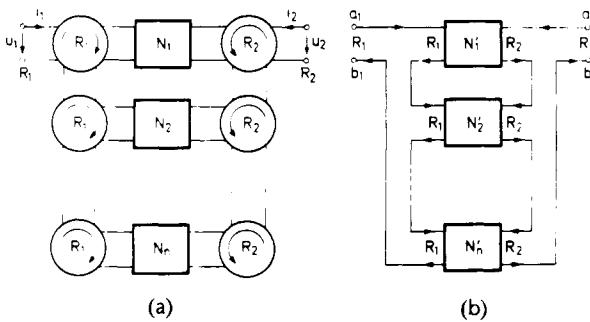


Fig. 59. (a) Synthesis of a classical two-port by scattering matrix factorization. (b) Corresponding WDF structure.

where N_1 to N_n are lossless two-ports of degree lower than that of N and where one may choose $R_2 = R_1$. If g_1 to g_n are the Hurwitz polynomials of N_1 to N_n , respectively, then the Hurwitz polynomial of N is $g = g_1 g_2 \cdots g_n$. The decomposition can, therefore, be carried out in such a way that the polynomials g_1 to g_n and thus the two-ports N_1 to N_n are of degree at most equal to 2.

The structure of Fig. 59(a) gives rise to the WDF structure of Fig. 59(b) where N'_1 to N'_n are the WDF two-ports corresponding to N_1 to N_n , respectively. Using the results of Section IX-A, the structure of Fig. 59(b) is thus always realizable.

If N is symmetric or antimetric, the factorization of the scattering matrix required to arrive at Fig. 59(a) can even be carried out in such a way that N_1 to N_n are again symmetric or (except for two simple sign inversions) antimetric, respectively [307]. The realization then becomes very simple using the results of Section VI-A and Fig. 55 (although with the three-port parallel adaptors in Fig. 55(b) and (c) and the three-port series adaptor in Fig. 55(d) replaced by corresponding unconstrained ones), respectively [117], [315]. In particular, in the symmetric case, if S' and S'' are canonic reflectances (cf. Section VI-A) one obtains simply

$$S' = S'_1 S'_2 \cdots S'_n \quad S'' = S''_1 S''_2 \cdots S''_n$$

where S'_i and S''_i , for $i = 1$ to n , are the canonic reflectances of N_i . Hence any factorization of S' and S'' leads to a solution, which however does not appear to offer advantages over those obtained by applying directly the results of Figs. 20 and 23.

On the other hand, whether or not N is symmetric or antimetric, the approach according to Fig. 59 can become attractive if g is available in simple factored form. An application of this is discussed in Section IX-C.

C. Nonrecursive Wave Digital Filters

Making use of (2), i.e., of

$$z = (1 + \psi)/(1 - \psi)$$

the transfer function of any nonrecursive filter can be written in the form

$$S_{21} = f/g \quad (108a)$$

$$g = (\psi + 1)^k \quad (108b)$$

where g is a simple Hurwitz polynomial whose degree k is equal to the degree of S_{21} in z and where $f = f(\psi)$ is also a polynomial in ψ . By including in f an appropriate constant factor one can ensure that

$$|S_{21}(j\phi)| \leq 1, \quad \text{for all } \phi \quad (109)$$

(cf. (3)) and thus that there exists a real polynomial $h = h(\psi)$ such that

$$gg_* = hh_* + ff_*$$

where g_* designates again the paraconjugate of g , etc. (cf. Subsection VI-A2).

The polynomials f , g , and h determine the scattering matrix, S , of a lossless two-port [32]. Since g is available in the simple factored form (108b), the approach of Fig. 59 leads to a realization by means of $k + 1$ two-ports N_1 to N_{k+1} of which the first k are of degree 1 and the last one of degree 0. Using results obtained in [307] it can be shown [306] that the factorization of S can be carried out in such a way that N_i , for $i = 1$ to k , can be synthesized as given in Fig. 60(a) (cf. Fig. 51(b)) or with the arrow reversed. Fig. 60(a) leads to the WDF realization of Fig. 60(b) or, equiv-

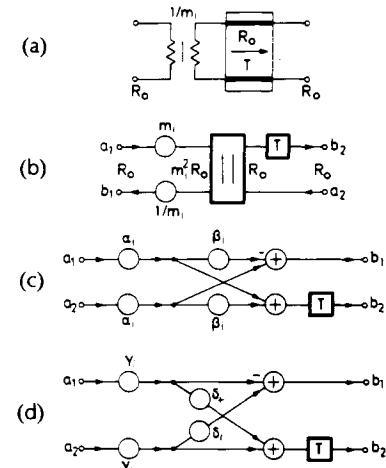


Fig. 60. (a) A two-port N_i , for $i = 1$ to k , required for synthesizing a nonrecursive wave digital filter according to Fig. 59. (b) to (d) Equivalent WDF realizations, with α_i , β_i , γ_i , and δ_i given according to (110).

alently, to those of Fig. 60(c) and (d) where

$$\alpha_i = 2m_i/(m_i^2 + 1) \quad (110a)$$

$$\beta_i = (m_i^2 - 1)/2m_i \quad (110b)$$

$$\gamma_i = (m_i^2 - 1)/(m_i^2 + 1) \quad (110c)$$

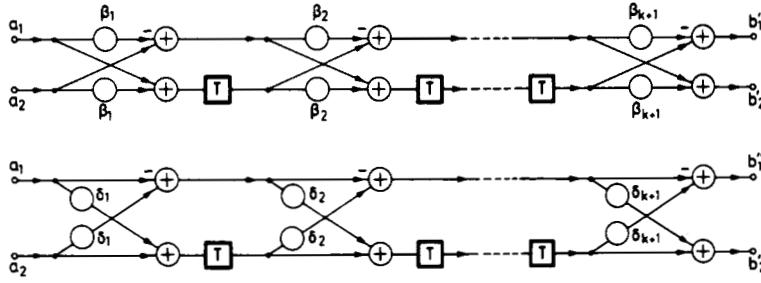


Fig. 61. Two structures for realizing nonrecursive WDFs.

$$\delta_i = 2m_i / (m_i^2 - 1). \quad (110d)$$

Furthermore, the constant two-port N_{k+1} is also an ideal transformer (although possibly followed by a gyrator of gyration constant R_0 , but such a gyrator may be ignored), which also leads to the realizations of Fig. 60(b)–(d) except for the fact that the delay T is now absent. Finally, if we introduce structures such as those of Fig. 60(c) and (d) (and the corresponding one for N_{k+1}) into Fig. 59(b) and if we move all multipliers α_i and/or γ_i to the output (cf. Fig. 44(b)), where they may simply be dropped, we finally arrive at the realizations of Fig. 61 [306]. Clearly, the structures of Fig. 61 are quite similar to those known as inverse filters [316]. (Notice, however, the minus signs at one of the inputs of each adder appearing in the two top lines.)

In Fig. 61 we have marked the output signals by b'_1 and b'_2 and by b''_1 and b''_2 , respectively. These are related to the original signals b_1 and b_2 by

$$\begin{aligned} b_1/b'_1 &= b_2/b'_2 = \alpha \\ b_1/b''_1 &= b_2/b''_2 = \gamma \\ \alpha &= \alpha_1 \alpha_2 \cdots \alpha_{k+1} \\ \gamma &= \gamma_1 \gamma_2 \cdots \gamma_{k+1}. \end{aligned}$$

Obviously, the structures of Fig. 61 are more complicated than those of conventional nonrecursive realizations. Nevertheless, they have at least two advantages, which may be of relevance in some cases. First, if the constant in f is chosen in such a way that equality is reached in (109) at the transmission maxima, the sensitivity argument holds again at these maxima. Hence, the accuracy requirement for the coefficients is reduced and, like for lattice filters, it is hardly necessary to check the passband behavior during the process of discrete optimization. Secondly, complementarity holds again as discussed in Section IV-B. Thus the structures of Fig. 61 can serve as perfect branching filters.

D. Open-Circuited and Short-Circuited Reference Filters

In classical circuits one considers not only filters that are resistively terminated at both ends, as we have done so far, but also others that are either open-circuited or short-circuited at one terminating port. In this case, however, the passband sensitivity is no longer as good as for the former type of filter. Nevertheless, all principles for deriving WDFs from such reference filters remain valid except that the port that is not resistively terminated must now be such that no delay-free path leads internally from the input to the output terminal of that port [154], [155]. The signal in the external path terminating that port is equal to the desired output

signal. Since passivity is preserved, the various stability properties remain guaranteed except for the stability under looped conditions.

The simplest type of filter that is open-circuited at the far end is the one of Fig. 62(a) (related to that of Fig. 36(a)).

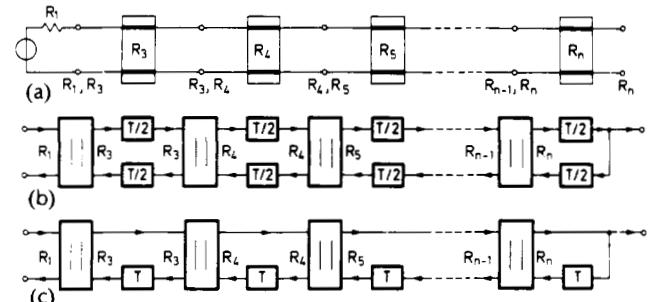


Fig. 62. (a) A filter circuit similar to that of Fig. 36(a), but open-circuit at the right port. (b) WDF structure derived from (a). (c) An essentially equivalent version of (b).

Two corresponding WDFs are shown in Fig. 62(b) and (c) (the latter being obtained as an essentially equivalent variant of the former by making use of Fig. 37 or, equivalently, directly from the reference filter after replacing in Fig. 62(a) the unit elements by appropriate QUARLs). The structure of Fig. 62(c) corresponds to the simplest type of filters sometimes referred to as lattice or ladder filters [85] (not to be confused with lattice or ladder WDFs, i.e., WDFs derived from lattice or ladder reference filters!).

More precisely, if one uses for the adaptors in Fig. 62(c) a realization according to Table 10D one has immediately a so-called one-multiplier lattice structure (more precisely: one multiplier per section). The two-multiplier and three-multiplier versions of such filters can also be easily obtained by inserting appropriate ideal transformers between the various unit elements of the structure of Fig. 62(a) [306] (as can indeed always be done without restriction, in fact also for the structures of Fig. 36, since it produces no change in the transmittances except, at most, for a multiplication by a constant). Since such lattice and ladder filters are also WDFs it is obvious that they enjoy all the stability properties of the latter so that a separate theory [317] is in fact not required.

From a structure such as that of Fig. 62(c) (or from that of Fig. 36) or any of its equivalents, filters with arbitrary transfer functions can be obtained by applying weighted taps at a sufficient number of independent locations, as is, e.g., described in [85]. The recursive part of such a filter is then

still that of a WDF. Hence, the same simple means as for other WDFs are sufficient to ensure all stability properties, except for that concerning looped stability (since under looped conditions (Fig. 47), a nonrecursive part of a digital filter can give rise to a recursive behavior). It should be stressed, however, that if one has recourse at all to structures such as those discussed here, it is usually preferable to base the design on Fig. 36 rather than Fig. 62, and this for the reasons explained above.

E. State-Space Wave Digital Filters

As already mentioned in [4], one simple possibility of obtaining a WDF of degree $\leq n$ is to start from any given LC filter structure and to redraw the resulting structure, say, as a constant lossless $(n+2)$ -port N , whose ports 1 and 2 are terminated by a resistive source and a resistance, respectively, and whose remaining ports are terminated by capacitances and inductances (Fig. 63(a)). Applying to N the

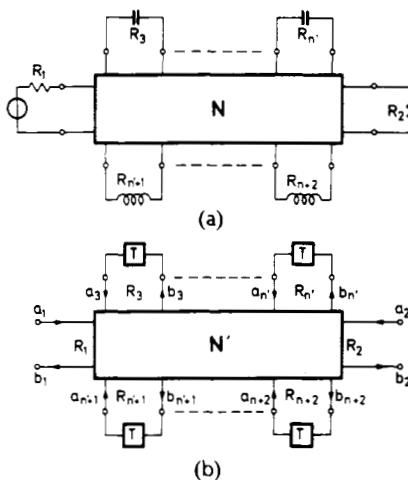


Fig. 63. (a) Representation of a reference filter as a passive (usually lossless) constant multiport with appropriate terminations. (b) Corresponding WDF structure (the sign inverters due to the inductances being included in N').

expressions (27), with n replaced by $n+2$, we can express b_1 to b_{n+2} in terms of a_1 to a_{n+2} , thus defining a wave $(n+2)$ -port N' . Clearly, N' plays the role of a *global adaptor*, and if we write for the capacitances and inductances expressions corresponding to (18), we derive from Fig. 63(a) the WDF structure of Fig. 63(b) (the sign inverters originating from the inductances being assumed to be included in N'). Furthermore, if we choose $t_0 = 0$ in (19), put $a_2 = 0$, ignore b_1 , and make appropriate eliminations, the final result can be written in the form

$$\mathbf{a}(mT + T) = \mathbf{A}\mathbf{a}(mT) + \mathbf{B}a_1(mT) \quad (111a)$$

$$b_2(mT) = \mathbf{C}\mathbf{a}(mT) + \mathbf{D}a_1(mT) \quad (111b)$$

where \mathbf{a} is the vector composed of a_3 to a_{n+2} and where \mathbf{A} , \mathbf{B} , \mathbf{C} , and \mathbf{D} are constant $n \times n$, $n \times 1$, and $1 \times n$ matrices and a scalar, respectively.

Clearly, (111) corresponds to the state-space description of the WDF considered, and a WDF directly implemented according to (111) will therefore be called a *state-space wave digital filter*. Furthermore, the passivity of N leads to the requirement that the matrix

$$1 - \mathbf{R}^{1/2} \mathbf{A}^T \mathbf{R}^{-1} \mathbf{A} \mathbf{R}^{1/2} \leq 1 \quad (112)$$

is nonnegative definite, usually even positive definite, which we also express by writing

$$\mathbf{R}^{-1/2} \mathbf{A} \mathbf{R}^{1/2} \leq 1 \quad (113a)$$

or

$$\mathbf{R}^{-1/2} \mathbf{A} \mathbf{R}^{1/2} < 1 \quad (113b)$$

respectively. In these expressions, \mathbf{R} is the diagonal matrix composed of R_3 to R_{n+2} . Thus if $R_3 = R_4 = \dots = R_{n+2}$, the three expressions (112) and (113) may be replaced by

$$1 - \mathbf{A}^T \mathbf{A} \leq 1 \quad (114a)$$

$$\mathbf{A} \leq 1 \quad (114b)$$

and

$$\mathbf{A} < 1 \quad (114c)$$

respectively. The results expressed by (111) to (114) can easily be extended to more general situations where N is not lossless, although passive (in which case N could even be replaced by a lossless multiport terminated by additional resistances at some of its ports [32]). Furthermore, we could also have assumed the desired transfer function to be a reflectance instead of a transmittance, in which case b_2 in (111b) is simply to be replaced by b_1 .

On the other hand, assume that a state-space description of the form (111) is given, with \mathbf{A} satisfying (114c). It can be shown that one can always find constants c_1 and c_2 such that the matrix \mathbf{M} defined by

$$\mathbf{M} = \begin{pmatrix} \mathbf{A} & \mathbf{B}' \\ \mathbf{C} & \mathbf{D}' \end{pmatrix}, \quad \mathbf{B}' = c_1 \mathbf{B}, \quad \mathbf{C} = c_2 \mathbf{C}, \quad \mathbf{D}' = c_1 c_2 \mathbf{D}$$

satisfies the condition $\mathbf{M} \leq 1$. Consequently, as follows from standard network results [32], the matrix \mathbf{M} can be synthesized as the scattering matrix of, e.g., a constant passive $(n+1)$ -port (that could again be replaced by a lossless multiport terminated by resistances on some of its ports). After properly terminating this $(n+1)$ -port with capacitances and/or inductances, we obtain a passive circuit whose corresponding state-space WDF is described by

$$\mathbf{a}(mT + T) = \mathbf{A}\mathbf{a}(mT) + \mathbf{c}_1 \mathbf{B}a_1(mT)$$

$$b_1(mT) = \mathbf{c}_2 \mathbf{C}\mathbf{a}(mT) + \mathbf{c}_1 \mathbf{c}_2 \mathbf{D}a_1(mT).$$

Hence, if we let the input terminal of this state-space WDF be preceded by a multiplier $1/c_1$ and the output terminal be followed by a multiplier $1/c_2$, the overall state-space description is the same as the one originally given.

Therefore, we conclude that after inserting, if required, two appropriate multipliers at the input and at the output, respectively, any state-space digital filter with $\mathbf{A} < 1$ can be realized as a state-space WDF with identical state-space description. In that sense, state-space digital filters with $\mathbf{A} < 1$ can be considered to belong to the class of state-space WDFs. It is thus clear that for state-space digital filters with $\mathbf{A} < 1$, all stability properties discussed in Section VII (except, possibly, stability under looped conditions) can be ensured, thus not only the properties considered in [318], [320], but also forced-response stability [306], [319] and that $\mathbf{A} < 1$ can even be replaced by the less stringent requirement (113b) [321].

Some further light on the advantages that can be gained

from using WDFs is shed by the following observation [306]. It is known that in the case of L_2 scaling the dynamic range can be optimized using two positive definite matrices \mathbf{K} and \mathbf{W} . The optimization can be carried out in particular if only the average wordlength is prescribed [322]. If this is the case, the optimum is attained if \mathbf{K} and \mathbf{W} are simultaneously diagonal, which can always be achieved by proper similarity transformations. In state-space WDFs derived from lattice reference filters these desired forms are in fact automatically obtained, the matrices \mathbf{K} and \mathbf{W} being then diagonal matrices formed of port resistances and port conductances, respectively. In other types of state-space WDFs derived from reciprocal lossless two-ports or multiports, the same remains true if the theory is appropriately generalized and if the noise considered is the total noise at all outputs [306], [315].

The implementation of state-space WDFs can be rendered more compact and thus more efficient by appropriate manipulation of the basic equations [226], [254]. Furthermore, the same simple approach mentioned in Section VIII-C in relation to the use of distributed arithmetic can also be employed for obtaining discretely optimized versions of the coefficients in the state equations [323]–[327].

F. Second-Order Sections for Cascade Synthesis of Digital Filters

The approach discussed in the last paragraph of Section IX-D suggests that general second-order sections can also be obtained by using the recursive part of any simple second-order WDF (consisting simply of, say, a resonant circuit and a resistance) and by applying tapping at appropriate locations. A second-order section obtained this way is shown in Fig. 64 [321], [328] together with expres-

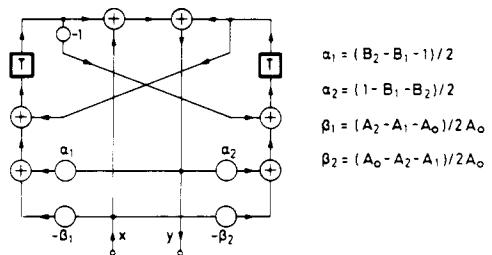


Fig. 64. Generally usable second-order section for which all stability problems (except that under looped conditions) can be solved in the same way as for WDFs.

sions giving the multiplier coefficients $\alpha_1, \alpha_2, \beta_1$, and β_2 in terms of the coefficients A_0, A_1, A_2, B_1 , and B_2 of the transfer function

$$H(z) = (A_2 + A_1 z + A_0 z^2) / (B_2 + B_1 z + z^2).$$

Clearly, this section enjoys all the stability properties of WDFs, including forced-response stability (although not necessarily that of stability under looped conditions) if the same simple means as described in Section VII are applied. This substantial advantage is achieved at only the slight extra cost of two adders per section. There are no added restrictions on the coefficients A_0, A_1, A_2, B_1 , and B_2 , i.e., sections according to Fig. 64 can freely be used in conventional cascade synthesis of digital filters. Closely related

sections have also been described and analyzed elsewhere [329]–[334].

G. Complex Wave Digital Filters

While one is usually interested in real circuits, complex digital filters also play some role. Corresponding concepts can also be applied to the design of WDFs. Such *complex WDFs* [335]–[337] have to be derived from complex reference filters, for which many results are available [32]. It has turned out, however, that in order to lead to useful WDFs, classical complex circuits must have the property of *one-realness*, or must at least be reducible in a simple way to circuits having this property [335]. One-realness is not very restrictive; it implies in particular that the relevant impedances are real for $\psi = 1$.

Until now, no example has been found in which complex WDFs would lead to a more efficient design than real WDFs. This holds true at least in the one-dimensional case, to which we are restricting ourselves so far, but may be different for multidimensional WDFs (cf. Section XI).

H. Wave Digital Filters Based on the Use of Power Waves

So far, we have only considered WDFs based on the use of voltage waves since this leads to the simplest realization. Nevertheless, there is also some interest to use *power waves* as basis for the analogy between the reference domain and the digital domain [73], [74], [106], [200], [308], [338]–[345], some such filters being also referred to as *orthogonal filters* [73], [74], [106], [200], [308], [338]–[342].

There is, however, no essential difference between using power waves or voltage waves. Indeed, denoting temporarily voltage waves by a' and b' and the corresponding power waves by a and b , we have instead of (5)

$$a = (v + Ri)/2\sqrt{R} \quad b = (v - Ri)/2\sqrt{R}$$

and therefore

$$a = a'/2\sqrt{R} \quad b = b'/2\sqrt{R}.$$

Consequently, a and b are related to a' and b' as shown in Fig. 65, i.e., by means of a pair of reciprocal multipliers.

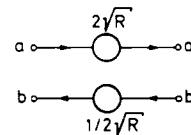


Fig. 65. Visualization of the relationship between power waves, a and b , and the corresponding voltage waves, a' and b' .

Therefore, passing from one type of waves to another simply amounts to inserting appropriate ideal transformers in the original reference filter. Hence, any *voltage-wave WDF* can be interpreted as a *power-wave WDF* and vice versa.

For WDFs based on power waves, all design principles involving the use of adaptors remain the same (including those concerning constrained and unconstrained adaptors), i.e., the representation of a WDF structure by means of adaptors is unchanged, except that the adaptor equations derived in Section III-B have to be modified. One might expect that for an n -port adaptor we now need n^2 multipliers

cations per cycle, but this number is reduced to $2n$ if the adaptor equations are written in the following form [345]:

$$b_v = \pm(\gamma_v a_0 - a_v), \quad v = 1 \text{ to } n \quad (115a)$$

$$a_0 = \gamma_1 a_1 + \gamma_2 a_2 + \cdots + \gamma_n a_n \quad (115b)$$

where the upper sign together with

$$\gamma_v = \sqrt{2G_v/G_0}, \quad G_0 = G_1 + G_2 + \cdots + G_n$$

holds in the case of a parallel adaptor, and the lower sign together with

$$\gamma_v = \sqrt{2R_v/R_0}, \quad R_0 = R_1 + R_2 + \cdots + R_n$$

in the case of a series adaptor, $G_v = 1/R_v$, holding as in (30). A disadvantage of writing the equations in the form (115) is that the multiplications required by (115a) can only be carried out after those required by (115b) are completed. Furthermore, instead of (31) we now have

$$\gamma_1^2 + \gamma_2^2 + \cdots + \gamma_n^2 = 2. \quad (116)$$

This implies that we cannot eliminate, in a simple manner, one of the γ_v , but this kind of restriction is unavoidable in the case of WDFs based on power waves.

In a more compact notation, the scattering matrix corresponding to (115) can be written as

$$\mathbf{S} = \pm(\boldsymbol{\gamma} \boldsymbol{\gamma}^T - \mathbf{1}), \quad \boldsymbol{\gamma}^T = (\gamma_1, \gamma_2, \dots, \gamma_n)$$

and for the corresponding dissipation matrix we thus obtain

$$\mathbf{1} - \mathbf{S}^T \mathbf{S} = (2 - \boldsymbol{\gamma}^T \boldsymbol{\gamma}) \boldsymbol{\gamma} \boldsymbol{\gamma}^T.$$

This matrix is zero (i.e., \mathbf{S} is orthogonal) if (116) is satisfied, but is still at least nonnegative definite if the actual γ_v (say, after discrete optimization) are chosen such that $\boldsymbol{\gamma}^T \boldsymbol{\gamma} \leq 2$. Hence, all stability aspects discussed in Section VII then remain preserved.

The simplest adaptor is, of course, one for $n = 2$; except, possibly, for some change in sign the elementary operation implied by this is a rotation in the geometrical sense and can be implemented by means of the CORDIC algorithm. It has been shown that all other operations needed can be reduced to such elementary operations, thus to the use of CORDIC processors [200], [273], [308], [341]–[343].

Actually, that such a result as well as obvious generalizations thereof hold can be shown to be an immediate consequence of the fact that any real orthogonal matrix of arbitrary order can be written (except, possibly, for some sign inversions) as product of elementary orthogonal matrices corresponding each to a *plane rotation*. (Indeed, using the Givens algorithm [346] any real matrix \mathbf{A} can be written as product of a triangular matrix \mathbf{B} and of a certain number of elementary orthogonal matrices corresponding to plane rotations; if \mathbf{A} is orthogonal, \mathbf{B} is also orthogonal, thus necessarily diagonal with diagonal entries equal to ± 1 .) Note that an orthogonal matrix of order n corresponding to a plane rotation is defined to comprise one principal submatrix of order 2 representing a rotation in the plane determined by the corresponding axes, the remaining $n - 2$ diagonal entries being equal to 1 and all other remaining entries equal to 0.

The disadvantages of power-wave WDFs are the increased number of multipliers and the fact that relationships such as (116) must hold, which, except in unusual circumstances, cannot be satisfied exactly with finite word-

lengths. The latter implies that multiplier coefficients cannot be changed independently and thus that the arguments given in Section II-C for guaranteeing zero sensitivity at the attenuation zeros do not strictly hold, i.e., that the sensitivity properties are not as good as for voltage-wave WDFs.

For power-wave WDFs, expressions such as (104) and (105) hold except that all G_v have to be replaced by unity. These new expressions are thus special cases of the old ones, and in that sense, voltage-wave WDFs are more general than power-wave WDFs. It is precisely the added freedom due to the possibility of choosing the G_v different from 1 which leads to the simplicity of WDFs, yet allows them to have all the excellent stability properties resulting from the existence of a convenient Lyapunov function. This function may be considered to be a vector norm generalized with respect to that obtained if $G_v = 1$ for all v .

Linear bounded-real (LBR) digital filters [55], [347] are also power-wave WDFs. The LBR structures that have been described are again composed of individual two-ports (called two-pairs) in a chain arrangement. The individual sections are lossless (pseudolossless) between ports (external losslessness), but not necessarily in as far as their detailed inner structure is concerned (internal losslessness, orthogonality), contrary to what is the case for those given in, or following from, [73], [74], [106], [200], [308], [338]–[345]. The situation is the same as that for the voltage-wave WDF approach discussed in the last paragraph of Section VI-B. In particular, if one requires the individual two-ports to be such that internal losslessness (i.e., orthogonality, and hence losslessness if the additional ports to which delays are connected are also taken into account) holds as well, the restricted class of structures then available does not appear to be different from that obtainable by the other methods [226].

It should be mentioned that more general linear combinations between voltages and currents have been examined for the realization of digital filters [99], [159], [163], [348]–[351]. However, again one does not arrive at truly different structures if the condition of internal losslessness is imposed [226], [352].

I. Digital Filters Based on Simply Connected Signal-Flow Networks

Principles for a possible generalization of the concept of WDFs have already been presented in [75]. Such generalized WDFs are signal-flow networks that had been called *simply connected*. More specifically, the corresponding signal-flow diagrams are composed of signal-flow *building blocks* for which the number of input leads (rays) is not required to bear any relationship to the number of output leads (rays). The building blocks are interconnected with precisely two leads, one input and one output lead. To each such node is assigned a *node weight*. All previous definitions for concepts such as pseudopower, pseudopassivity, pseudolosslessness, etc., carry over in an obvious manner, the node weights entering the pseudopower expressions explicitly in a similar manner as the port conductances in the case of WDFs. General laws, such as conservation of pseudopower, also still hold, and the same is true for all stability aspects under linear as well as finite-arithmetic conditions.

Clearly, WDF circuits are special cases of such more general structures. For WDFs, the building blocks are adaptors and delays, and these are port-wise interconnected. Thus each building block has as many input leads as output leads. These are grouped in pairs, and the interconnection is such that the rules given in Section IV-A are respected. In particular, the two nodes interconnecting two ports have the same node weight, equal to the port conductance. Orthogonal filters thus follow as further special cases if all node weights are equal to unity.

WDFs can be derived from reference filters, but, although the advantages that could be gained are obvious, a corresponding general design theory for the generalized structures mentioned above is not yet available [353]. Nevertheless, an interesting subclass, in fact for all node weights equal to unity, has recently been described [199]. Other multivariable extensions have also been considered [73], [354].

J. Wave Digital Filters Derived from Active Circuits

Suitable active structures can also be used as reference filters for WDFs. One type of such structures are those involving supercapacitances and superinductances [89], [355], [356] as introduced first for realizing low-sensitivity active filters by appropriately transforming passive structures [357]. Other approaches use specific *RC*-active designs as points of departure [358]–[363]. While in all these methods certain aspects of stability can be taken into account it seems difficult to cover the full range of stability properties that have been mentioned in Section VII to hold for realizations derived from passive reference structures.

X. WAVE DIGITAL FILTERS FOR SPECIAL APPLICATIONS

A. Multirate Wave Digital Filters

Multirate WDFs can be designed very efficiently in a number of cases. The simplest case is that of a *lattice WDF* with bireciprocal characteristic function, such as that of Fig. 34. In many applications the output sampling rate $F = 1/T$ of such a filter has to be twice that of the two inputs (in the example considered, e.g., 48 and 24 kHz, respectively), thus corresponding to a case of interpolation. In principle, the structure would thus have to operate at the rate F , but since one of the branches is odd in z and the other one even, the additions and multiplications have to be carried out only at the lower rate $F/2$, amounting to a 50-percent saving in the arithmetic units. The doubling of the sampling rate is then achieved by interleaving, i.e., the output adder that would have to be provided according to Fig. 23(b) can be replaced by a simple switch, as is in fact shown in Fig. 34(b).

The situation is in fact very similar if a filter such as that of Fig. 34(a) is used in the opposite direction of transmission, i.e., with one input at the high rate $F = 1/T$ and two outputs at the rate $F/2$ (decimation). In this case we simply have, e.g., to reverse the flow in all the signal paths of Fig. 34, and the switch then distributes the consecutive samples alternately to the upper and lower branch. These branches thus have to operate again only at the lower rate $F/2$.

While the principles just discussed hold for sampling rate alterations by 2 or $1/2$, a suitable *generalization* leads again to substantial savings also for other changes in rate [145],

[146]. For this the number of all-pass branches is increased according to the desired ratio of change. The method is closely related to the polyphase approach [142], [143], yet allows one to draw particular benefit, as in [144], from the advantageous properties of WDFs. Thus using a skilfully chosen computational procedure the design yields filters of high performance, yet of remarkably low complexity.

For WDFs derived from ladder reference filters, methods of similar efficiency do not seem possible. Nevertheless, even for *multirate ladder WDFs* a specific design theory has been developed [156] that still leads to substantial savings compared to standard WDFs employed for the same filtering purpose.

For certain applications, e.g., for *subband coding*, multirate digital filters are desired that make it possible to first split a signal into a number of partial bands (either with equal absolute or, preferably, equal relative bandwidths) and then to reconstruct this signal without aliasing error. For this application, WDFs have again turned out to be particularly advantageous [103]. In principle, ladder or lattice WDFs, in fact even of real or complex type, can be used, but real lattice WDFs appear to be usually by far the most advantageous.

B. Adjustable and Adaptive Wave Digital Filters

WDFs remain stable under linear conditions as long as *all* the γ_i (including those corresponding to dependent ports) discussed in Subsections III-b2 and III-B3 remain > 0 . In addition, the means that guarantee absence of parasitic oscillations and ensure forced-response stability are independent of the particular values chosen for the multiplier coefficients. Hence, WDFs can easily be made adjustable without endangering stability. Some related aspects have been considered in the literature [364]–[369].

Furthermore, in view of these excellent stability properties and the fact that very regular WDF structures are available, properly selected WDFs should be good candidates for adaptive digital filtering. That this is indeed the case follows on the one hand from the fundamental role that lattice digital filters play for adaptive signal processing [46], [370], and on the other from the fact pointed out in Section IX-D that so-called lattice filters are actually WDFs of very simple type. The interest of power-wave WDFs (and generalizations thereof) for adaptive processing has also been pointed out [73], [105], [199], [200], [344]. It seems, however, that not all interesting possibilities available have been investigated so far.

Note in this respect that for ensuring stability in adaptive filters it is not sufficient to guarantee that the circuit would be stable if the set of coefficients remained constant at any of the values reached when the filter is operating. On the other hand, a requirement that stability must be ensured for any time-varying change of the coefficients within the range available is much too strict, contrary to what is sometimes believed.

C. Wave Digital Hilbert Transformers

Hilbert transformers are closely related to the concept of complex filtering. We have seen in Section IX-G that the latter concept can also be used successfully in the realm of WDFs, and it is thus to be expected that WDFs offer an

attractive alternative for realizing Hilbert transformers. Remarkably efficient designs have been obtained, especially again when lattice WDFs are used [371].

D. Equalizers and Related Circuits

The realization of phase and delay equalizers, i.e., of all-pass circuits has been covered in Section V. In communications engineering one also frequently needs *loss equalizers* and *balancing networks* [372], [373]. In classical circuits these are realized by means of arrangements that essentially involve an impedance composed of a certain number of inductances, capacitances, and resistances, usually in a ladder-type configuration. Such circuits can in general be implemented very easily in WDF form. Absence of limit cycles and forced-response stability can then be guaranteed by the same means as in other WDFs.

As an example consider a loss equalizer, which is classically realized as a bridged-T configuration. Except for a factor 1/2, the resulting transmittance S is of the form $Z/(Z + 2R_0)$ where Z is the passive impedance referred to above. It can thus also be written as

$$S = (Z' - R_0)/(Z' + R_0) \quad (117a)$$

$$Z' = Z + R_0. \quad (117b)$$

Since this is the reflectance of the passive impedance Z' with respect to R_0 , (117a) amounts to realizing Z' as reflectance with respect to the resistance R_0 , i.e., referring to Fig. 66(a), as $S = B/A$. Specifically, if Z is given in ladder

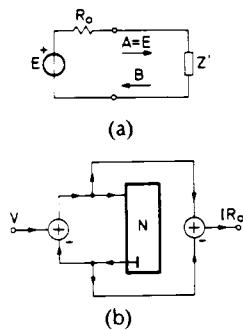


Fig. 66. (a) Concerning the realization of an equalizer transfer function as reflectance B/A of an impedance Z' with respect to R_0 . (b) Direct realization of an admittance.

configuration then Z' is also in ladder configuration and thus easily realizable.

It is true that for conventional applications, Z is prescribed in terms of elements with p as complex frequency, while for WDFs the complex frequency to be considered is ψ . However, it is usually not difficult to readjust the element values in such a way that the required loss curve is approximated with sufficient accuracy. The advantages thus to be gained are particularly attractive if the circuit is to be made adjustable, and this for the same reasons as those given in the first paragraph of Section X-B. Altogether, the procedure described here should frequently be much more advantageous than to determine first an acceptable transfer function and then to synthesize this by some general method available in digital filtering.

Consider also the *direct realization* of an *immittance* as a transfer function H (thus not indirectly as the correspond-

ing reflectance). More specifically, let H be given as $H = YR_0$ where Y is an admittance and R_0 a positive constant, the relation to be satisfied being thus $IR_0 = YR_0V$. Using (6), i.e.,

$$2V = A + B \quad 2RI = A - B$$

one obtains quite easily the structure of Fig. 66(b) where N is the usual WDF realization of $Z = 1/Y$ (i.e., the realization in terms of the reflectance $(Z - R_0)/(Z + R_0)$). Clearly, in order to avoid delay-free loops, N must be such that there is no delay-free path leading from its input to its output terminal (indicated in Fig. 66(b) by the same stroke as for constrained adaptors).

E. Wave Digital Filters for Speech Analysis and Synthesis

WDFs offer some specific properties that are of interest for speech analysis and synthesis. Some of these properties may be considered to be in a sense accidental, like those that determine the attractiveness of WDFs for subband coding (cf. Section X-A) or for realizing adaptive filters (cf. Section X-B). Others, however, follow immediately from physical analogies existing for the reference filter.

Thus it is sometimes desired to model as accurately as possible the vocal tract. Since the vocal tract can be considered in its main part as composed of a succession of two-ports whose electrical equivalents are transmission lines it is obvious that structures of the form of Fig. 36 are very suitable. Such a model can in fact be refined by providing stubs for the nasal tract, etc., which can again be simulated in a natural way by the WDF principle. How this can be done follows immediately from the general principles explained in Section VI-D.

Several papers on investigations taking advantage of these possibilities have been published [64], [374]–[379].

F. Application to Numerical Integration

The concepts of positivity and passivity have been shown to play an important role in numerical integration of ordinary differential equations [380], [381]. Advantage can be taken from this to improve the numerical accuracy in such integration procedures by basing these on the use of WDF concepts [382], [383].

XI. MULTIDIMENSIONAL WAVE DIGITAL FILTERS

A. General Principles

The principle of wave digital filtering can easily be extended to any number, say k , of dimensions [45], [384]–[389]. We are then dealing with k actual complex frequencies p_i , thus with k equivalent complex frequencies ψ_i

$$\psi_i = \tanh(p_i T/2), \quad i = 1 \text{ to } k$$

and thus also with k corresponding real frequencies ϕ_i

$$\phi_i = \tan(\omega_i T/2), \quad i = 1 \text{ to } k$$

T_i being the sampling interval (unit shift) in the i th variable t_i . The reference filter from which the WDF is to be derived is now a multidimensional (MD) Kirchhoff circuit comprising in particular reactive elements such as inductances, capacitances, unit elements, and QUARLs in the various dimensions, and furthermore constant elements of the same

type as in the one-dimensional (1D) case. For the reactive elements the definitions and relations of Tables 1 and 2 apply with ψ , T , and Δ replaced by ψ_i , T_i , and Δ_i , respectively, $i = 1$ to k .

The interconnections in an MD Kirchhoff circuit are governed by the same laws as in the 1D case. Hence, the simulation of these laws in the digital domain is precisely as for 1D circuits, i.e., all definitions and considerations concerning adaptors and their interconnections carry over unchanged, and the derivation of an MD WDF from its reference filter follows the same principles as those already established. The resulting WDFs are always *causal*. As an example, consider the two-dimensional (2D) reference filter of Fig. 67(b), where for the sake of clarity we have indicated

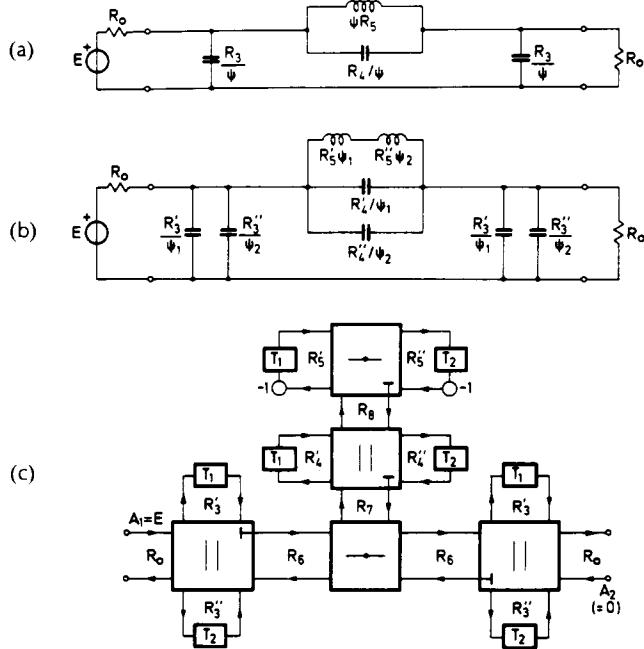


Fig. 67. (a) A 1D low-pass filter of degree 3. (b) A 2D filter that can be derived from (a) by ψ -domain rotation. (c) WDF derived from (b).

for each element not only its resistive parameter but its full impedance. Fig. 67(b) yields immediately the WDF of Fig. 67(c), where (letters "C" refer to the reciprocals of the corresponding letters "R")

$$C_6 = C_0 + C_3 + C_3' \quad R_8 = R'_5 + R''_5 \quad C_7 = C_8 + C_4 + C'_4.$$

A circuit such as that of Fig. 67(c) is realizable, at least for off-line processing. It can indeed be shown that in the latter case, realizability is ensured for a signal-flow diagram with only integer shifts (i.e., with all shifts equal to integer multiples of unit shifts), if there are no shift-free directed loops. For real-time processing, the realizability conditions are, of course, as given by Theorem 1 (Section II-A). It can be shown that the latter conditions can always be fulfilled by starting from a causal signal-flow diagram and applying a suitable rotation of the data.

If the reference filter is passive the resulting MD WDF is not only automatically stable under linear conditions, but all small- and large-scale parasitic oscillations can fully be suppressed by exactly the same simple means as in the 1D

case [390]. Note in this respect that it is not sufficient in the case of an MD digital filter to speak of limit cycles because in the case of more than one dimension, parasitic oscillations do not have to follow a periodically repetitive pattern (MD digital filters are not strictly finite-state machines). Forced-response stability can also be guaranteed in exactly the same way as for 1D WDFs [306]. By properly choosing the reference filter, coefficient wordlength requirements and dynamic range of the same order as for 1D WDFs are obtainable. All this holds independently of the number of dimensions or the degree of the filter. Even the property of stability under looped conditions fully carries over, but this is so far only of academic interest.

To illustrate the effectiveness of the suppression of parasitic oscillations, a WDF as shown in Fig. 67(c) has been tested with a strongly saturating initial signal (located along one of the axes) applied to it [391], [392]. The result is shown in Fig. 68 where small-signal values are strongly

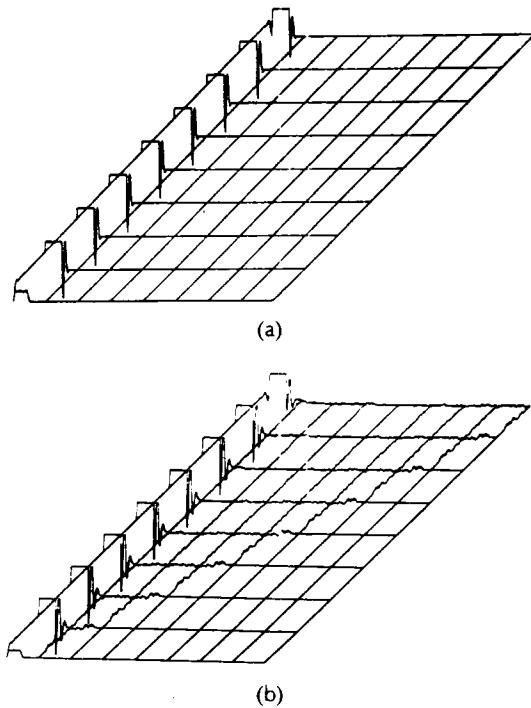


Fig. 68. Response of a filter according to Fig. 67(c) to a signal that is initially strongly saturating, small-signal values being strongly enlarged in the graphical representation: (a) if the proper means for suppressing parasitic oscillations are applied, (b) if these means are not applied.

enlarged so that even 1 LSB of oscillation would be visible. If the proper means for suppressing parasitic oscillations have been applied the filter comes completely to rest (Fig. 68(a)), but if they have not been applied some small parasitic oscillations persist (Fig. 68(b)).

The advantages to be gained from using MD WDFs were not that important as long as in MD filtering only a few applications were considered and that for these, big computers with their large (floating point) number ranges were used for implementing the filter algorithm. This is becoming different now that VLSI progress is bringing real-time MD filtering within practical reach. Obviously, it will be paramount to keep the required hardware to a minimum,

i.e., to adopt design approaches as efficient as possible. In this case, extreme care must be taken to avoid, as can be done with WDFs, unacceptable disturbances resulting from imperfections associated with digital filtering.

One major problem however exists for MD WDFs, i.e., the design of suitable reference filters. As a result there has been lately a considerable revival in the interest in MD reactance networks [393]–[400]. However, solutions for two major 2D problems are available, as will be discussed hereafter. Further solutions can be obtained (as for any MD digital filter) by appropriate sampling and modulation, interpolation, and decimation procedures [401]–[403].

B. Two-Dimensional Wave Digital Filters with Nearly Circularly Symmetric Response

As is well known, the simplest way to obtain a 2D low-pass filter with a loss response that has approximately circular symmetry is to start from a stable 1D transfer function, to apply to this a transformation (ψ -domain rotation)

$$\psi = c_1\psi_1 + c_2\psi_2 \quad (118)$$

where c_1 and c_2 are nonnegative constants, to repeat this a sufficient number of times with appropriately chosen distinct c_1 and c_2 , and to cascade the resulting partial filters. This process is immediately applicable to WDFs since (118) transforms an inductance of impedance $R\psi$ into two inductances in series of impedances $Rc_1\psi_1$ and $Rc_2\psi_2$, respectively, and a capacitance of impedance R/ψ into two capacitances in parallel of impedances $R/c_1\psi_1$ and $R/c_2\psi_2$, respectively [391], [392], [404]. As is true also for other 2D digital filters, rotations with, say, $c_2 < 0$ can, e.g., be achieved implicitly by 90° rotation of the data, and phase compensation is possible by processing the data in each partial filter once in the forward and once in the backward direction.

As an example, the 1D filter of Fig. 67(a) is transformed this way into the 2D filter of Fig. 67(b), with

$$\begin{aligned} R_3/R'_3 &= R_4/R'_4 = R'_5/R_5 = c_1 \\ R_3/R''_3 &= R_4/R''_4 = R''_5/R_5 = c_2 \end{aligned} \quad (119)$$

and the corresponding 2D WDF ladder structure (Fig. 67(c)) has already been discussed (Section XI-A). However, since the filter of Fig. 67(a) is symmetrical it is more efficient to use in this case the equivalent lattice configuration of Fig. 22 where Z' and Z'' are as given in Fig. 69(a). The corre-

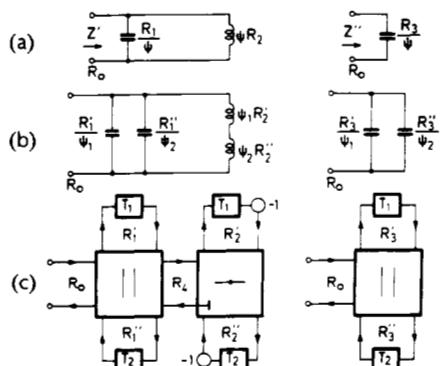


Fig. 69. (a) Lattice impedances Z' and Z'' corresponding to Fig. 67(a) (cf. Fig. 22). (b) 2D reactances obtain by applying (118) to (a). (c) WDF realizations of (b).

sponding impedances obtained by applying (118) and the resulting 2D WDF lattice branches are shown in Fig. 69(b) and (c), respectively, the expressions replacing (119) being easy to derive.

The simplest application of this example is to use two rotations with $c_1 = c_2 = 1$ plus phase compensation, altogether thus four cascaded filters. The corresponding transfer function is shown in Fig. 70 [391], [392]. Note that

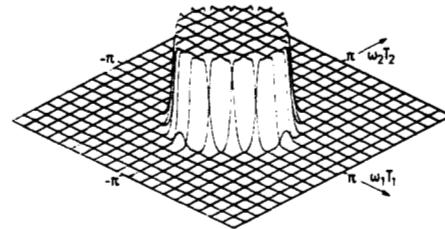


Fig. 70. Transfer function relief of a 2D WDF based on Figs. 67 or 69.

due to the simplicity of the choice for c_1 and c_2 there are two equal multipliers in each adaptor. Hence, simplifications are possible as explained with respect to Table 9. On the other hand, general investigations of the transformations involved facilitate the design [392], [404].

The method described so far for obtaining transfer properties with nearly circular symmetry can be further perfected by using triequilateral sampling, i.e., sampling according to a raster of equilateral triangles (also called hexagonal or quincuncial sampling) [405]. It would be even better, however, to have available single reference filters offering the desired frequency response. Although no analytic solution for this has been found, procedures by numerical optimization appear possible. Phase equalization is then still feasible either in the way stated before or, e.g., by an added MD all-pass WDF.

C. Wave Digital Fan Filters

In the original formulation [406], $\pm 45^\circ$ fan filters have been considered, but quadrant fan filters can be used just as well after rotating the data by 45° [407] (such a rotation being anyhow more advantageous in the case of real-time processing [45], [388]). Ideally, a quadrant fan filter has pass and stop regions either as shown in Fig. 71(a) ((ω_1, ω_2)-plane)

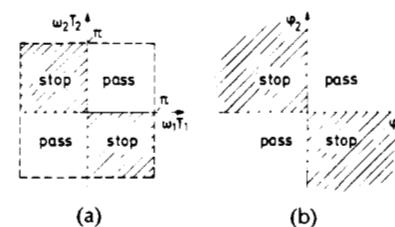


Fig. 71. Ideal pass and stop regions of a quadrant fan filter, (a) in the (ω_1, ω_2) -plane, (b) in the (ϕ_1, ϕ_2) -plane.

and Fig. 71(b) ((ϕ_1, ϕ_2)-plane) or the other way around. An attractive solution has been found that is based on a lattice structure (Fig. 22) whose branches are 2D LC impedances [394], [403], [407], [408].

The approach is based on the classical image parameter method, keeping the simplicity of this method without

having the disadvantages known from 1D filter theory. Thus due to the 2D nature of the problem, the maximum permitted loss in the pass region is reached at what appears to be a maximum number of times, and the same is true for the minimum permitted loss in the stop region. It may be conjectured that the solution is a global optimum for the types of boundaries resulting for the pass and stop regions. In one pair of quadrants of the (ϕ_1, ϕ_2) -plane (first and third or second and fourth) these boundaries are arbitrary symmetrically located straight lines passing through the origin, and in the other pair they are arbitrary hyperbolas whose asymptotes coincide with the axes (Fig. 72 or a corresponding figure obtained by interchanging the straight lines and hyperbolas).

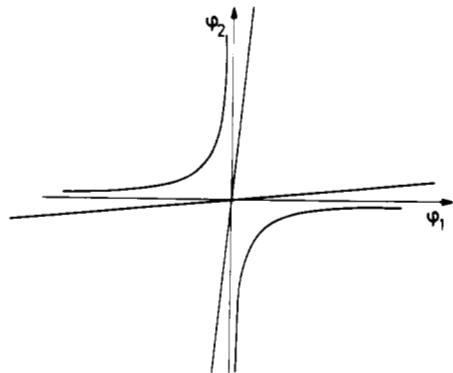


Fig. 72. One of the two possible choices for the boundaries of the actual pass and stop regions.

For arbitrarily tight specifications in the actual pass and stop regions thus selected, the method leads to the desired solution in a simple, straightforward, and essentially analytic manner. In the transition region located between the lines mentioned before the behavior is not controlled in the design process. The lattice impedances obtained can easily be synthesized as LC structures in such a way that a corresponding WDF structure follows by applying known principles. Of the two outputs available according to Fig. 23(a) (where we may set $A_2 = 0$), one corresponds to the situation depicted in Fig. 71, the other to that with the pass and stop quadrants interchanged.

As an example, a quadrant fan filter of degree 15 in each of the variables ψ_1 and ψ_2 has been designed [403], [409]. The structure of one of the lattice impedances, say Z' , is shown in Fig. 73. The corresponding WDF structure can be selected in such a way that it requires 30 multipliers, but due to relations existing between the elements (made apparent by the use of double parameters R_1 to R_5 and k_1 to k_3 in Fig. 73) only six coefficient values are distinct. The following, remarkably simple coefficient values (in binary representation) have been found to be satisfactory:

$$\begin{aligned}\gamma_1 &= 0.001, & \gamma_4 &= 0.000\ 101\ 11 \\ \gamma_2 &= 0.001\ 01, & \gamma_5 &= 0.010\ 1 \\ \gamma_3 &= 0.01, & \gamma_6 &= 0.000\ 001\ 11.\end{aligned}$$

Of these coefficients, γ_1 and γ_2 are each used 10 times, and γ_3 to γ_6 , each twice. The realization of Z'' is closely related to that of Z' and implies the same coefficients γ_1 to γ_6 . Fig. 74(a) shows in black where $|S_{21}| \geq 0.95$, S_{21} being the transmittance, and in Fig. 74(b), where $|S_{21}| \leq 0.05$. A perspective representation of $|S_{21}|$ is given in Fig. 75.

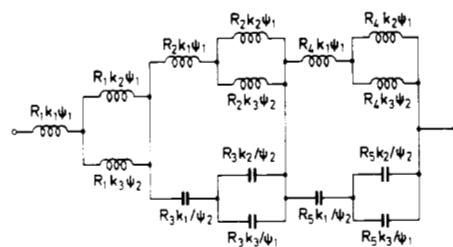


Fig. 73. Lattice impedance Z' of the quadrant fan filter designed as an example.

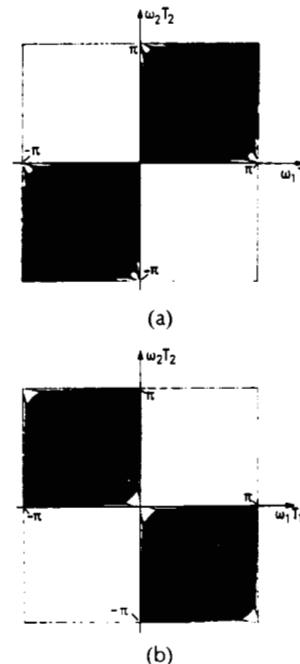


Fig. 74. (a) In dark is marked the area for which in the example we have $|S_{21}| \geq 0.95$. (b) In dark is marked the area for which in the example we have $|S_{21}| \leq 0.05$.

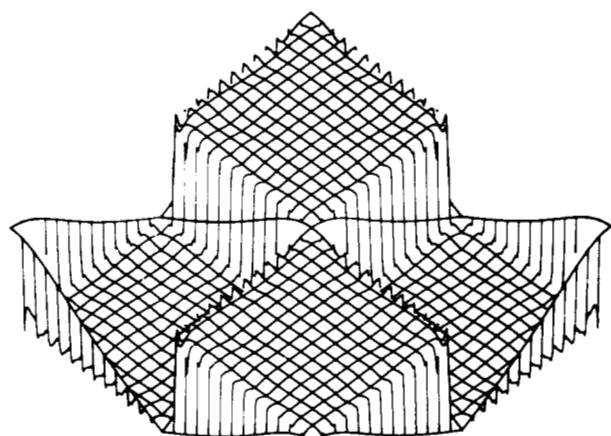


Fig. 75. Perspective representation of the transfer function magnitude for the fan filter example considered.

From a quadrant fan filter, designs with arbitrarily narrow sectors in the (ϕ_1, ϕ_2) -plane can be derived (Fig. 76), the filter degree in each variable being then double of what it was before. In order to ensure stability, the sectors with opening less than 90° are located in the second and fourth quadrant, but corresponding sectors in the first and third quadrant can be obtained, e.g., by the known principle of reversing the orientation of one of the axes. Two choices of

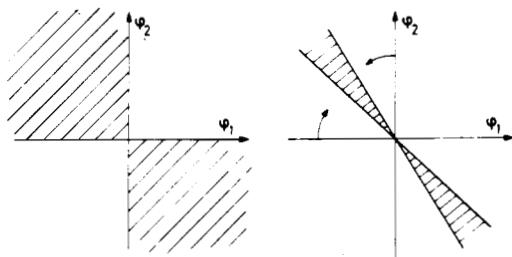


Fig. 76. Illustration of how filters with sector openings smaller than 90° can be generated from a quadrant fan filter.

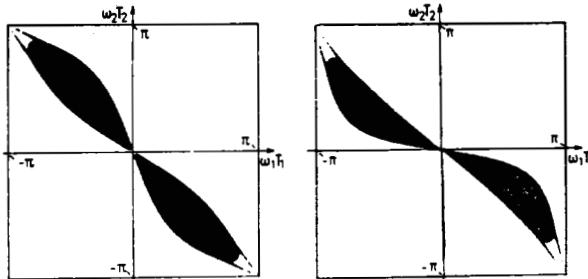


Fig. 77. Two examples of narrow sectors obtained in the way illustrated by Fig. 76.

narrow sectors are shown in Fig. 77. If the limits of the sectors must be straight lines rather than curves as those of Fig. 77 one can achieve this to any degree of perfection, e.g., by operating the filter at higher rates, applying zero stuffing to the input signal, and providing a further low-pass filtering at the input or output. The filter has been tested successfully with actual geophysical data [403].

A quite different approach of realizing quadrant fan filters consists in cascading two 1D complex low-pass filters with cutoff frequencies at $\omega_1 = 0$ and $\omega_2 = 0$, respectively [410], or, equivalently, of applying suitable modulation to the signal before processing it in corresponding real filters [402], [403]. The filters required in this case can again be realized by means of WDFs [402], [411], but the approach appears to be less efficient than the one discussed above, especially if sectors narrower than 90° are considered.

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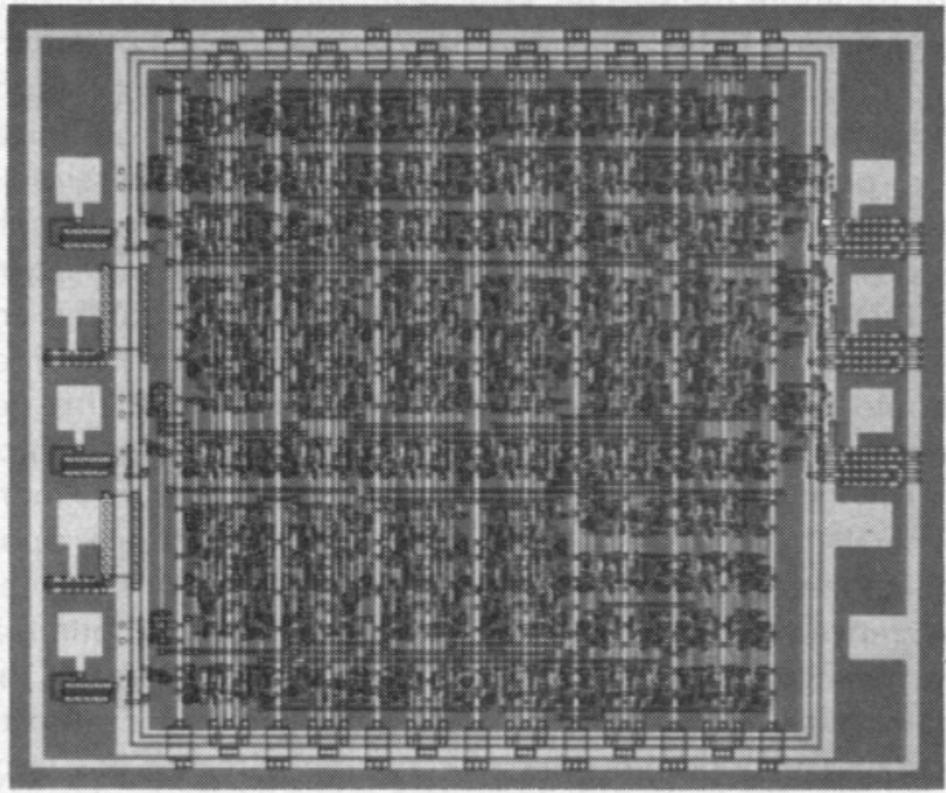


Fig. 33. Photomicrograph of an operational NMOS integrated circuit implementing a filter according to Figs. 23(b) and 32(a), with coefficients given by (99a). (Reproduced with permission of the authors [128], [132].)

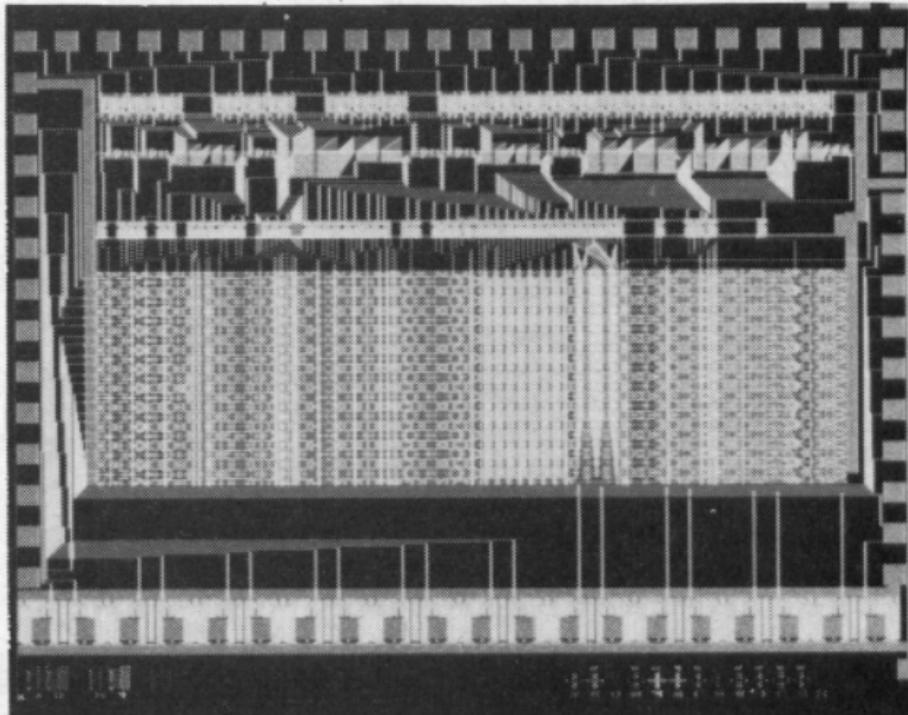


Fig. 52. Photomicrograph of the execution unit used on the adder-based digital signal processor PROFI, which is particularly suitable for implementing WDFs (reproduced with permission of Siemens, Munich).

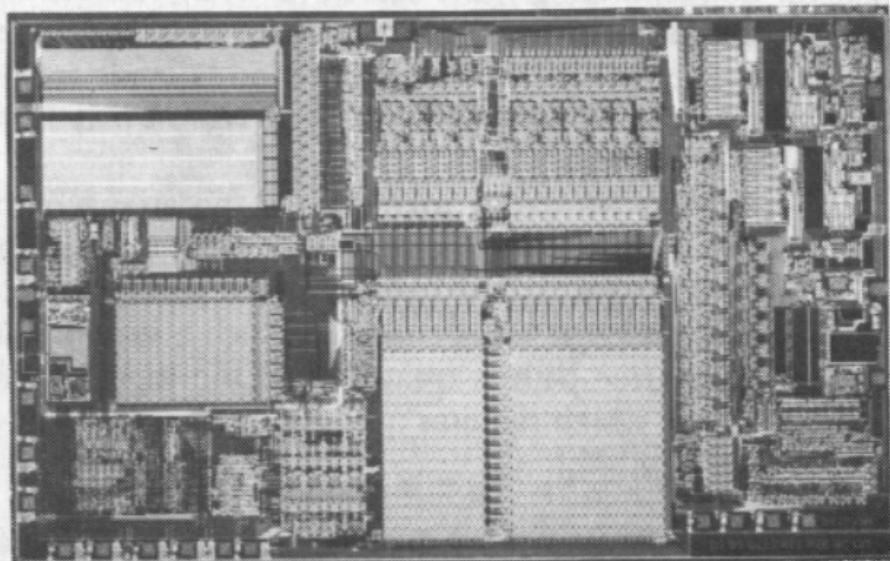


Fig. 53. Photomicrograph of the PCM codec chip SICOFI that comprises a WDF (reproduced with permission of Siemens, Munich).