# HW3 – PROBLEM 2 SOLUTION

# Cycle 1

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | | | |
| DIVD | F2, F0, F6 | 2 | | | | |
| LD | F6, 8(R1) | 3 | | | | |
| DIVD | F6, F6, F2 | 4 | | | | |
| SD | F6, 16(R1) | 5 | | | | |
| DADDI | R1, R1, #-32 | 6 | | | | |
| BNEQZ | R1, LOOP | 7 | | | | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | | | | |
| 9 | | | | |
| 10 | | | | |
| 11 | | | | |
| 12 | | | | |
| 13 | | | | |
| 14 | | | | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | #1 | | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| | Mult3 | | | | | | |
| | Mult4 | | | | | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| 2 | Ld1 | Yes | 0+R1 | |
| | Ld2 | | | |
| | Sd1 | | | |
| | Sd2 | | | |

# Cycle 2

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | Head 1 | 1 | 2- | | |
| DIVD | F2, F0, F6 | Tail 2 | 2 | | | |
| LD | F6, 8(R1) | 3 | | | | |
| DIVD | F6, F6, F2 | 4 | | | | |
| SD | F6, 16(R1) | 5 | | | | |
| DADDI | R1, R1, #-32 | 6 | | | | |
| BNEQZ | R1, LOOP | 7 | | | | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | | | | |
| 9 | | | | |
| 10 | | | | |
| 11 | | | | |
| 12 | | | | |
| 13 | | | | |
| 14 | | | | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | #1 | #2 | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | Yes | DIVD | | F6 | #1 | |
| | Mult2 | | | | | | |
| | Mult3 | | | | | | |
| | Mult4 | | | | | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| 1 | Ld1 | Yes | 0+R1 | |
| | Ld2 | | | |
| | Sd1 | | | |
| | Sd2 | | | |

# Cycle 3

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | Head 1 | 1 | 2-3 | | |
| DIVD | F2, F0, F6 | 2 | 2 | | | |
| LD | F6, 8(R1) | Tail 3 | 3 | | | |
| DIVD | F6, F6, F2 | 4 | | | | |
| SD | F6, 16(R1) | 5 | | | | |
| DADDI | R1, R1, #-32 | 6 | | | | |
| BNEQZ | R1, LOOP | 7 | | | | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | | | | |
| 9 | | | | |
| 10 | | | | |
| 11 | | | | |
| 12 | | | | |
| 13 | | | | |
| 14 | | | | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | #1 | #2 | #3 | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | Yes | DIVD | | F6 | #1 | |
| | Mult2 | | | | | | |
| | Mult3 | | | | | | |
| | Mult4 | | | | | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| 0 | Ld1 | Yes | 0+R1 | |
| 2 | Ld2 | Yes | 8+R1 | |
| | Sd1 | | | |
| | Sd2 | | | |

# Cycle 4

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | Head 1 | 1 | 2-3 | 4 | |
| DIVD | F2, F0, F6 | 2 | 2 | | | |
| LD | F6, 8(R1) | 3 | 3 | 4- | | |
| DIVD | F6, F6, F2 | Tail 4 | 4 | | | |
| SD | F6, 16(R1) | 5 | | | | |
| DADDI | R1, R1, #-32 | 6 | | | | |
| BNEQZ | R1, LOOP | 7 | | | | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | | | | |
| 9 | | | | |
| 10 | | | | |
| 11 | | | | |
| 12 | | | | |
| 13 | | | | |
| 14 | | | | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | #1 | #2 | #4 | |

| CDB | ROB # |
|---|---|
| | #1 |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| 15 | Mult1 | Yes | DIVD | M(A1) | F6 | | |
| | Mult2 | Yes | DIVD | | | #3 | #2 |
| | Mult3 | | | | | | |
| | Mult4 | | | | | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| 1 | Ld2 | Yes | 8+R1 | |
| | Sd1 | | | |
| | Sd2 | | | |

# Cycle 5

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | Head 2 | 2 | 5- | | |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | | |
| DIVD | F6, F6, F2 | 4 | 4 | | | |
| SD | F6, 16(R1) | Tail 5 | 5 | | | |
| DADDI | R1, R1, #-32 | 6 | | | | |
| BNEQZ | R1, LOOP | 7 | | | | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | | | | |
| 9 | | | | |
| 10 | | | | |
| 11 | | | | |
| 12 | | | | |
| 13 | | | | |
| 14 | | | | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #2 | #4 | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| 14 | Mult1 | Yes | DIVD | M(A1) | F6 | | |
| | Mult2 | Yes | DIVD | | | #3 | #2 |
| | Mult3 | | | | | | |
| | Mult4 | | | | | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| 0 | Ld2 | Yes | 8+R1 | |
| | Sd1 | Yes | 16+R1 | #4 |
| | Sd2 | | | |

# Cycle 6

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | Head 2 | 2 | 5- | | |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | |
| DIVD | F6, F6, F2 | 4 | 4 | | | |
| SD | F6, 16(R1) | 5 | 5 | | | |
| DADDI | R1, R1, #-32 | Tail 6 | 6 | | | |
| BNEQZ | R1, LOOP | 7 | | | | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | | | | |
| 9 | | | | |
| 10 | | | | |
| 11 | | | | |
| 12 | | | | |
| 13 | | | | |
| 14 | | | | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #2 | #4 | #6 |

| CDB | ROB # |
|---|---|
| | #3 |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| 1 | Add1 | Yes | DADDI | R1 | -32 | | |
| | Add2 | | | | | | |
| 13 | Mult1 | Yes | DIVD | M(A1) | F6 | | |
| | Mult2 | Yes | DIVD | M(A2) | | | #2 |
| | Mult3 | | | | | | |
| | Mult4 | | | | | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | Yes | 16+R1 | #4 |
| | Sd2 | | | |

# Cycle 7

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | Head 2 | 2 | 5- | | |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | |
| DIVD | F6, F6, F2 | 4 | 4 | | | |
| SD | F6, 16(R1) | 5 | 5 | | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | | |
| BNEQZ | R1, LOOP | Tail 7 | 7 | | | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | | | | |
| 9 | | | | |
| 10 | | | | |
| 11 | | | | |
| 12 | | | | |
| 13 | | | | |
| 14 | | | | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #2 | #4 | #7 |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| 0 | Add1 | Yes | DADDI | R1 | -32 | | |
| | Add2 | Yes | BNEQZ | | 0 | #6 | |
| 12 | Mult1 | Yes | DIVD | M(A1) | F6 | | |
| | Mult2 | Yes | DIVD | M(A2) | | | #2 |
| | Mult3 | | | | | | |
| | Mult4 | | | | | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | Yes | 16+R1 | #4 |
| | Sd2 | | | |

# Cycle 8

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | Head 2 | 2 | 5- | | |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | |
| DIVD | F6, F6, F2 | 4 | 4 | | | |
| SD | F6, 16(R1) | 5 | 5 | | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | Tail 7 | 7 | | | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | | | | |
| 9 | | | | |
| 10 | | | | |
| 11 | | | | |
| 12 | | | | |
| 13 | | | | |
| 14 | | | | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #2 | #4 | #7 |

| CDB | ROB # |
|---|---|
| | #6 |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| 1 | Add2 | Yes | BNEQZ | R1 | 0 | | |
| 11 | Mult1 | Yes | DIVD | M(A1) | F6 | | |
| | Mult2 | Yes | DIVD | M(A2) | | | #2 |
| | Mult3 | | | | | | |
| | Mult4 | | | | | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | Yes | 16+R1 | #4 |
| | Sd2 | | | |

# Cycle 9

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | Head 2 | 2 | 5- | | |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | |
| DIVD | F6, F6, F2 | 4 | 4 | | | |
| SD | F6, 16(R1) | 5 | 5 | | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | Tail 7 | 7 | 9 | | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | | | | |
| 9 | | | | |
| 10 | | | | |
| 11 | | | | |
| 12 | | | | |
| 13 | | | | |
| 14 | | | | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #2 | #4 | #7 |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| 0 | Add2 | Yes | BNEQZ | R1 | 0 | | |
| 10 | Mult1 | Yes | DIVD | M(A1) | F6 | | |
| | Mult2 | Yes | DIVD | M(A2) | | | #2 |
| | Mult3 | | | | | | |
| | Mult4 | | | | | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | Yes | 16+R1 | #4 |
| | Sd2 | | | |

# Cycle 10

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | Head 2 | 2 | 5- | | |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | |
| DIVD | F6, F6, F2 | 4 | 4 | | | |
| SD | F6, 16(R1) | 5 | 5 | | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| Tail 8 | 10 | | | |
| 9 | | | | |
| 10 | | | | |
| 11 | | | | |
| 12 | | | | |
| 13 | | | | |
| 14 | | | | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | #8 | #2 | #4 | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| 9 | Mult1 | Yes | DIVD | M(A1) | F6 | | |
| | Mult2 | Yes | DIVD | M(A2) | | | #2 |
| | Mult3 | | | | | | |
| | Mult4 | | | | | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| 2 | Ld1 | Yes | 0+R1 | |
| | Ld2 | | | |
| | Sd1 | Yes | 16+R1 | #4 |
| | Sd2 | | | |

# Cycle 11

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | Head 2 | 2 | 5- | | |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | |
| DIVD | F6, F6, F2 | 4 | 4 | | | |
| SD | F6, 16(R1) | 5 | 5 | | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11- | | |
| Tail 9 | 11 | | | |
| 10 | | | | |
| 11 | | | | |
| 12 | | | | |
| 13 | | | | |
| 14 | | | | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | #8 | #9 | #4 | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| 8 | Mult1 | Yes | DIVD | M(A1) | F6 | | |
| | Mult2 | Yes | DIVD | M(A2) | | | #2 |
| | Mult3 | Yes | DIVD | | | #8 | #4 |
| | Mult4 | | | | | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| 1 | Ld1 | Yes | 0+R1 | |
| | Ld2 | | | |
| | Sd1 | Yes | 16+R1 | #4 |
| | Sd2 | | | |

# Cycle 12

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | Head 2 | 2 | 5- | | |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | |
| DIVD | F6, F6, F2 | 4 | 4 | | | |
| SD | F6, 16(R1) | 5 | 5 | | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | | |
| 9 | 11 | | | |
| Tail 10 | 12 | | | |
| 11 | | | | |
| 12 | | | | |
| 13 | | | | |
| 14 | | | | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | #8 | #9 | #10 | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| 7 | Mult1 | Yes | DIVD | M(A1) | F6 | | |
| | Mult2 | Yes | DIVD | M(A2) | | | #2 |
| | Mult3 | Yes | DIVD | | | #8 | #4 |
| | Mult4 | | | | | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| 0 | Ld1 | Yes | 0+R1 | |
| 2 | Ld2 | Yes | 8+R1 | #9 |
| | Sd1 | Yes | 16+R1 | #4 |
| | Sd2 | | | |

# Cycle 13

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | Head 2 | 2 | 5- | | |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | |
| DIVD | F6, F6, F2 | 4 | 4 | | | |
| SD | F6, 16(R1) | 5 | 5 | | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | |
| 9 | 11 | | | |
| 10 | 12 | 13- | | |
| Tail 11 | 13 | | | |
| 12 | | | | |
| 13 | | | | |
| 14 | | | | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | #8 | #9 | #10 | |

| CDB | ROB # |
|---|---|
| | #8 |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| 6 | Mult1 | Yes | DIVD | M(A1) | F6 | | |
| | Mult2 | Yes | DIVD | M(A2) | | | #2 |
| | Mult3 | Yes | DIVD | M(A3) | | | #4 |
| | Mult4 | Yes | DIVD | | | #10 | #9 |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| 1 | Ld2 | Yes | 8+R1 | #9 |
| | Sd1 | Yes | 16+R1 | #4 |
| | Sd2 | | | |

# Cycle 14

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | Head 2 | 2 | 5- | | |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | |
| DIVD | F6, F6, F2 | 4 | 4 | | | |
| SD | F6, 16(R1) | 5 | 5 | | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | |
| 9 | 11 | | | |
| 10 | 12 | 13-14 | | |
| 11 | 13 | | | |
| Tail 12 | 14 | | | |
| 13 | | | | |
| 14 | | | | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | #10 | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| 5 | Mult1 | Yes | DIVD | M(A1) | F6 | | |
| | Mult2 | Yes | DIVD | M(A2) | | | #2 |
| | Mult3 | Yes | DIVD | M(A3) | | | #4 |
| | Mult4 | Yes | DIVD | | | #10 | #9 |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| 0 | Ld2 | Yes | 8+R1 | #9 |
| | Sd1 | Yes | 16+R1 | #4 |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 15

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | Head 2 | 2 | 5- | | |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | |
| DIVD | F6, F6, F2 | 4 | 4 | | | |
| SD | F6, 16(R1) | 5 | 5 | | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | |
| 9 | 11 | | | |
| 10 | 12 | 13-14 | 15 | |
| 11 | 13 | | | |
| 12 | 14 | | | |
| Tail 13 | 15 | | | |
| 14 | | | | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | #10 | #13 |

| CDB | ROB # |
|---|---|
| | #10 |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| 1 | Add1 | Yes | DADDI | R1 | -32 | | |
| | Add2 | | | | | | |
| 4 | Mult1 | Yes | DIVD | M(A1) | F6 | | |
| | Mult2 | Yes | DIVD | M(A2) | | | #2 |
| | Mult3 | Yes | DIVD | M(A3) | | | #4 |
| | Mult4 | Yes | DIVD | M(A4) | | | #9 |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | Yes | 16+R1 | #4 |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 16

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | Head 2 | 2 | 5- | | |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | |
| DIVD | F6, F6, F2 | 4 | 4 | | | |
| SD | F6, 16(R1) | 5 | 5 | | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | |
| 9 | 11 | | | |
| 10 | 12 | 13-14 | 15 | |
| 11 | 13 | | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | | |
| Tail 14 | 16 | | | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | | #14 |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| 0 | Add1 | Yes | DADDI | R1 | -32 | | |
| | Add2 | Yes | BNEQZ | | 0 | R1 | |
| 3 | Mult1 | Yes | DIVD | M(A1) | F6 | | |
| | Mult2 | Yes | DIVD | M(A2) | | | #2 |
| | Mult3 | Yes | DIVD | M(A3) | | | #4 |
| | Mult4 | Yes | DIVD | M(A4) | | | #9 |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | Yes | 16+R1 | #4 |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 17

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | Head 2 | 2 | 5- | | |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | |
| DIVD | F6, F6, F2 | 4 | 4 | | | |
| SD | F6, 16(R1) | 5 | 5 | | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | |
| 9 | 11 | | | |
| 10 | 12 | 13-14 | 15 | |
| 11 | 13 | | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | | | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | | #14 |

| CDB | ROB # |
|---|---|
| | #13 |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| 2 | Add2 | Yes | BNEQZ | R1 | 0 | | |
| 2 | Mult1 | Yes | DIVD | M(A1) | F6 | | |
| | Mult2 | Yes | DIVD | M(A2) | | | #2 |
| | Mult3 | Yes | DIVD | M(A3) | | | #4 |
| | Mult4 | Yes | DIVD | M(A4) | | | #9 |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | Yes | 16+R1 | #4 |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 18

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | Head 2 | 2 | 5- | | |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | |
| DIVD | F6, F6, F2 | 4 | 4 | | | |
| SD | F6, 16(R1) | 5 | 5 | | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | |
| 9 | 11 | | | |
| 10 | 12 | 13-14 | 15 | |
| 11 | 13 | | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | | #14 |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| 1 | Add2 | Yes | BNEQZ | R1 | 0 | | |
| 1 | Mult1 | Yes | DIVD | M(A1) | F6 | | |
| | Mult2 | Yes | DIVD | M(A2) | | | #2 |
| | Mult3 | Yes | DIVD | M(A3) | | | #4 |
| | Mult4 | Yes | DIVD | M(A4) | | | #9 |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | Yes | 16+R1 | #4 |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 19

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | Head 2 | 2 | 5-19 | | |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | |
| DIVD | F6, F6, F2 | 4 | 4 | | | |
| SD | F6, 16(R1) | 5 | 5 | | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | |
| 9 | 11 | | | |
| 10 | 12 | 13-14 | 15 | |
| 11 | 13 | | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| 0 | Add2 | Yes | BNEQZ | R1 | 0 | | |
| 0 | Mult1 | Yes | DIVD | M(A1) | F6 | | |
| | Mult2 | Yes | DIVD | M(A2) | | | #2 |
| | Mult3 | Yes | DIVD | M(A3) | | | #4 |
| | Mult4 | Yes | DIVD | M(A4) | | | #9 |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | Yes | 16+R1 | #4 |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 20

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | Head 2 | 2 | 5-19 | 20 | |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | |
| DIVD | F6, F6, F2 | 4 | 4 | | | |
| SD | F6, 16(R1) | 5 | 5 | | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | |
| 9 | 11 | | | |
| 10 | 12 | 13-14 | 15 | |
| 11 | 13 | | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | | |

| CDB | ROB # |
|---|---|
| | #2 |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| 15 | Mult2 | Yes | DIVD | M(A2) | M(A5) | | |
| | Mult3 | Yes | DIVD | M(A3) | | | #4 |
| | Mult4 | Yes | DIVD | M(A4) | | | #9 |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | Yes | 16+R1 | #4 |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 21

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | Head 3 | 3 | 4-5 | 6 | |
| DIVD | F6, F6, F2 | 4 | 4 | 21- | | |
| SD | F6, 16(R1) | 5 | 5 | | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | |
| 9 | 11 | | | |
| 10 | 12 | 13-14 | 15 | |
| 11 | 13 | | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| 14 | Mult2 | Yes | DIVD | M(A2) | M(A5) | | |
| | Mult3 | Yes | DIVD | M(A3) | | | #4 |
| | Mult4 | Yes | DIVD | M(A4) | | | #9 |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | Yes | 16+R1 | #4 |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 22

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | Head 4 | 4 | 21- | | |
| SD | F6, 16(R1) | 5 | 5 | | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | |
| 9 | 11 | | | |
| 10 | 12 | 13-14 | 15 | |
| 11 | 13 | | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| 13 | Mult2 | Yes | DIVD | M(A2) | M(A5) | | |
| | Mult3 | Yes | DIVD | M(A3) | | | #4 |
| | Mult4 | Yes | DIVD | M(A4) | | | #9 |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | Yes | 16+R1 | #4 |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 35

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | Head 4 | 4 | 21-35 | | |
| SD | F6, 16(R1) | 5 | 5 | | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | |
| 9 | 11 | | | |
| 10 | 12 | 13-14 | 15 | |
| 11 | 13 | | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| 0 | Mult2 | Yes | DIVD | M(A2) | M(A5) | | |
| | Mult3 | Yes | DIVD | M(A3) | | | #4 |
| | Mult4 | Yes | DIVD | M(A4) | | | #9 |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | Yes | 16+R1 | #4 |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 36

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | Head 4 | 4 | 21-35 | 36 | |
| SD | F6, 16(R1) | 5 | 5 | | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | |
| 9 | 11 | | | |
| 10 | 12 | 13-14 | 15 | |
| 11 | 13 | | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | | |

| CDB | ROB # |
|---|---|
| | #4 |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| 15 | Mult3 | Yes | DIVD | M(A3) | M(A6) | | |
| | Mult4 | Yes | DIVD | M(A4) | | | #9 |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| 2 | Sd1 | Yes | 16+R1 | |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 37

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | 4 | 4 | 21-35 | 36 | 37 |
| SD | F6, 16(R1) | Head 5 | 5 | 37- | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | |
| 9 | 11 | 37- | | |
| 10 | 12 | 13-14 | 15 | |
| 11 | 13 | | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| 14 | Mult3 | Yes | DIVD | M(A3) | M(A6) | | |
| | Mult4 | Yes | DIVD | M(A4) | | | #9 |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| 1 | Sd1 | Yes | 16+R1 | |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 38

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | 4 | 4 | 21-35 | 36 | 37 |
| SD | F6, 16(R1) | Head 5 | 5 | 37-38 | | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | |
| 9 | 11 | 37- | | |
| 10 | 12 | 13-14 | 15 | |
| 11 | 13 | | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| 13 | Mult3 | Yes | DIVD | M(A3) | M(A6) | | |
| | Mult4 | Yes | DIVD | M(A4) | | | #9 |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| 0 | Sd1 | Yes | 16+R1 | |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 39

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | 4 | 4 | 21-35 | 36 | 37 |
| SD | F6, 16(R1) | Head 5 | 5 | 37-38 | 39 | |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | |
| 9 | 11 | 37- | | |
| 10 | 12 | 13-14 | 15 | |
| 11 | 13 | | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| 12 | Mult3 | Yes | DIVD | M(A3) | M(A6) | | |
| | Mult4 | Yes | DIVD | M(A4) | | | #9 |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | | | |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 40

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | 4 | 4 | 21-35 | 36 | 37 |
| SD | F6, 16(R1) | 5 | 5 | 37-38 | 39 | 40 |
| DADDI | R1, R1, #-32 | Head 6 | 6 | 7 | 8 | |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | |
| 9 | 11 | 37- | | |
| 10 | 12 | 13-14 | 15 | |
| 11 | 13 | | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| 11 | Mult3 | Yes | DIVD | M(A3) | M(A6) | | |
| | Mult4 | Yes | DIVD | M(A4) | | | #9 |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | | | |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 41

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | 4 | 4 | 21-35 | 36 | 37 |
| SD | F6, 16(R1) | 5 | 5 | 37-38 | 39 | 40 |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | 41 |
| BNEQZ | R1, LOOP | Head 7 | 7 | 9 | 10 | |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | |
| 9 | 11 | 37- | | |
| 10 | 12 | 13-14 | 15 | |
| 11 | 13 | | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| 10 | Mult3 | Yes | DIVD | M(A3) | M(A6) | | |
| | Mult4 | Yes | DIVD | M(A4) | | | #9 |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | | | |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 42

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | 4 | 4 | 21-35 | 36 | 37 |
| SD | F6, 16(R1) | 5 | 5 | 37-38 | 39 | 40 |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | 41 |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | 42 |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| Head 8 | 10 | 11-12 | 13 | |
| 9 | 11 | 37- | | |
| 10 | 12 | 13-14 | 15 | |
| 11 | 13 | | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| 9 | Mult3 | Yes | DIVD | M(A3) | M(A6) | | |
| | Mult4 | Yes | DIVD | M(A4) | | | #9 |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | | | |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 43

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | 4 | 4 | 21-35 | 36 | 37 |
| SD | F6, 16(R1) | 5 | 5 | 37-38 | 39 | 40 |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | 41 |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | 42 |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | 43 |
| Head 9 | 11 | 37- | | |
| 10 | 12 | 13-14 | 15 | |
| 11 | 13 | | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| 8 | Mult3 | Yes | DIVD | M(A3) | M(A6) | | |
| | Mult4 | Yes | DIVD | M(A4) | | | #9 |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | | | |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 51

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | 4 | 4 | 21-35 | 36 | 37 |
| SD | F6, 16(R1) | 5 | 5 | 37-38 | 39 | 40 |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | 41 |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | 42 |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | 43 |
| Head 9 | 11 | 37-51 | | |
| 10 | 12 | 13-14 | 15 | |
| 11 | 13 | | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| 0 | Mult3 | Yes | DIVD | M(A3) | M(A6) | | |
| | Mult4 | Yes | DIVD | M(A4) | M(A7) | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | | | |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 52

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | 4 | 4 | 21-35 | 36 | 37 |
| SD | F6, 16(R1) | 5 | 5 | 37-38 | 39 | 40 |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | 41 |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | 42 |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | 43 |
| Head 9 | 11 | 37-51 | 52 | |
| 10 | 12 | 13-14 | 15 | |
| 11 | 13 | | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | #9 | | |

| CDB | ROB # |
|---|---|
| | #9 |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| | Mult3 | | | | | | |
| 15 | Mult4 | Yes | DIVD | M(A4) | M(A7) | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | | | |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 53

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | 4 | 4 | 21-35 | 36 | 37 |
| SD | F6, 16(R1) | 5 | 5 | 37-38 | 39 | 40 |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | 41 |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | 42 |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | 43 |
| 9 | 11 | 37-51 | 52 | 53 |
| Head 10 | 12 | 13-14 | 15 | |
| 11 | 13 | 53- | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| | Mult3 | | | | | | |
| 14 | Mult4 | Yes | DIVD | M(A4) | M(A7) | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | | | |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 54

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | 4 | 4 | 21-35 | 36 | 37 |
| SD | F6, 16(R1) | 5 | 5 | 37-38 | 39 | 40 |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | 41 |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | 42 |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | 43 |
| 9 | 11 | 37-51 | 52 | 53 |
| 10 | 12 | 13-14 | 15 | 54 |
| Head 11 | 13 | 53- | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| | Mult3 | | | | | | |
| 13 | Mult4 | Yes | DIVD | M(A4) | M(A7) | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | | | |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 67

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | 4 | 4 | 21-35 | 36 | 37 |
| SD | F6, 16(R1) | 5 | 5 | 37-38 | 39 | 40 |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | 41 |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | 42 |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | 43 |
| 9 | 11 | 37-51 | 52 | 53 |
| 10 | 12 | 13-14 | 15 | 54 |
| Head 11 | 13 | 53-67 | | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| | Mult3 | | | | | | |
| 0 | Mult4 | Yes | DIVD | M(A4) | M(A7) | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | | | |
| | Sd2 | Yes | 16+R1 | #11 |

# Cycle 68

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | 4 | 4 | 21-35 | 36 | 37 |
| SD | F6, 16(R1) | 5 | 5 | 37-38 | 39 | 40 |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | 41 |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | 42 |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | 43 |
| 9 | 11 | 37-51 | 52 | 53 |
| 10 | 12 | 13-14 | 15 | 54 |
| Head 11 | 13 | 53-67 | 68 | |
| 12 | 14 | | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| | Mult3 | | | | | | |
| | Mult4 | | | | | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | | | |
| 2 | Sd2 | Yes | 16+R1 | |

# Cycle 69

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | 4 | 4 | 21-35 | 36 | 37 |
| SD | F6, 16(R1) | 5 | 5 | 37-38 | 39 | 40 |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | 41 |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | 42 |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | 43 |
| 9 | 11 | 37-51 | 52 | 53 |
| 10 | 12 | 13-14 | 15 | 54 |
| 11 | 13 | 53-67 | 68 | 69 |
| Head 12 | 14 | 69- | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| | Mult3 | | | | | | |
| | Mult4 | | | | | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | | | |
| 1 | Sd2 | Yes | 16+R1 | |

# Cycle 70

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | 4 | 4 | 21-35 | 36 | 37 |
| SD | F6, 16(R1) | 5 | 5 | 37-38 | 39 | 40 |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | 41 |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | 42 |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | 43 |
| 9 | 11 | 37-51 | 52 | 53 |
| 10 | 12 | 13-14 | 15 | 54 |
| 11 | 13 | 53-67 | 68 | 69 |
| Head 12 | 14 | 69-70 | | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| | Mult3 | | | | | | |
| | Mult4 | | | | | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | | | |
| 0 | Sd2 | Yes | 16+R1 | |

# Cycle 71

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | 4 | 4 | 21-35 | 36 | 37 |
| SD | F6, 16(R1) | 5 | 5 | 37-38 | 39 | 40 |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | 41 |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | 42 |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | 43 |
| 9 | 11 | 37-51 | 52 | 53 |
| 10 | 12 | 13-14 | 15 | 54 |
| 11 | 13 | 53-67 | 68 | 69 |
| Head 12 | 14 | 69-70 | 71 | |
| 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| | Mult3 | | | | | | |
| | Mult4 | | | | | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | | | |
| | Sd2 | | | |

# Cycle 72

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | 4 | 4 | 21-35 | 36 | 37 |
| SD | F6, 16(R1) | 5 | 5 | 37-38 | 39 | 40 |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | 41 |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | 42 |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | 43 |
| 9 | 11 | 37-51 | 52 | 53 |
| 10 | 12 | 13-14 | 15 | 54 |
| 11 | 13 | 53-67 | 68 | 69 |
| 12 | 14 | 69-70 | 71 | 72 |
| Head 13 | 15 | 16 | 17 | |
| Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| | Mult3 | | | | | | |
| | Mult4 | | | | | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | | | |
| | Sd2 | | | |

# Cycle 73

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | 4 | 4 | 21-35 | 36 | 37 |
| SD | F6, 16(R1) | 5 | 5 | 37-38 | 39 | 40 |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | 41 |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | 42 |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | 43 |
| 9 | 11 | 37-51 | 52 | 53 |
| 10 | 12 | 13-14 | 15 | 54 |
| 11 | 13 | 53-67 | 68 | 69 |
| 12 | 14 | 69-70 | 71 | 72 |
| 13 | 15 | 16 | 17 | 73 |
| Head/Tail 14 | 16 | 18 | 19 | |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| | Mult3 | | | | | | |
| | Mult4 | | | | | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | | | |
| | Sd2 | | | |

# Cycle 74

Reorder Buffer / Instruction Status Iter 1

| Instructions | | ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|---|---|
| LD | F0, 0(R1) | 1 | 1 | 2-3 | 4 | 5 |
| DIVD | F2, F0, F6 | 2 | 2 | 5-19 | 20 | 21 |
| LD | F6, 8(R1) | 3 | 3 | 4-5 | 6 | 22 |
| DIVD | F6, F6, F2 | 4 | 4 | 21-35 | 36 | 37 |
| SD | F6, 16(R1) | 5 | 5 | 37-38 | 39 | 40 |
| DADDI | R1, R1, #-32 | 6 | 6 | 7 | 8 | 41 |
| BNEQZ | R1, LOOP | 7 | 7 | 9 | 10 | 42 |

Reorder Buffer / Instruction Status Iter 2

| ROB Entry # | IS | EX | WB | CMT |
|---|---|---|---|---|
| 8 | 10 | 11-12 | 13 | 43 |
| 9 | 11 | 37-51 | 52 | 53 |
| 10 | 12 | 13-14 | 15 | 54 |
| 11 | 13 | 53-67 | 68 | 69 |
| 12 | 14 | 69-70 | 71 | 72 |
| 13 | 15 | 16 | 17 | 73 |
| 14 | 16 | 18 | 19 | 74 |

Register Result Status

| Reg | F0 | F2 | F6 | R1 |
|---|---|---|---|---|
| ROB # | | | | |

| CDB | ROB # |
|---|---|
| | |

Reservation Stations

| Time (until complete) | Name | Busy | Op | Vj | Vk | Qj | Qk |
|---|---|---|---|---|---|---|---|
| | Add1 | | | | | | |
| | Add2 | | | | | | |
| | Mult1 | | | | | | |
| | Mult2 | | | | | | |
| | Mult3 | | | | | | |
| | Mult4 | | | | | | |

LD/SD Buffers

| Time (until complete) | Name | Busy | Addr | Qj |
|---|---|---|---|---|
| | Ld1 | | | |
| | Ld2 | | | |
| | Sd1 | | | |
| | Sd2 | | | |

# Reservation Station Notes

Op: Operation to perform in the unit

Qj, Qk: Reservation stations producing source registers (value to be written)

- Note: No ready flags needed as in Scoreboard
- Qj,Qk=0 => ready
- Store buffers only have Qi for RS producing result

Vj, Vk: Value of Source operands

- Store buffers has V field, result to be stored

Busy: Indicates reservation station or FU are occupied

Register Result Status: Indicates which functional unit will write each register, if one exists. Blank when no pending instructions that will write that register.

# Four Steps of Speculative Tomasulo Algorithm

1. Issue—get instruction from FP Op Queue

   If reservation station and reorder buffer slot free, issue instr & send operands & reorder buffer no. for destination (this stage sometimes called "dispatch")

2. Execution—operate on operands (EX)

   When both operands ready then execute; if not ready, watch CDB for result; when both in reservation station, execute; checks RAW (sometimes called "issue")

3. Write result—finish execution (WB)

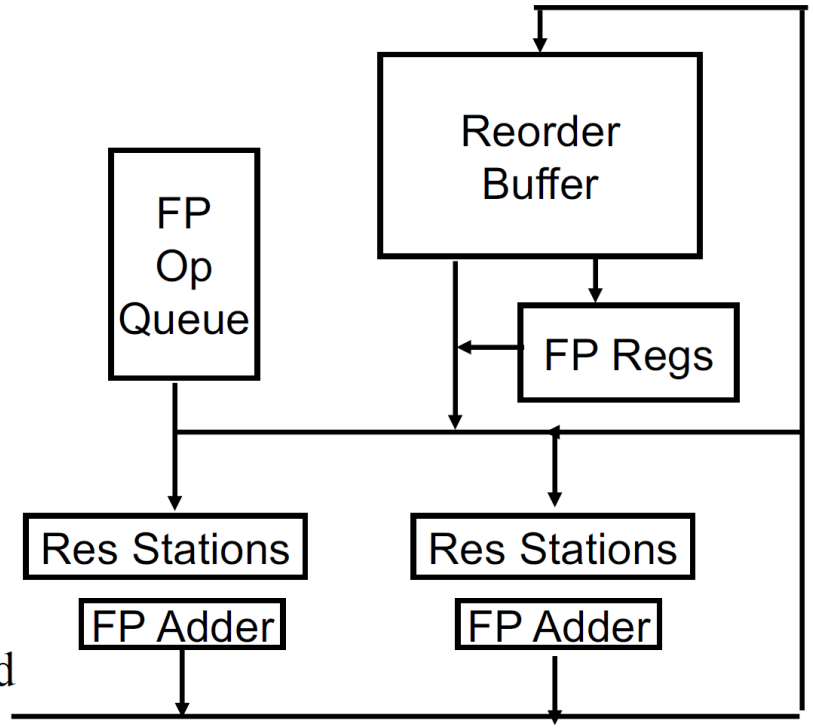
   Write on Common Data Bus to all awaiting FUs & reorder buffer; mark reservation station available. (tags are now ROB #s not RS #s)

4. Commit—update register with reorder result

   When instr. at head of reorder buffer & result present, update register with result (or store to memory) and remove instr from reorder buffer. Mispredicted branch flushes reorder buffer (sometimes called "graduation")

# Reorder Buffer: HW buffer for results of uncommitted instructions

- 3 fields: instr, destination, value
- Reorder buffer can be operand source => more registers like RS
- Use reorder buffer number instead of reservation station when execution completes
- Supplies operands between execution complete & commit
- Once operand commits, result is put into register
- Instructions commit
- As a result, its easy to undo speculated instructions on mispredicted branches or on exceptions



# Tips: How to Update each Slide

1. Renumber Cycle on Slide
2. To Issue an Instruction
    1. Add cycle number when issued
    2. Update Reservation Station
        1. Check if instruction inputs are ready (Vi, Vk) or not ready (Qi, Qk)
            1. If data is not ready, identify which Function Unit will produce using Register Result Status
    3. For non SD / BR instructions – must update Register Result Status
    4. Move Tail
3. To Update Instructions in Execution
    1. Change time to finish execution
    2. If time = 0, write in cycle on exe in Instruction Status table
4. To Update Instructions in Write Result
    1. For non SD / BR instructions – write FU to CDB
    2. Fill in cycle number for write back
    3. Only 1 instruction may write to CDB at a time (but SD / BR can also be in Write Result stage since not using CDB)
    4. Remove data from reservation station
    5. Update all Reservation Stations which depended on FU for data
5. To Commit an Instruction
    1. Instruction must have finished write back
    2. Move Head