



SERVIÇO PÚBLICO FEDERAL · MINISTÉRIO DA EDUCAÇÃO  
UNIVERSIDADE FEDERAL DE VIÇOSA · UFV  
CAMPUS FLORESTAL

## **Trabalho 1 - ISL**

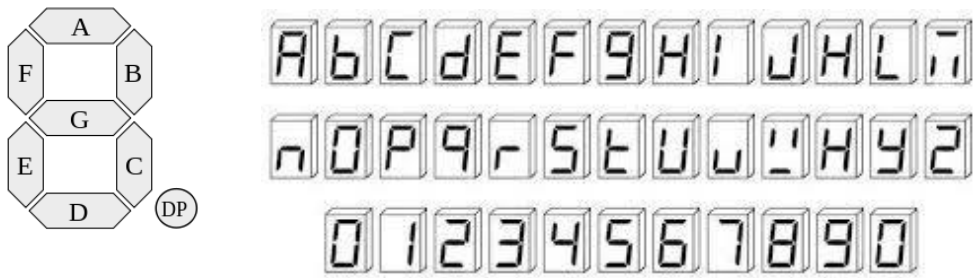
### **Implementação de Circuito Combinacional para Display de 7 Segmentos**

Matheus Toledo [05909]

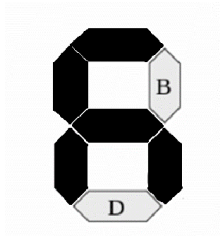
Vítor Afonso [05906]

Florestal - MG

2024



**Figura 1:** Display de sete segmentos e definição dos caracteres.



Caso esteja com o bit de paridade invalido (verificação for 0) o display irá ter essa saída: (1010111).

### 3.1 Tabela da Verdade

Para produzir a tabela da verdade, foi necessário identificar as letras e números codificados com base nos valores binários correspondentes:

Bits	00000	00001	00010	00011	00100	00101	00110	00111	01000	01001	01010	01011	01100	01101	01110	01111	10000	10001	10010	10011
9	S	A	4	M	G	V	O	P	K	1	J	9	X	F	7	W	L	3	C	T

NÚMERO	E1	E2	E3	E4	E5	P	Verificação	A	B	C	D	E	F	G	Representa
1	0	0	0	0	0	0	0	1	0	1	0	1	1	1	Erro
1	0	0	0	0	0	0	1	1	0	1	1	0	1	1	S
2	0	0	0	0	1	0	1	1	1	1	0	1	1	1	A
2	0	0	0	0	1	1	0	1	0	1	0	1	1	1	Erro
3	0	0	0	1	0	0	1	0	1	1	0	0	1	1	4
3	0	0	0	1	0	1	0	1	0	1	0	1	1	1	Erro
4	0	0	0	1	1	0	0	1	0	1	0	1	1	1	Erro
4	0	0	0	1	1	1	1	1	0	1	0	1	0	0	M
5	0	0	1	0	0	0	1	1	1	1	1	0	1	1	G
5	0	0	1	0	0	1	0	1	0	1	0	1	1	1	Erro
6	0	0	1	0	1	0	0	1	0	1	0	1	1	1	Erro
6	0	0	1	0	1	1	1	0	0	1	1	1	0	0	V
7	0	0	1	1	1	0	0	1	0	1	0	1	1	1	Erro
7	0	0	1	1	0	1	1	1	1	1	1	1	1	0	O
8	0	0	1	1	1	0	1	1	1	0	0	1	1	1	P
8	0	0	1	1	1	1	0	1	0	1	0	1	1	1	Erro
9	0	1	0	0	0	0	1	0	1	1	0	1	1	1	K
9	0	1	0	0	0	1	0	1	0	1	0	1	1	1	Erro
10	0	1	0	0	1	0	0	1	0	1	0	1	1	1	Erro
10	0	1	0	0	1	1	1	0	1	1	0	0	0	0	1
11	0	1	0	1	0	0	0	1	0	1	0	1	1	1	Erro
11	0	1	0	1	0	1	1	0	1	1	1	1	0	0	J
12	0	1	0	1	1	0	1	1	1	1	1	0	1	1	9
12	0	1	0	1	1	1	0	1	0	1	0	1	1	1	Erro
13	0	1	1	0	0	0	0	1	0	1	0	1	1	1	Erro
13	0	1	1	0	0	1	1	0	1	1	0	1	1	1	X
14	0	1	1	0	1	0	1	1	0	0	0	1	1	1	F
14	0	1	1	0	1	1	0	1	0	1	0	1	1	1	Erro
15	0	1	1	1	1	0	1	1	1	1	0	0	0	0	7
15	0	1	1	1	0	1	0	1	0	1	0	1	1	1	Erro
16	0	1	1	1	1	0	0	1	0	1	0	1	1	1	Erro
16	0	1	1	1	1	1	1	0	1	0	1	0	1	0	W
17	1	0	0	0	0	0	1	0	0	0	1	1	1	0	L
17	1	0	0	0	0	1	0	1	0	1	0	1	1	1	Erro
18	1	0	0	0	1	0	0	1	0	1	0	1	1	1	Erro
18	1	0	0	0	1	1	1	1	1	1	1	0	0	1	3
19	1	0	0	1	0	0	0	1	0	1	0	1	1	1	Erro
19	1	0	0	1	0	1	1	1	0	0	1	1	1	0	C
20	1	0	0	1	1	0	1	0	0	0	1	1	1	1	T
20	1	0	0	1	1	1	0	1	0	1	0	1	1	1	Erro
21	1	0	1	0	0	0	0	1	0	1	0	1	1	1	Erro
21	1	0	1	0	0	1	1	0	0	0	0	0	0	0	Vazio
22	1	0	1	0	1	0	1	0	0	0	0	0	0	0	Vazio
22	1	0	1	0	1	1	0	1	0	1	0	1	1	1	Erro
23	1	0	1	1	0	0	1	0	0	0	0	0	0	0	Vazio
23	1	0	1	1	0	1	0	1	0	1	0	1	1	1	Erro
24	1	0	1	1	1	0	0	1	0	1	0	1	1	1	Erro
24	1	0	1	1	1	1	1	0	0	0	0	0	0	0	Vazio
25	1	1	0	0	0	0	0	1	0	1	0	1	1	1	Erro
25	1	1	0	0	0	1	1	0	0	0	0	0	0	0	Vazio
26	1	1	0	0	1	0	1	0	0	0	0	0	0	0	Vazio
26	1	1	0	0	1	1	0	1	0	1	0	1	1	1	Erro
27	1	1	0	1	0	0	1	0	0	0	0	0	0	0	Vazio
27	1	1	0	1	0	1	0	1	0	1	0	1	1	1	Erro
28	1	1	0	1	1	0	0	1	0	1	0	1	1	1	Erro
28	1	1	0	1	1	1	1	0	0	0	0	0	0	0	Vazio
29	1	1	1	0	0	0	1	0	0	0	0	0	0	0	Vazio
29	1	1	1	0	0	1	0	1	0	1	0	1	1	1	Erro
30	1	1	1	0	1	0	0	1	0	1	0	1	1	1	Erro
30	1	1	1	0	1	1	1	0	0	0	0	0	0	0	Vazio
31	1	1	1	1	0	0	0	1	0	1	0	1	1	1	Erro
31	1	1	1	1	0	1	1	0	0	0	0	0	0	0	Vazio
32	1	1	1	1	1	0	1	0	0	0	0	0	0	0	Vazio
32	1	1	1	1	1	1	0	1	0	1	0	1	1	1	Erro

### 3.2 Mapas de Karnaugh

Inicialmente é necessário visualizar o mapa de Karnaugh da Paridade:

Gerador Paridade

	000	001	011	010	110	111	101	100
00	1	0	1	0	1	0	1	0
01	0	1	0	1	0	1	0	1
11	1	0	1	0	1	0	1	0
10	0	1	0	1	0	1	0	1

Após verificar o modulo da paridade, é necessário fazer o mapa de Karnaugh para todas as saídas do display:

A

	000	001	011	010	110	111	101	100
00	1	1	1	0	1	1	0	1
01	0	0	1	0	1	0	0	0
11	0	0	0	0	0	0	0	0
10	0	1	0	1	0	0	0	0

B

	000	001	011	010	110	111	101	100
00	0	1	0	1	1	1	0	1
01	1	1	1	1	1	1	0	1
11	0	0	0	0	0	0	0	0
10	0	1	0	0	0	0	0	0

C

	000	001	011	010	110	111	101	100
00	1	1	1	1	1	0	1	1
01	1	1	1	1	1	0	0	1
11	0	0	0	0	0	0	0	0
10	0	1	0	0	0	0	0	0

D

	000	001	011	010	110	111	101	100
00	1	0	0	0	1	0	1	1
01	0	0	1	1	0	1	0	0
11	0	0	0	0	0	0	0	0
10	1	1	1	1	0	0	0	0

	E							
	000	001	011	010	110	111	101	100
00	0	1	1	0	1	1	1	0
01	1	0	0	1	0	0	1	1
11	0	0	0	0	0	0	0	0
10	1	0	1	1	0	0	0	0

	F							
	000	001	011	010	110	111	101	100
00	1	1	0	1	1	1	0	1
01	1	0	1	0	0	1	1	1
11	0	0	0	0	0	0	0	0
10	1	0	1	1	0	0	0	0

	G							
	000	001	011	010	110	111	101	100
00	1	1	0	1	0	1	0	1
01	1	0	1	0	0	0	1	1
11	0	0	0	0	0	0	0	0
10	0	1	1	0	0	0	0	0

Dessa forma a simplificação de cada Mapa de Karnaugh fica:

$$\mathbf{P:} E1 \overline{E2} E3 \overline{E4} \overline{E5} + E1 \overline{E2} E3 E4 E5 + E1 \overline{E2} \overline{E3} E4 \overline{E5} + E1 \overline{E2} \overline{E3} \overline{E4} E5 + E1 E2 E3 \overline{E4} E5 + E1 E2 E3 E4 \overline{E5} + E1 E2 \overline{E3} E4 E5 + E1 E2 \overline{E3} \overline{E4} \overline{E5} + \overline{E1} E2 E3 \overline{E4} \overline{E5} + \overline{E1} E2 E3 E4 E5 + \overline{E1} E2 \overline{E3} E4 \overline{E5} + \overline{E1} E2 \overline{E3} \overline{E4} E5 + \overline{E1} E2 E3 \overline{E4} E5 + \overline{E1} \overline{E2} E3 E4 \overline{E5} + \overline{E1} \overline{E2} \overline{E3} E4 E5 + \overline{E1} \overline{E2} \overline{E3} \overline{E4} \overline{E5}$$

$$\mathbf{A:} \overline{E1} E3 E4 \overline{E5} + \overline{E1} \overline{E2} E3 E4 + \overline{E1} \overline{E3} E4 E5 + \overline{E2} \overline{E3} \overline{E4} E5 + \overline{E1} \overline{E2} \overline{E4} \overline{E5} + E1 \overline{E2} \overline{E3} E4 \overline{E5} + \overline{E1} E2 E3 \overline{E4} E5$$

$$\mathbf{B:} \overline{E1} E2 \overline{E3} + \overline{E1} E3 \overline{E5} + \overline{E1} E3 E4 + \overline{E1} E4 \overline{E5} + \overline{E2} \overline{E3} \overline{E4} E5$$

$$\mathbf{C:} \overline{E1} \overline{E5} + \overline{E1} \overline{E3} + \overline{E1} \overline{E2} \overline{E4} + \overline{E2} \overline{E3} \overline{E4} E5$$

$$\mathbf{D:} E1 \overline{E2} \overline{E3} + \overline{E1} E2 E4 E5 + \overline{E1} E2 \overline{E3} E4 + \overline{E1} \overline{E2} E3 \overline{E4} + \overline{E1} \overline{E2} E3 \overline{E5} + \overline{E2} \overline{E3} \overline{E4} \overline{E5}$$

$$\mathbf{E:} \overline{E1} \overline{E2} E5 + E1 \overline{E2} \overline{E3} E4 + E1 \overline{E2} \overline{E3} \overline{E5} + \overline{E1} E2 E3 \overline{E4} + \overline{E1} E2 \overline{E3} \overline{E5} + \overline{E1} \overline{E2} E3 E4$$

$$\mathbf{F:} \overline{E1} \overline{E2} \overline{E3} \overline{E4} + \overline{E1} \overline{E4} \overline{E5} + \overline{E2} \overline{E3} \overline{E5} + \overline{E1} \overline{E2} E3 E4 + \overline{E1} E2 E4 E5 + \overline{E1} E2 E3 \overline{E4} + E1 \overline{E2} \overline{E3} E4$$

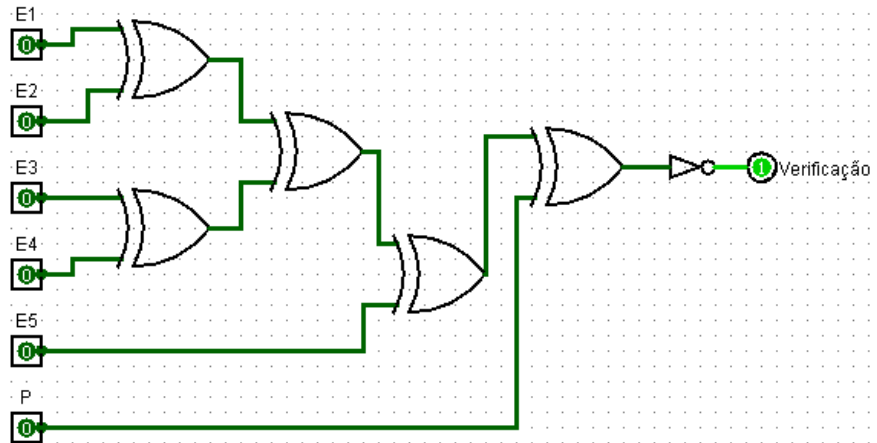
$$\mathbf{G:} \overline{E1} \overline{E2} \overline{E3} \overline{E4} + \overline{E1} \overline{E2} \overline{E3} \overline{E5} + \overline{E1} \overline{E4} \overline{E5} + \overline{E1} \overline{E2} E3 E4 E5 + \overline{E1} E2 \overline{E3} E4 E5 + \overline{E1} E2 E3 \overline{E4} + E1 \overline{E2} \overline{E3} E5$$

**Verificador Paridade:**  $\overline{E1 \oplus E2 \oplus E3 \oplus E4 \oplus E5 \oplus P}$

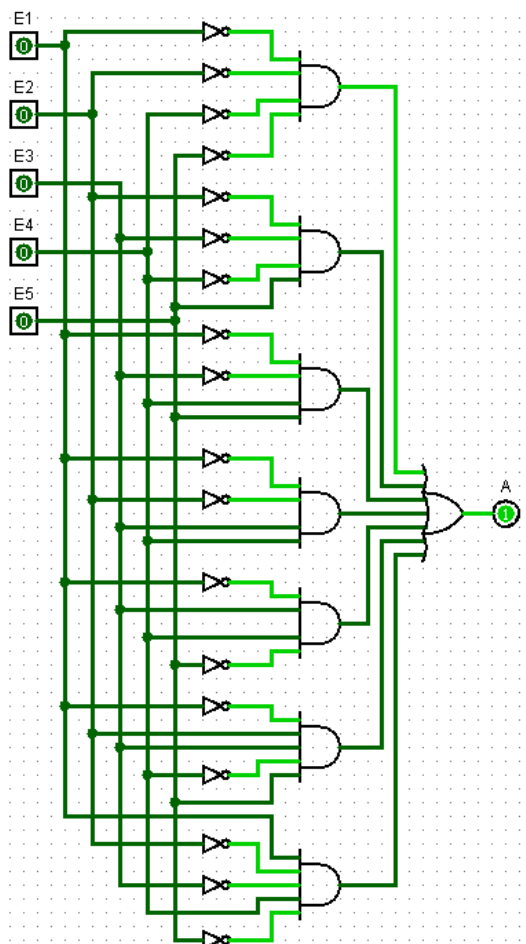
### 3.3 Diagramas de portas lógicas

Após descobrir a função booleana minimizada do gerador de paridade e da verificação de paridade e de cada saída, transformamos em portas lógicas com o auxílio do programa Logisim

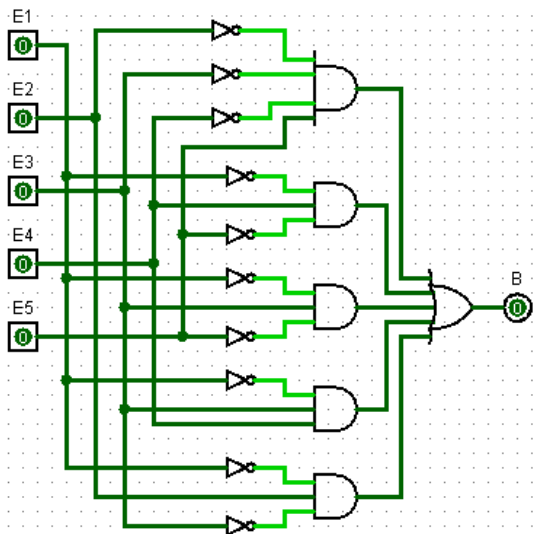
Verificador paridade:



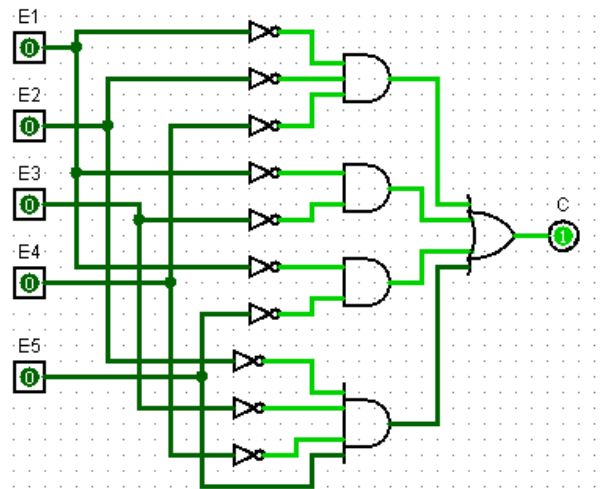
Saída A:



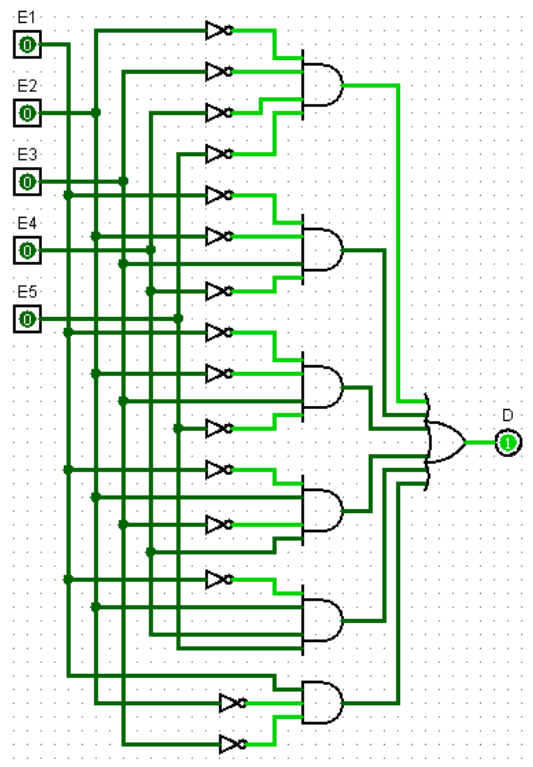
Saída B:



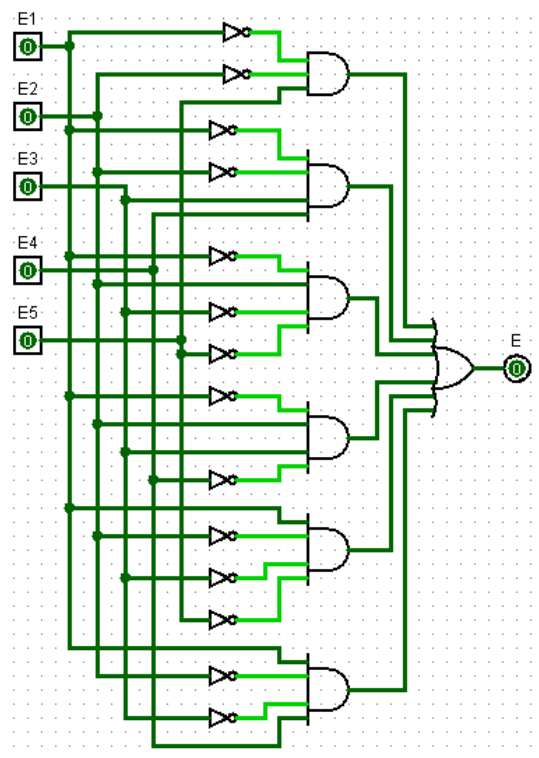
Saída C:



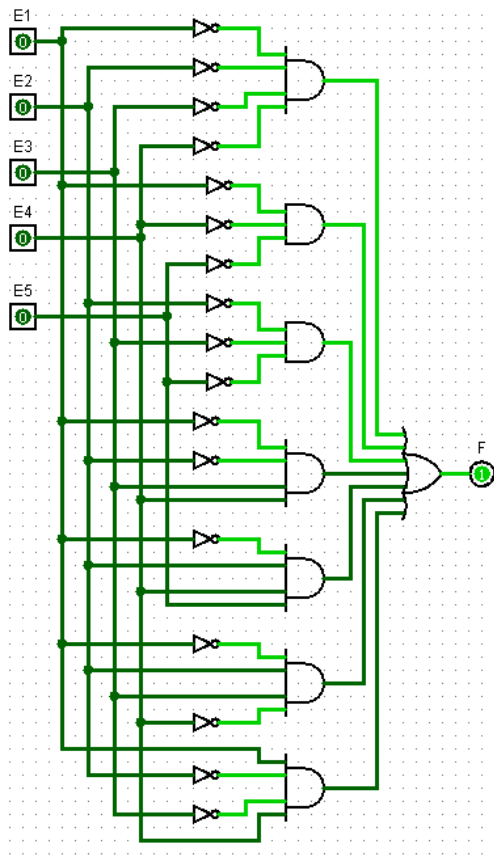
Saída D:



Saída E:



Saída F:



Saída G:

