Intelligent Targeting of Cell-Aware-Faults by the use of mandatory conditions

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Outline

1. Introduction
   - Cell-Aware-Type Faults
   - Cell Aware Type Example
   - Functional Simulation
   - Motivation

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   - Cell-Aware-Type UDFM Generation
   - Mandatory Condition Extraction
   - Circuit Goodstate Extraction Functional Simulation
   - Mandatory Counts During Functional Simulation

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3. Results & Analysis
   - Mandatory Counts as Fault Classifiers
   - Regression Analysis
4. Conclusion

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Previous Work

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  - Overview valid state space
- Extension of work on targeting very difficult stuck-at faults

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Note

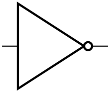
This type of fault is considered different than a pure cell-aware fault because no Analog analysis is required to generate tests. This will be illustrated during the next example

CAT Example

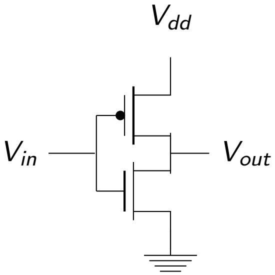
CAT Example

imagine you have an inverter...

CAT Example



CAT Example



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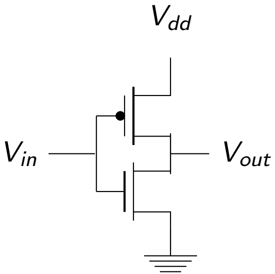


Transistor Parameters

$V_{tn} = V_{tp} = 0.7$ Volts.

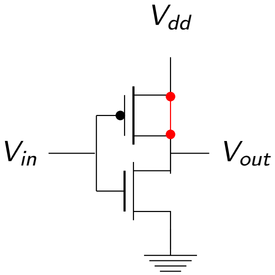
CAT Example

But Transistors are not linear elements, so our model is still not perfect...

CAT Example

During the manufacture of this inverter...

CAT Example



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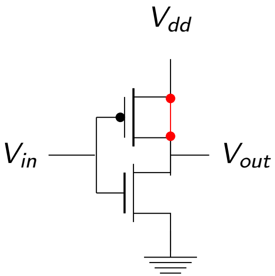

In this simple example cell...

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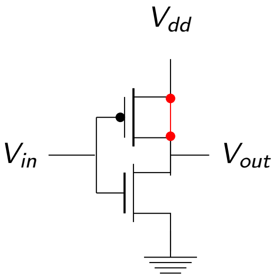

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Set $V_{in} = 1$, and observe $V_{out} = 1$

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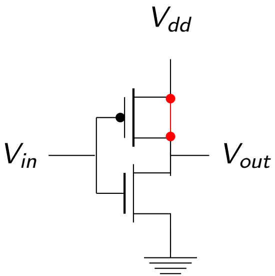

In this simple example cell...

Set $V_{in} = 1$, and observe $V_{out} = 1$

This analysis is difficult to perform on millions of transistors

CAT Example

With Cell-Aware-Type faults, we examine stuck-at ATPG test patterns...

CAT Example

With Cell-Aware-Type faults, we examine stuck-at ATPG test patterns...
And add patterns that cause conflict, but might not be choosen by ATPG tool.

Functional Simulation

Recall that the state space of an automaton refers to...

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All possible configurations of the memory elements in a device.

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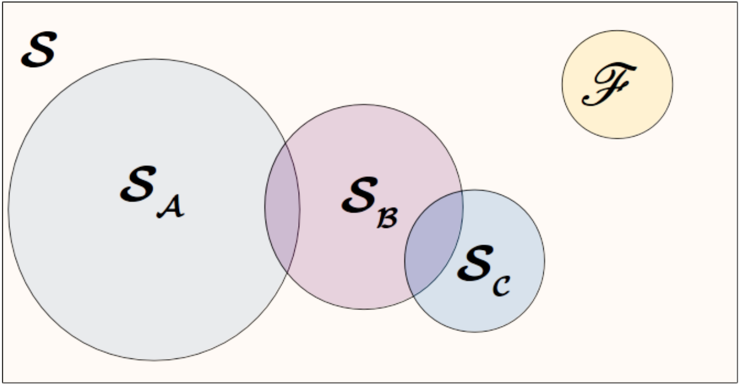
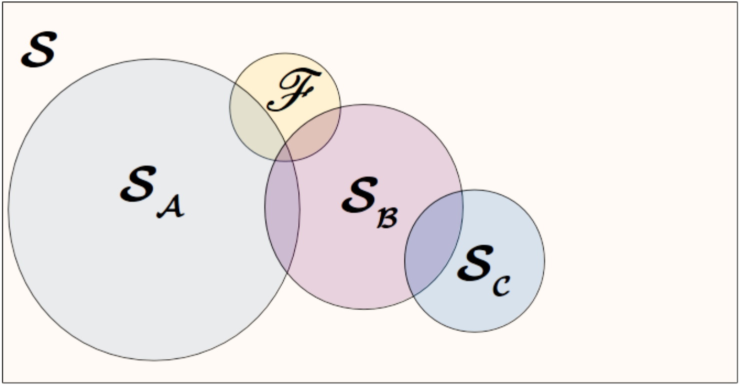
Recall that the state space of an automaton refers to...
All possible configurations of the memory elements in a device.
Consider a general purpose device that contains fault F as shown:

Functional Simulation



Functional Simulation



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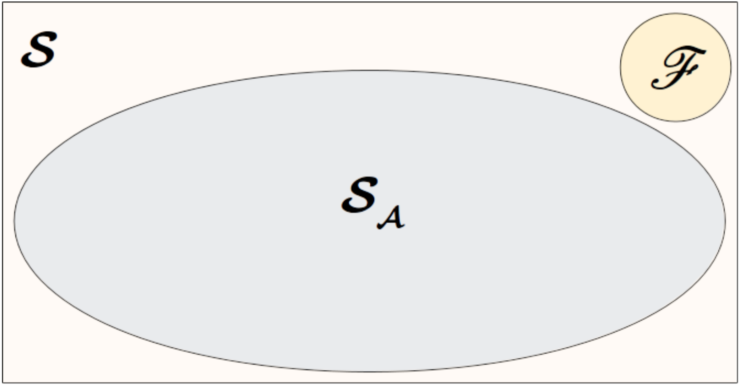

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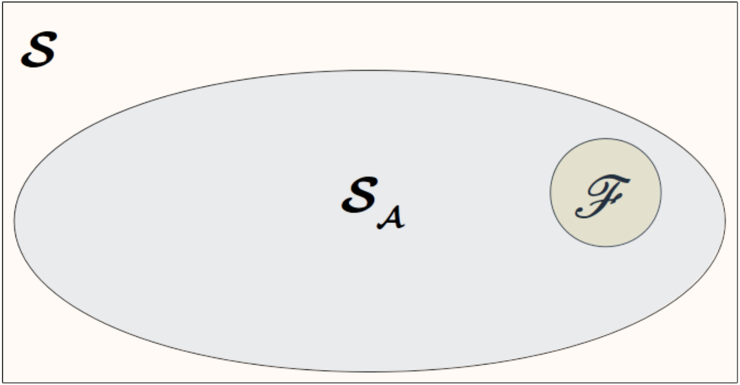

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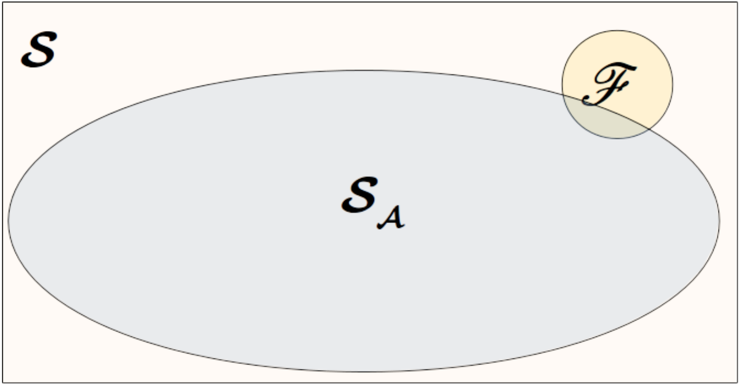

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ATPG for pure Cell-Aware Faults is Hard...

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It requires many resources (time/computational power)

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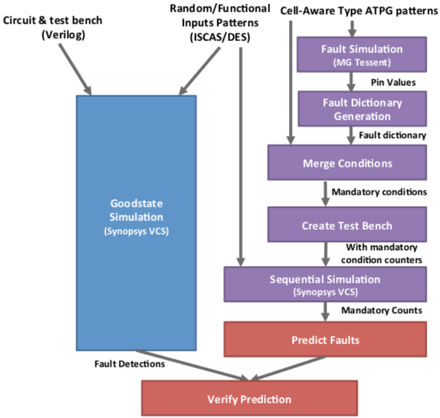
It requires many resources (time/computational power)
Let's prioritize faults using functional analysis of faults.

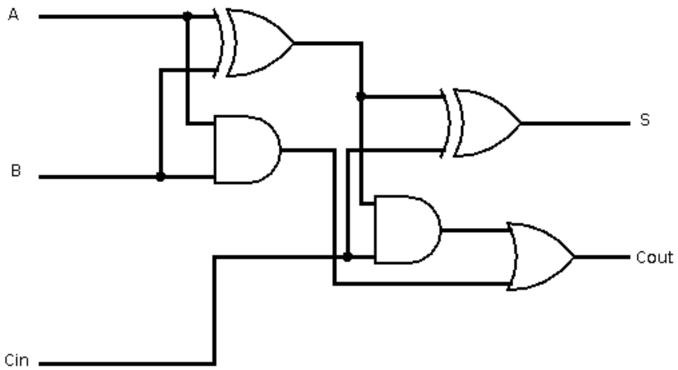
Flow Chart


Circuit & test bench
(Verilog)
Random/Functional
Inputs Patterns
(ISCAS/DES)
Cell-Aware Type ATPG patterns
Fault Simulation
(MG Tessent)
Pin Values
Fault Dictionary
Generation
Fault dictionary
Merge Conditions
Mandatory conditions
Create Test Bench
With mandatory
condition counters
Goodstate
Simulation
(Synopsys VCS)
Sequential Simulation
(Synopsys VCS)
Mandatory Counts
Predict Faults
Fault Detections
Verify Prediction

Cell-Aware-Type UDFM Generation

```
model s_faddx1_CO_(CO, CI, B, A)(
  model_source = verilog_udp;
  input (CI) ( )
  input (B) ( )
  input (A) ( )
  output (CO) (    )
  (
    primitive = _and mlc_sop_product_gate0 (B, A,
        mlc_product_net0_0);
    primitive = _and mlc_sop_product_gate1 (CI, A,
        mlc_product_net0_1);
    primitive = _and mlc_sop_product_gate2 (CI, B,
        mlc_product_net0_2);
    primitive = _or mlc_sop_sum_gate0 (mlc_product_net0_0,
        mlc_product_net0_1, mlc_product_net0_2, CO);
  ))
```

Cell-Aware-Type UDFM Generation



Cell-Aware-Type UDFM Generation

A	B	C_{in}	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Cell-Aware-Type UDFM Generation

```
Cell ( "FADDX1" ) {
    Fault ( "FADDX1_i000_o1" ){
        Test {
                StaticFault { "S" : 1; }
                Conditions { "A" : 0; "B": 0; "CI":
                    0;}
                        }
                }
    Fault ( "FADDX1_i000_o1" ) {
        Test {
                StaticFault { "CO" : 1; }
                Conditions { "A" : 0; "B": 0; "CI":
                    0;}
                        }
                }
        }
```

Mandatory Condition Extraction

Imagine you are testing a circuit with...

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Imagine you are testing a circuit with...
6 Primary Inputs
2 State Elements
you are looking for a fault f
and perform stuck-at-ATPG 4 times (or with n=4 on n-detect)

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These were the patterns that detected it...

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	Inputs	Flip-Flops
Pattern 1	010111	00
Pattern 2	001001	10
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Circuit Goodstate Extraction Functional Simulation

- This was reported on in the last publication.
- we inserted scanchains into circuits (ISCAS/DES56)
- Random inputs for ISCAS circuits
- Functional Testbench patterns for DES (both encryption and decryption)
- Captured state after every clock cycle, and had functional states for circuits.

Mandatory Counts During Functional Simulation

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- After determining the mandatory conditions for each circuit

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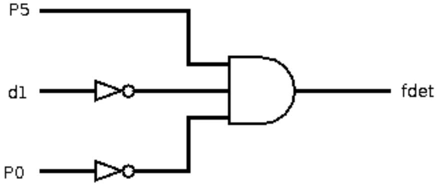
- After determining the mandatory conditions for each circuit
- Mandatory-Condition checking and gates were added to each circuit
- Using the goodstates we extracted
- We performed functional simulation on the circuit,
- and counted the number of times the mandatory conditions occurred.

MAND gates

Figure : Mandatory Condition Detector for fault f



ISCAS s9234

		Detected	
		T	F
Predicted	T	453 (TP)	119 (FP)
	F	0 (FN)	462 (TN)

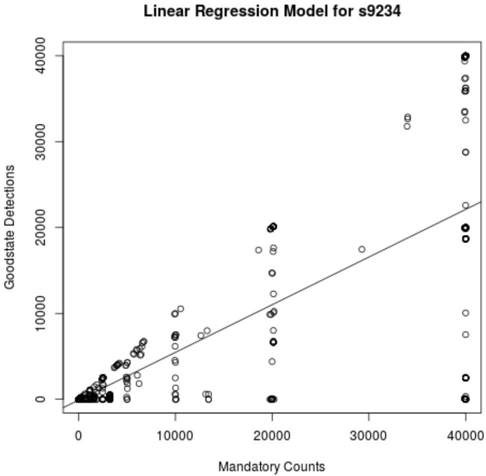
Statistic	Value
Precision	79%
Accuracy	88%
Specificity	79%
Fall-out	20.5%

DES 56

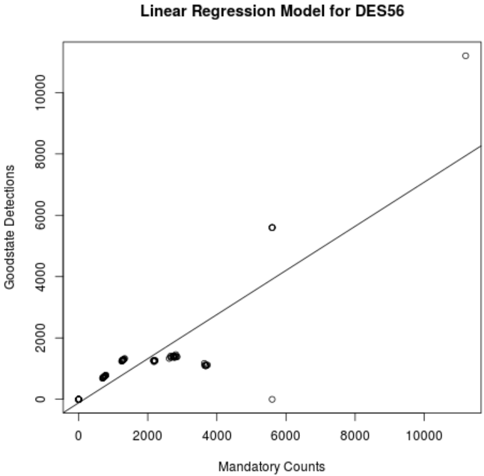
		Detected	
		T	F
Predicted	T	461 (TP)	2 (FP)
	F	0 (FN)	14 (TN)

Statistic	Value
Sensitivity	100%
Accuracy	99.5%
Specificity	87.5%
Fall-out	14.2%
Precision	99.5%

ISCAS s9234


Linear Regression Model for s9234
Goodstate Detections
0
10000
20000
30000
40000
0
10000
20000
30000
40000
Mandatory Counts

DES 56


Linear Regression Model for DES56
Goodstate Detections
0
2000
4000
6000
8000
10000
0
2000
4000
6000
8000
10000
Mandatory Counts

Conclusion

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- Large number of C.A. Faults for given circuits
- Functional Simulation and Mandatory Conditions allow us to prioritize fault detections
- We provided examples of mandatory condition calculations, and showed how they could be used to predict whether or not a cell-aware fault is functional

Acknowledgement

The authors would like to thank Semiconductor Research Corporation who supports this research under Task ID 2465.001. The authors are also grateful for the support of our industrial liaisons.

Thank You

Questions?