When N-Detect Doesn't Detect: Cell-Aware-Type Faults and Stuck-At ATPG

Fanchen Zhang, Micah Thornton, Jennifer Dworak

***Abstract*—Cell-aware faults have been proposed to more effectively detect defects within gates. We investigate the effectiveness of different types of ATPG for efficiently detecting cell-aware-type faults that are most important during functional operation.**

CONTENTS

I. INTRODUCTION

II. PREVIOUS WORK

When a manufacturer goes about designing their test set, they have to realize that there is always an inherent trade off between the time used to complete the test and the coverage of defaults by the test set. Thus their goal is to examine a method whereby test pattern sets are created that are both effective and efficient.

In 1959 Eldred discovered a fault model called the "stuck-at fault model" that has since been used to generate a highly effective test set of a reasonable size [1] This model, unfortunately, breaks down in the presence of faults that do not behave as stuck-at faults. For these faults variations of n-detect test sets(which require that each fault be detected n times, where $n > 1$) are used. These tests obtain better fortuitous detection of faults that did not fit the model [2] [3] [4].

The notion of these n-detect test sets have been extended and optimized even further to ensure that each additional detection provides the best possible value, including the maximum excitation balance [5]. Some have even considered the site values in a particular region around a particular gate [6].

Other researchers in addition have proposed gate exhaustive tests, which attempt to ensure that all possible input combinations for each gate are tested [7]. These methods have a much higher defect coverage, but follow the general trade off between fault coverage and test time as discussed above.

All of the previously mentioned faults deal with the values that occur on the wires, and do not necessarily consider that faults can occur within the gates or "cells" themselves. In order to address this variety of fault, the cell-aware fault model was presented [8].This model was extensively tested and found to be a decent new model [9] [10] [11]. This model was subsequently compared with other models, and test set generation methods [12]. The one unfortunate thing about considering these additional models, as expected, the more models tested for the greater the test duration.

Although certain models test for all the possible faults that fit a certain fault model, it might be more beneficial to only consider the faults that would significantly affect the end user of the product. In the past it has been shown that stuck-at faults can be graded based on fault criticality and how estimates of such can be used to create effective test sets when testing resources are limited [13] [14]. Some researchers have even deemed that defective parts can be sold if it is unlikely that the end user will ever use the product in such a way that the defects that passed the test phase will ever effect them [15] [16].

III. ALGORITHM/ PROBLEM ETC.

A. Cell-Aware Fault Models and their Relation to Stuck-at ATPG

1) Cell-aware fault detection conditions:

2) Why n-detect ATPG Test Sets May Be Biased:

B. Determining which Cell-aware faults to target

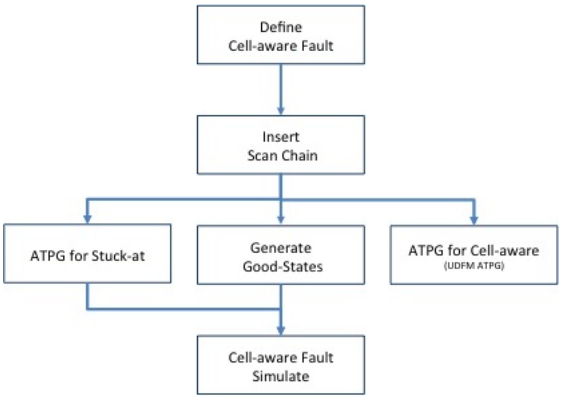
IV. EXPERIMENTAL SETUP & RESULTS

A. Set Up

To approve the effectiveness of functional cell-aware detection, s38584, s38417, s15850, s13207 and s9234 are chosen as benchmarks since they have more kind and larger number of gates among ISCAS89. The experiment Testing flow is shown in Fig.4. We create two different Cell-Aware fault sets except for two inputs gates as described in section 3. (Cell-Aware Fault Models and their Relation to Stuck-at ATPG), replaced all primitive gates with two more inputs by cell library. One Scan-Chain is inserted in each benchmark for testing. Then ATPG testing pattern sets for Stuck-at and Cell-aware faults are obtained on Mentor Graph- ics Tessent. To achieve N-detect of Stuck-at model effects on Cell-Aware faults, four setting up arguments for ATPG Stuck- at are implemented; they are n0 (disable multiple detection function), n1 (guaranteed detections=1, desired detections=3), n2 (guaranteed detections=2, desired detections=5) and n3 (guaranteed detections=3, desired detections=7). According to section 3, a test bench in which initializes DFFs as 0 to engender DFFs into

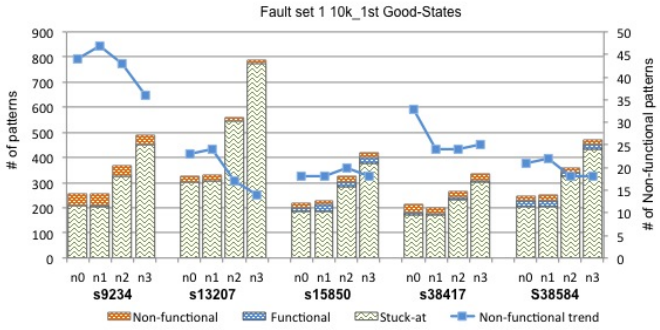
stable state is employed for capturing Good-State sets when Synopsys VCS simulates a golden benchmark. Note because the functionality of benchmarks are unknown, random patterns are created to represent the real functional inputs. In order to balancing randomness, we do two times of creating random pattern sets for each number of Good-States. Since UDFM of Tessent does not support N detection, we split Good-state sets and APTG sets into 5 patterns per simulation pattern file and repeat simulation processes multiple times.

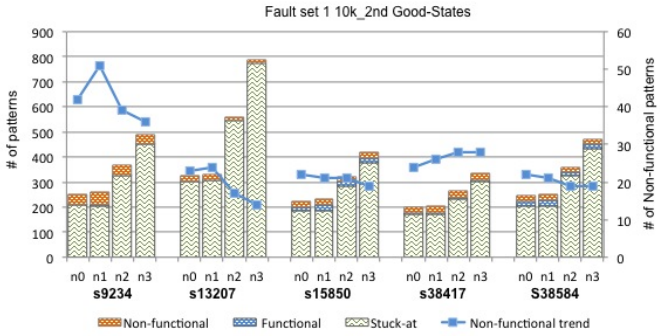
Flow of Set Up

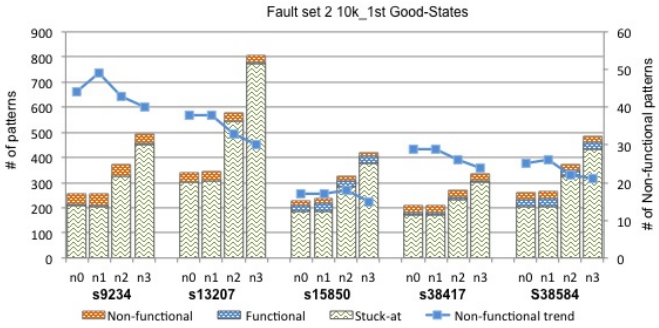


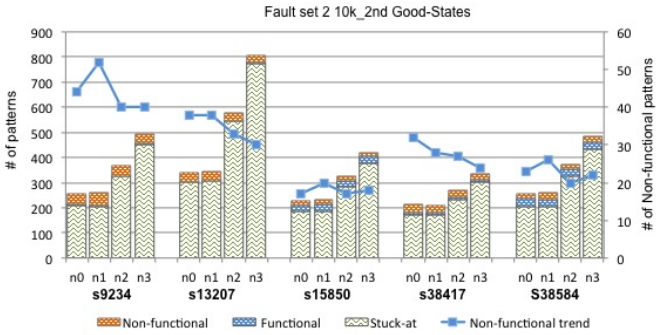
B. Results

Stuck-At Patterns V.S. Cell-Aware Top-Off Patterns



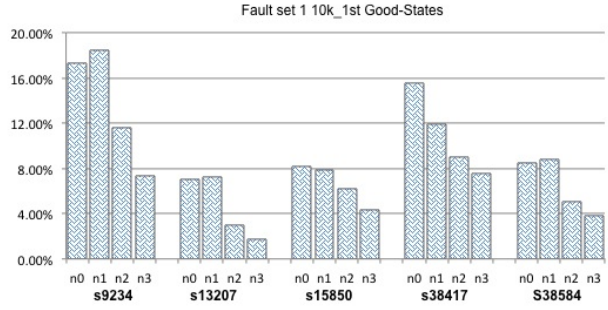


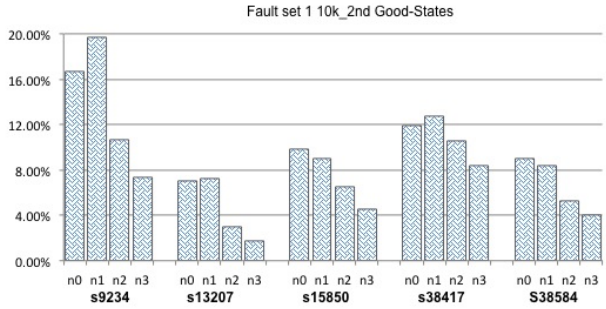


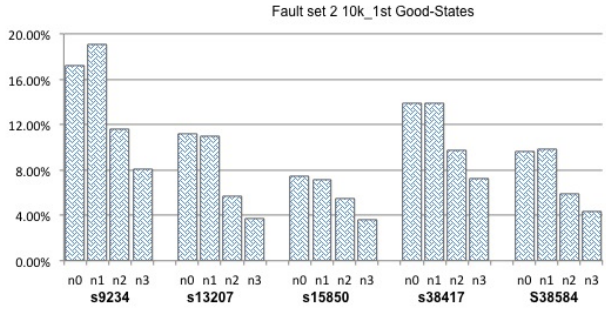


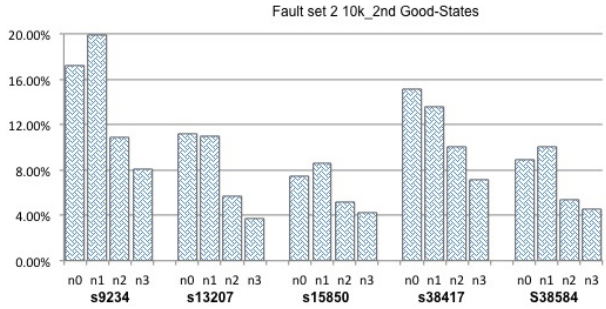
In the above figures we can see that two different generations of 10 000 good-states used on two different permutations of Cell-aware fault set yielded similar results. Another observation is that in each of the four cases there are more patterns that test for non-functional defects than those that tests for functional defects that are generated by cell aware ATPG, even in comparison with the large number of patterns generated by stuck-at ATPG, the number of non-functional patterns is significant. The number of functional test patterns is negligible compared to the large amount of patterns generated by the stuck-at ATPG. Because adding all of the non-functional tests to the test set adds significant costs, these figures suggest that using n-detect with a higher degree of n can decrease the number of non-functional tests which will decrease the added costs associated with testing all of the non-functional defects.

% Increase in Test Length When Non-Functional Cell-Aware Faults are Included in the Fault Set



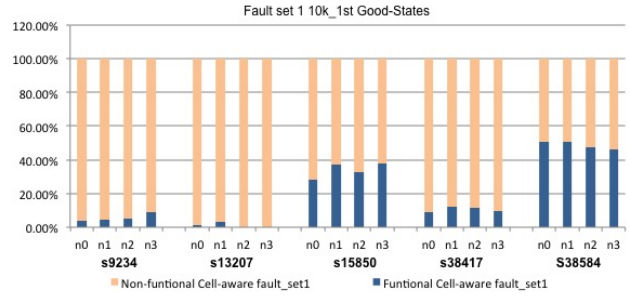


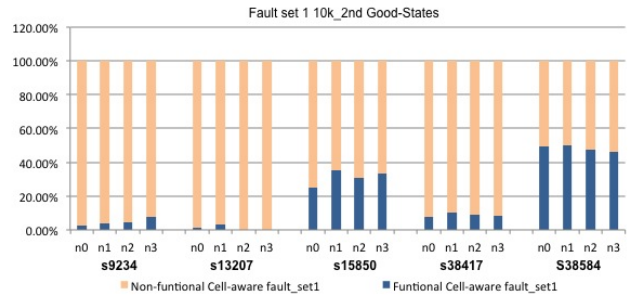


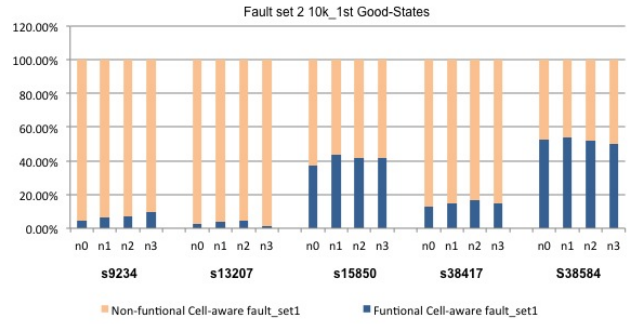


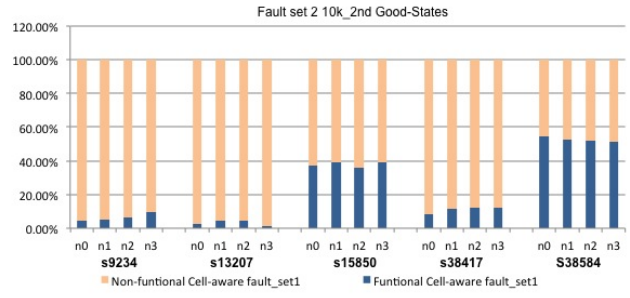
These graphs represent the total percentage of patterns that test for non-functional defaults generated by Cell-aware ATPG out of all Stuck-at ATPG plus functional Cell-aware ATPG patterns for each of the five circuits that were tested. Here again we see that two different sets of 10 000 good-states, as well as two different Cell-aware fault set's achieved similar results. As the n-detect redundancy increases we see a sharp decrease in the percentage of patterns that check for non-functional defects. Although even when we use n3 there remains 3 4% of patterns testing non-functional defects this is still a dramatic decrease from the normal percentage which is around 17 18% of all test patterns. This percentage decrease is not due to a decrease in the actual number of non-functional test patterns (as seen in figure 1), but an overall increase in the number of stuck-at ATPG patterns generated in response to the desired redundancy of the n-detect pattern generation.

Distribution of Cell-Aware Faults Between Functional Non-Functional for those not Detected by Stuck-At ATPG





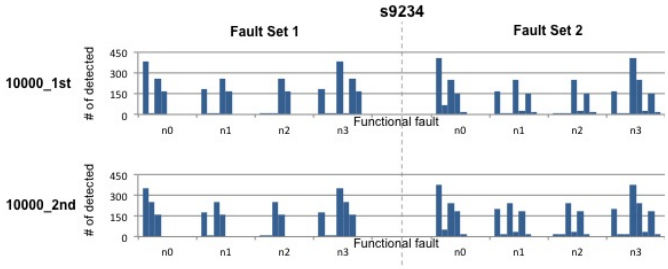


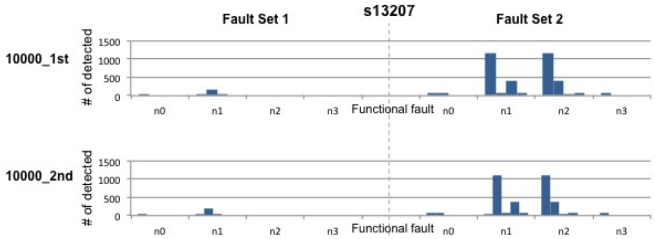


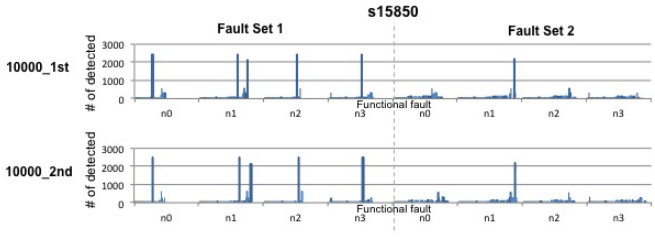
The above figures show the distribution of percentages of functional, and non-functional Cell-aware faults not detected by stuck-at ATPG. Once again the results were similar for all of the tested patterns and Cell-aware fault sets. Different

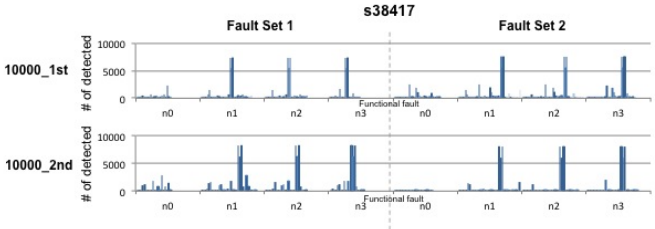
circuits obtained different distributions based on circuits characters. However we can see that the non-functional Cell-aware faults that were detected accounted for a large percentage of the total Cell-aware faults for those not detected by Stack-at ATPG . In s13207 the non-functional Cell-aware faults accounted for 97-100% of all non-detected Cell-aware faults by Stuck-at ATPG, even in s38584 non-functional Cell-aware faults accounted for 50-54% of the total non-detected Cell-aware faults by Stuck-at ATPG.

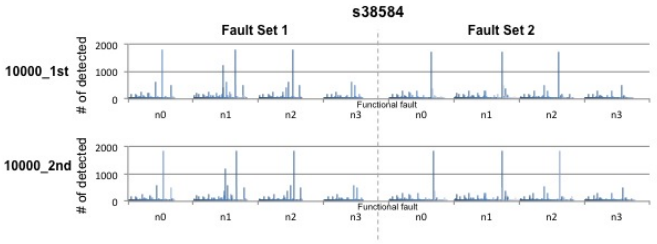
Number of Detections for each Fault Detected by Good-State Patterns











Here are charts for each of the five circuits that were tested. They show the number of functional faults that were detected based on Cell-aware fault sets used and the iteration of the test. The bars above each of the n-detect numbers represent the faults detected in each set of gates: AND, NAND, NOR, and OR respectively, with 2,3, and 4 input pins each. We noticed that some faults were detected only 2 or 3 times, whereas others were detected as many as 8 000 times. The faults that were detected many times are likely the most crucial faults. N-detect does not detect many important functional faults, even as n increases. This suggests that increasing the redundancy of the test set with n-detect is ineffective for examining these crucial functional faults.

# of Functional Faults Table

Benchmark		**s9234**				**s13207**				**s15850**				**s38417**				**s38584**			
n **number**		**n0**	**n1**	**n2**	**n3**	**n0**	**n1**	**n2**	**n3**	**n0**	**n1**	**n2**	**n3**	**n0**	**n1**	**n2**	**n3**	**n0**	**n1**	**n2**	**n3**
2*Fault Set 1	10k 1st	4	5	5	7	1	3	0	0	26	41	31	37	26	38	31	23	153	177	142	128
	10k 2nd	3	4	4	6	1	3	0	0	23	39	29	33	21	33	24	20	149	175	141	128
2*Fault Set 2	10k 1st	5	7	7	8	2	4	4	1	41	53	45	47	35	46	45	36	183	216	178	160
	10k 2nd	5	6	6	8	2	5	4	1	41	47	39	44	23	36	33	30	190	212	177	163

This table shows the number of functional Cell-aware faults in each circuit, because Cell-aware faults are inserted in each of the gates we can see that the larger the circuit, the more functional Cell-aware faults are inserted.

V. Conclusions

References

[1] R. D. Eldred, "Test routines based on symbolic logical statements," *J. ACM*, vol. 6, no. 1, pp. 33–37, Jan. 1959. [Online]. Available: http://doi.acm.org.proxy.libraries.smu.edu/10.1145/320954.320957

[2] S. Ma, P. Franco, and E. McCluskey, "An experimental chip to evaluate test techniques experiment results," in *Test Conference, 1995. Proceedings., International*, Oct 1995, pp. 663–672.

[3] I. Pomeranz and S. Reddy, "On n-detection test sets and variable n-detection test sets for transition faults," in *VLSI Test Symposium, 1999. Proceedings. 17th IEEE*, 1999, pp. 173–180.

[4] ——, "On the use of fault dominance in n-detection test generation," in *VLSI Test Symposium, 19th IEEE Proceedings on. VTS 2001*, 2001, pp. 352–357.

[5] J. Dworak, B. Cobb, J. Wingfield, and M. R. Mercer, "Balanced excitation and its effect on the fortuitous detection of dynamic defects," in *Proceedings of the Conference on Design, Automation and Test in Europe - Volume 2*, ser. DATE '04. Washington, DC, USA: IEEE Computer Society, 2004, pp. 21 066–. [Online]. Available: http://dl.acm.org.proxy.libraries.smu.edu/citation.cfm?id=968879.969191

[6] K. N. Dwarakanath and R. D. Blanton, "Universal fault simulation using fault tuples," in *Proceedings of the 37th Annual Design Automation Conference*, ser. DAC '00. New York, NY, USA: ACM, 2000, pp. 786–789. [Online]. Available: http://doi.acm.org.proxy.libraries.smu.edu/10.1145/337292.337779

[7] E. McCluskey and C.-W. Tseng, "Stuck-fault tests vs. actual defects," in *Test Conference, 2000. Proceedings. International*, 2000, pp. 336–342.

[8] F. Hapke and J. Schloeffel, "Introduction to the defect-oriented cell-aware test methodology for significant reduction of dppm rates," in *Test Symposium (ETS), 2012 17th IEEE European*, May 2012, pp. 1–6.

[9] J. Rajski, M. Potkonjak, A. Singh, A. Chatterjee, Z. Navabi, M. Guthaus, and S. Goren, "Embedded tutorials: Embedded tutorial 1: Cell-aware test-from gates to transistors," in *Very Large Scale Integration (VLSI-SoC), 2013 IFIP/IEEE 21st International Conference on*, Oct 2013, pp. xv–xvi.

[10] F. Hapke, M. Reese, J. Rivers, A. Over, V. Ravikumar, W. Redemund, A. Glowatz, J. Schloeffel, and J. Rajski, "Cell-aware production test results from a 32-nm notebook processor," in *Test Conference (ITC), 2012 IEEE International*, Nov 2012, pp. 1–9.

[11] F. Hapke, J. Schloeffel, H. Hashempour, and S. Eichenberger, "Gate-exhaustive and cell-aware pattern sets for industrial designs," in *VLSI Design, Automation and Test (VLSI-DAT), 2011 International Symposium on*, April 2011, pp. 1–4.

[12] F. Hapke, R. Krenz-Baath, A. Glowatz, J. Schloeffel, H. Hashempour, S. Eichenberger, C. Hora, and D. Adolfsson, "Defect-oriented cell-aware atpg and fault simulation for industrial cell libraries and designs," in *Test Conference, 2009. ITC 2009. International*, Nov 2009, pp. 1–10.

[13] Y. Shi, W.-C. Hu, and J. Dworak, "Too many faults, too little time on creating test sets for enhanced detection of highly critical faults and defects," in *VLSI Test Symposium (VTS), 2010 28th*, April 2010, pp. 319–324.

[14] Y. Shi, K. DiPalma, and J. Dworak, "Efficient determination of fault criticality for manufacturing test set optimization," in *Defect and Fault Tolerance of VLSI Systems, 2008. DFTVS '08. IEEE International Symposium on*, Oct 2008, pp. 403–411.

[15] M. A. Breuer and X.-a. Zhu, "A knowledge based system for selecting a test methodology for a pla," in *Proceedings of the 22Nd ACM/IEEE Design Automation Conference*, ser. DAC '85. Piscataway, NJ, USA: IEEE Press, 1985, pp. 259–265. [Online]. Available: http://dl.acm.org.proxy.libraries.smu.edu/citation.cfm?id=317825.317868

[16] T.-Y. Hsieh, K.-J. Lee, and M. A. Breuer, "Reduction of detected acceptable faults for yield improvement via error-tolerance," in *Proceedings of the Conference on Design, Automation and Test in Europe*, ser. DATE '07. San Jose, CA, USA: EDA Consortium, 2007, pp. 1599–1604. [Online]. Available: http://dl.acm.org.proxy.libraries.smu.edu/citation.cfm?id=1266366.1266717