VLSI

Exp. No. 6

Redhat Linux

Application → Terminal → csh →
source /home/install/cshrc → virtuoso &
→ log window occur

Go to tools → Lib manager → file → New
→ library → give name → okay

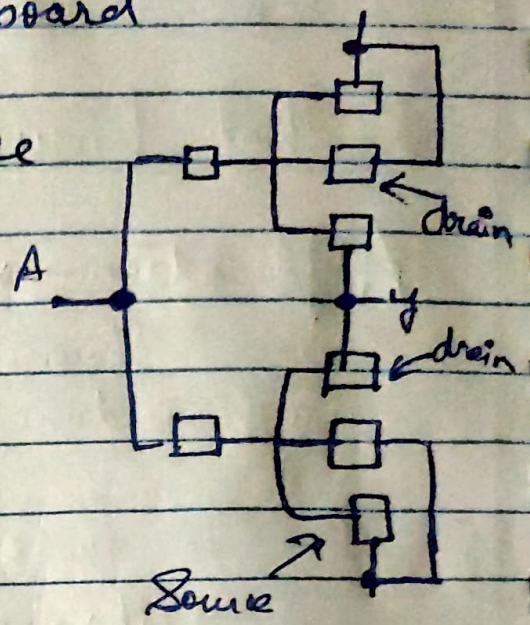
pop-up below occur → 4 options occur →
select attach to an existing library →
ok

in library part → file → new → cell view →
pop-up come → inside cell → give
name → Type → Schematic → ok

new window occur →
shortcut key → 2 : open mg add instance
lib → gpdk180
cell → pmos select → ok
— place on screen and then
esc
lib → gpdk180
cell → nmos

wire → press 'w' on keyboard

Sorting body terminal with source



select P on keyboard —

Name = Vdd gnd A

dir = input →

Connect Vdd at source of pmos and nmos

Create one more pin

Name → y

dir → o/p

Click save and check

* if there is an error go to log window and rectify

Changing the width of pmos

Select pmos and press 'q'

Change the width → 2 μm to 4 μm
length → 180nm

Save check again

Create option → Create cell view from cell view → nothing to be changed → click ok

Symbol generation pin occur
Left pin A
Right pin y
Top pin → Vdd
Bottom pin → gnd
and then okay

New window will occur

Delete the path name and delete the name → save check

→ go back to lib manager
→ go to file → new → cell view → pop-up → change the name → invert text → in invert → a new window will come → lib → name invAAAL → cell → inv → ok

Outer rectangle should exist which is invisible can be seen when mouse is near to circuit

Press 'I' → lib → analoglib cell → vdc → cell → vdc → hide put on screen

Press 'I' → lib → analog lib cell → v pulse

press 'I' → lib → analog lib
cell → gnd

Press 'W' →
connect vdc + to vdd.

Press 'P' → name y
dir ⇒ output
. save check

Launch → Adel → new window (tool used to simulate circuit)

Do some setting → setup → model lib → shows 1 lib 180nm ; if 90 & 45 nm is selected, deselect them → okay → analysis

go back to test circuit → select vdc → '0'
→ DC voltage : 1.8 (no symbols to be added)

select vpulse → '0' → voltage 1: remain same
voltage 2: 1.8V
period : 20n
(optional)
pulsewidth : 10n

→ ok → save check

→ go to adel → analysis → transient analysis
(voltage on one axis → time on one axis)

→ stop time → 40n → okay

→ window RHS → select setup output
→ new window → from design → it takes back to test circuit and then click once on output wire and input wire

→ setting : output → it show → y and net 7

analysis → tran
output → y, net 7
R. H. S. → green arrow (A) → Run

give a waveform window → split all script
→ right click on input and output and
change colour

Calculation :-

Delay - i.) Rising : 28.5105p
ii.) Falling : 20.974p

Propogation delay (t_p) : $\frac{28.5105 + 20.974}{2}$ = 24.742p

Rise time : 56.678p
Fall time : 39.99p