Exp 6B (Inverter)

Open InV
inv test →
Transistors have default 'l' and 'w'.

Launch > Layout XL > Open Popup > Okay

New file (pop up) → layout view (select).

Opens New window

Connectivity > Generate > All from Source.
Click okay (No changes).

Press Shift F → shows details about pmos & nmos.

Select transistor (turns white) → Q (properties) →
parameter → Body type (integrated)
(Connected to Sources)

1) Drag Vdd and Gnd to left side for easy connections.

Drag select & P → drag & leave

~~Contact poly~~

For poly to metal connection →

Drag poly to metal Connect

 → drag → stop → Right click → Wa down to → poly.

Save

DRC → design rule checker

Top Menu > Click Assura > Run DRC >
Open Pop Up Menu > Check Technology
gpdk 180 and Rule file added >
Click on OK if all things are right.

Assura > Run LVS > Opens pop up > Check Technology & Rule File > Click OK if all correct.
(Top Menu)

Assura > Run Quantus & RC > Extraction Panel >
Extraction Type > Check 'RC' & & Ref Node > Click on OK if alright.

ADEL pop window

delay → t_{PLH} = 35.0914p

t_{PHL} = 13.6383 p

ADEL window can be saved

Lib Manager

New File (av_extracted) → Double click to open →

Lib Manager → inv TEST → File → New → Cell View → New file (pop up) →
Use View → Change layout to config.

Configuration pop up.
Change View to schematic
Use template
Pop up → Name → spectre → OK
OK

Configuration Panel | IO → Right click →
Go to Tree View → Set instance
View to av_extracted

Inv test → config → double click →
popup → okay

Launch ADEL again → Netlist and Run
We will see increase in delay

Before:

$t_{PLH} = 35.0714p$
$t_{PHL} = 13.6383p$

After:

$t_{PLH} = 38.944p$
$t_{PHL} = 16.5358p$