

Exp 6B (Inverter)

Open Inv

inv test →

Transistors have default 'L' and 'W'.

Launch > Layout XL > Open Popup > Okay

New file (pop up) → layoutview (select).

Open New window

Connectivity > Generate > All from Source.
(Click okay (No changes)).

Press Shift F → shows details about pins & names.

Select transistor (two white) → Q (properties) →
parameter → Body type (integrated)

↓
Connected to Source(s)

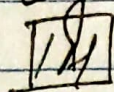
Drag Vdd and Gnd to left side for easy connections.

Drag Select & P → drag & leave

~~For poly~~

For poly to metal connection →

Drag poly to metal connect



→ drag → stop → Right click →
wa down to → poly

Save

DRC → design rule checker

Top Menu > Clicks Assura > Run DRC >

Open Pop Up Menu > Check Technology

gpad 180 and Rule file added >

Click on OK if all things are right.

Assura > Run LVS > Open pop up > Check Technology
(Top Menu) & Rule File > Click OK if all correct.

Assura > Run Quantus DRC > Extraction Panel >
Extraction Type > Check 'RC' & Ref
Node > Click on OK if alright.

ADEL per window

delay →

$$t_{PLH} = 35.0714 \text{ p}$$

$$t_{PHL} = 13.6383 \text{ p}$$

ADSL window can be saved

Lib Manager

New File (av - extracted) → ~~File~~ Double
click to open →

Lib Manager → invTEST → File → New →
Cell view → New file (pop up) →
the View → Change layout to Config.

Configuration pop up.

Change view to schematic

Use template

Pop up → Name → spectre → OK
OK

Configuration Panel | I/O → Right click →
Go to Tree View → Set instance
view to av - extracted

Inv test → config → double click →
popup → okay

Launch ADSL again → Netlist end Run
We will see increase in delay

Before:

$$t_{PLH} = 35.0714 \mu$$
$$t_{PHL} = 13.6383 \mu$$

After:

$$t_{PLH} = 38.944 \mu$$
$$t_{PHL} = 16.5358 \mu$$

✓
③
1/14/23