Checkpoint 3

Checkpoint 3 Progress Report

Status: We believe that we have completed all of checkpoint 3 functionality, with full data forwarding implemented and tested, along with a unified L2 cache in our cache hierarchy. We have written additional test code to check each of our forwarding paths, and we believe that our pipelined processor is correctly operating in each of the cases and can handle all needs of this.

Our multi-cycle L2 cache was made multicycle as our arbiter is clocked with registers and a state machine, allowing our critical path to not extend all the way to L2. This ensures that our fmax stays above the required 100MHz. At this time, it is the same size as our L1 cache, but we plan on expanding on its size in the future.

Testing: We wrote several test programs to test our forwarding and data hazard functionality, as the provided test code does not test all cases. Additionally, the provided test code is much longer and more complex, so writing smaller tests allowed us to incrementally test our forwarding paths.

Work Split:
Rohan worked on adding the multicycle L2 cache
Tanishq and Tadas implemented forwarding/data hazard/branch flushing

Checkpoint 4 Roadmap

Rohan is going to implement the performance counters and then help in the eviction write buffer
Tanishq and Tadas are going to work on the eviction write buffer
We already have static branch prediction (not taken), along with pipeline flushing if the branch is predicted incorrectly, so this is completed.