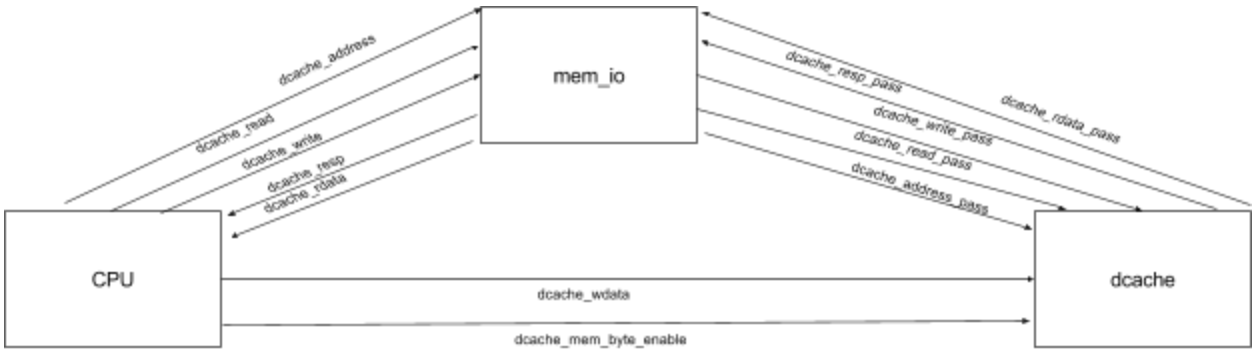
Performance Counters Design:



MEM_IO is going to essentially pass through the read/write/resp/rdata/address signals to dcache all the time combinationally, unless the address is found to be one of the memory mapped I/O addresses (near 0xFFFF)

If one of these addresses is read/written to, then mem_io will not pass through the read/write signals. On a read, it will set rdata to the counter value assigned to that specific address, and then send a resp back. On a write, it will set a counter reset wire high, which resets the counter in the specific stage it comes from.

Branch instruction/Branch taken counters are going to be in the MEM Stage, so that both counters can be kept in sync of each other.

IF Stalling counter will be placed into IR in the IF stage of the pipeline, where the stall originates.

MEM Stalling counter will be placed into the MEM stage of the pipeline, where that stalling originates.

Cache hits/misses will be placed into each of the cache's (icache, dcache, L2 cache) control logic.

All of these counters will also have a reset signals originating in mem_io and going to the other parts of the hierarchy. When the counters detect this signal is high, they will reset their value to 0.