File Comparison Report

...osed_Loop_Control_Voltage.slx vs. ...osed_Loop_Control_Voltage.slx
vlenzi
04-Jul-2024

Files

	Left File	Right File
File name	Closed_Loop_Control_Voltage	Closed_Loop_Control_Voltage
File path	C:\Users\vlenzi\AppData\Local\Temp\MatlabComparisons\8c3f8a0a-22f7-47cd-ad0b-a636088e8e75\b68de0f51e2fa0e09d3b880aa220e72cb2987b45\36213c06b6fa19b6a7c477b546fc8de956429867_0	C:\VersionControl\Git\MBD_for_SEPIC\Models\SoftwareModules
Last modified	04-Jul-2024 16:52:48	04-Jul-2024 16:40:09
MD5 checksum	f8d87c87f24dea34c25546d57788ef19	31a0bc92d0a1b82148623fb270b03d41
Model Version	9.57	9.59
Saved in Simulink version	R2024a	R2024a
Model Description		

Environment

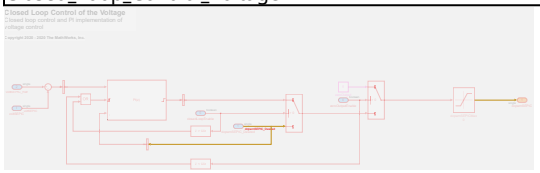
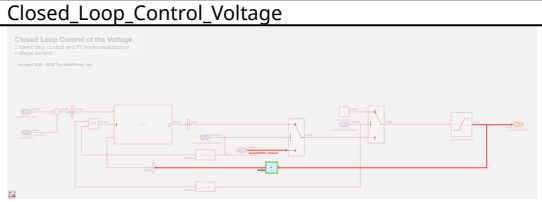
MATLAB 24.1 (R2024a)
Simulink24.1 (R2024a)

Filters

Filter Mode: hide
Built-In Filters
Nonfunctional Changes
Block Defaults
Custom Filters
No custom filters applied

Comparison Results

Simulink

Closed_Loop_Control_Voltage	Closed_Loop_Control_Voltage
	
Simulink	**Simulink**
	Unit Delay HasFrameUpgradeWarning : on BlockType : UnitDelay SampleTime : -1 Name : Unit Delay
Saturation:1 -> dcpwmSEPIC:1 SrcPort : 1 SrcBlock : Saturation DstBlock : dcpwmSEPIC DstPort : 1	

dcpwmSEPIC_Desired:1 -> Branch
SrcPort : 1
SrcBlock : dcpwmSEPIC_Desired
Name : dcpwmSEPIC_Desired

dcpwmSEPIC_Desired:1 -> Branch/Branch -> Data Type Conversion2:1
DstBlock : Data Type Conversion2
DstPort : 1

dcpwmSEPIC_Desired:1 -> Branch/Branch -> Switch1:3
DstBlock : Switch1
DstPort : 3

Saturation:1 -> Branch
SrcPort : 1
SrcBlock : Saturation

Saturation:1 -> Branch/Branch -> Unit Delay:1
DstBlock : Unit Delay
DstPort : 1

Saturation:1 -> Branch/Branch -> dcpwmSEPIC:1
DstBlock : dcpwmSEPIC
DstPort : 1

Unit Delay:1 -> Data Type Conversion2:1
SrcPort : 1
SrcBlock : Unit Delay
DstBlock : Data Type Conversion2
DstPort : 1

dcpwmSEPIC_Desired:1 -> Switch1:3
SrcPort : 1
SrcBlock : dcpwmSEPIC_Desired
DstBlock : Switch1
DstPort : 3
Name : dcpwmSEPIC_Desired

Custom Filter Details

No custom filters applied