Radio Frequency DC–DC Flyback Converter

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Abstract- **An RF (radio frequency) dc-dc converter has been developed to demonstrate the possibility of using a flyback configuration at 63 MHz. The converter consists of two sections: a variable pulse width generator (PWG) and a FET switch with a transformer and a detector. The bulk of the design effort was concentrated on improving the efficiency of the switch, the transformer and the detector. Low capacitances of the heterostructure AlGaAs/GaAs FET (HFET), a low leakage inductance of the RF transformer, a fast Schottky diode, multilayer ceramic chip capacitors and surface mount chip resistors made it possible to achieve high efficiencies from 20 MHz to 63 MHz. The "hard switching" 1-Watt converter achieves 60 to 70 percent efficiency, while operating with a wide range of input and output voltages.**

I. INTRODUCTION

Current spread spectrum wireless communications systems require very linear and efficient RF/microwave power amplifiers in conjunction with a closed loop adaptive power control. One of the possible applications of the fast dc-dc converter is to boost the efficiency of the power stage in wireless transmitters. Today's wireless communications systems use one of three multiple access schemes: TDMA - Time Division Multiple Access, FDMA - Frequency Division Multiple Access, or CDMA - Code Division Multiple Access. Popular CDMA Direct Sequence systems rely on tight reverse (adaptive) link power control, with a deleterious effect on capacity when the adaptive power control is not effective. A near-far effect, fast/slow fading, and the Doppler effect characterize the communication channel. In order to maintain maximum performance (capacity) of the system, the RF power of the transmitting stations must be constantly adjusted to the required level –"the right power, at the right place, at the right time." These power changes can be represented by three major statistical distributions:

$$\text{Lognormal} \quad p(x) = \frac{1}{\sigma\sqrt{2\cdot\pi}} \cdot \exp\left[\frac{-(x-m)^2}{2\cdot\sigma^2}\right] \tag{1}$$

$$\text{Rayleigh} \quad p(r) = \frac{r}{\sigma^2}\exp\left[-\frac{r^2}{\sigma^2}\right] \tag{2}$$

$$\text{Rician} \quad p(r) = \frac{r}{\sigma^2} \cdot \exp\left[\frac{-(r^2+a^2)}{2\cdot\sigma^2}\right] \bullet I_0\left(\frac{a\cdot r}{\sigma^2}\right) \tag{3}$$

where $I_0\left(\frac{a\cdot r}{\sigma^2}\right) = \frac{1}{2\pi}\int_0^{2\pi} \exp\left(\frac{a\cdot r\cdot\cos\theta}{\sigma^2}\right)\cdot d\theta$ (3a)

The average statistical efficiency of the RF amplifier is defined as:

$$\eta = \frac{\int P_{LRFout} \bullet g(P_{LRFout}) \bullet dP_{LRFout}}{\int f_{DC}(P_{LRFout}) \bullet g(P_{LRFout}) \bullet dP_{LRFout}} \tag{4}$$

where g(P) is probability density function.

In all these cases, the mean power of the signal is much smaller than peak power.

One way to increase the long-term efficiency of the RF power amplifier is to use Kahn's Envelope Elimination and Restoration Modulation Technique [1][2]. To reduce the dc power consumption when a low RF power is required, the dc voltage of the RF power amplifier is adaptively lowered which also improves the long-term efficiency [3]. Both schemes require a fast and efficient switching dc-dc converter. Due to feedback voltage control, the switching frequency should be at least two decades higher than the modulation frequency and/or the Adaptive Power Control update rate. The explosive growth of the Internet is driving the introduction of the third generation (CDMA2000) of wireless networks with data rates of up to 2.4 Mb/s. For backward compatibility with IS-95-B, CDMA2000 will support the following chip rates: 1.228, 3.686, 7.732, 11.059 and 14.745 Mchips/s [5].

To take full advantage of Kahn's technique, the dc voltage must be adjustable down to 0 Volts. For this or a similar application, the flyback scheme seems to be the best choice. With these stringent requirements, a 63 MHz flyback dc-dc converter was developed. In contrast to the buck or boost approaches, a flyback converter produces an output voltage which can be higher or lower than the input voltage.

II. DC-DC FLYBACK CONVERTER CRITERIA.

All dc-dc converters are based on timely voltage changes and timely current flow. Any deviation from that ideal timing will generate power losses due to a voltage/current overlap. At low frequencies, the on-resistance of the switch and on-resistance of the diode limit the maximum efficiency. At higher frequencies the situation is more complex and efficiency is limited mainly by parasitic capacitances and inductances (switching losses). The introduction of a transformer in a flyback converter lowers the efficiency even more. A time delay between primary and secondary, leakage inductances, and magnetic material cause energy losses, which are

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converted into heat. These major contributors to inefficiency may be summarized as follows:

$$P_{TotalLoss} = P_{DCloss} + P_{ONloss} + P_{OFFloss} + P_{magnetic} + P_{driver} \quad (5)$$

A. Conductive loss

At steady state, the FET drain-source resistance R_{DS}, the diode ON resistance R_D and the diode forward voltage drop V_D contribute to the conductive losses.

$$P_{DCloss} = I^2_{DSrms} \bullet R_{DS} + I^2_{Drms} \bullet R_D + I_{Dav} \bullet V_D \quad (6)$$

Resistances of the primary and the secondary of the transformer can be included into FET resistance and diode resistance, respectively.

B. Turn-on losses (switching losses).

$$P_{ONloss} = \frac{1}{2} \sum_n C_n \bullet V^{\,2}_{npeak} \bullet f_{SW} \quad (7)$$

C. Turn-off loss (switching loss from leakage inductance and time delays).

$$P_{OFFloss} = \int_0^{toff} v_{DS}(t) \bullet i_{DS}(t) \cdot dt^{\,2} \quad (8)$$

D. Magnetic loss.

Sometimes, it is convenient to state magnetic loss in the form of real permeability (μ_R);

$$\mu(f) = \mu_I(f) - j \cdot \mu_R(f) \quad (9)$$

In most cases, the core loss can be approximated as being proportional to the switching frequency times the peak inductor current squared [6].

$$P_{magnetic} \approx P_{core} \approx k_{core} \bullet I^2_{peak} \bullet f_{SW} \quad (10)$$

E. Drivers and Control Circuitry losses (not addressed in this paper).

In recent years, several high frequency, fully adjustable dc-dc converters have been developed. Most of them operate at switching frequencies ranging from 0.1 to 10 MHz and have the buck or boost configuration [2][3]. To produce a wide range of output voltages, a converter must operate close to a "hard switching" condition. At 60 MHz even small parasitic capacitances and/or inductances will reduce efficiency (see equations 7 and 8). The switching transistors, diodes, and the transformer pose real challenges. At switching frequencies around 60 MHz rise and fall times of a few nanoseconds require a magnetic core with low losses up to approximately 600 MHz.

III. CIRCUIT DESCRIPTION

The schematic diagram of the converter is shown in Fig 1. The converter contains two sections: a pulse width generator and a flyback converter.

A. Pulse Width Generator

The first section of the converter, from R1 through Q2, is a Pulse Width Generator (PWG), which operates at frequencies ranging from 9 to 100 MHz. The input is a 15 dBm sinusoidal wave from an RF signal generator. The pulse width at the output of Q2 is a function of the input RF power and frequency. By adjusting R1 it is possible to vary the duty ratio from 0 to 90 percent. This approach is very convenient if a test is performed over wide frequency ranges. The power consumption of this circuitry is not addressed here because the PWG was designed only for test purposes.

B. FET Switch

The use of a new high-frequency heterostructure AlGaAs/GaAs FET (HFET) from Stanford Microelectronics makes it possible to build a converter that can run at 60 MHz with reasonable efficiency over a wide range of output voltages. For currents up to 1.2 A, the on-resistance, at Vgs=+1 V, is approximately Rsd=0.6 ohms. The –3V gate bias must be used to protect the FET from conducting large saturation currents in situations where the pulse width is approaching or equal to zero. In applications where the output voltage never reaches zero (the duty ratio is always greater than zero) an external negative bias is not required.

C. Transformer

The transformer is used for two reasons. It electrically isolates the input from the output and steps up the voltage. A wide band RF transformer can model this pulse transformer. This is because the voltage and current pulses can be represented, in the frequency domain, as a number of harmonic sine waves. Additionally, fast transitions of the FET's drain current (~ 4 ns) produce voltage overshoot spikes across the leakage inductance (Lr, see Fig. 2). The magnitude of these spikes is related to Lr and di/dt (not counting parasitic capacitances):

$$V_{spike} = V_{D-S} - Lr \frac{dI_L}{dt} \quad (11)$$

At the same time, approaching this problem from another direction, we can say that rise and fall times are limited by leakage inductance (Lr) and parasitic capacitances (including the self capacitance of windings). These two components form a resonant circuit. In this situation the FET drain voltage as well as the diode voltage approach damped sinewaves. To minimize these effects, a multi aperture magnetic core was chosen. Transformer TR1 provides a 2:1voltage step up.

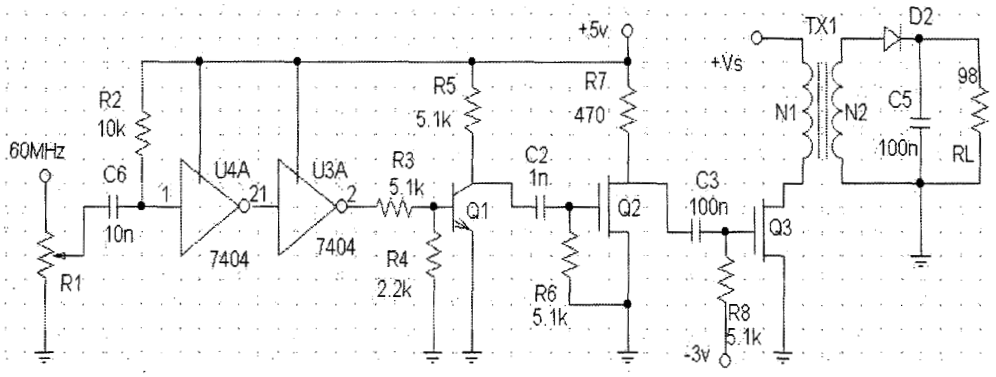

Fig. 1 63 MHz Flyback Dc-Dc Converter

It was constructed using one Fair-Rite # 2861002402 core, NiZn, u=120 with N1=3 turns of #28 wire on the primary and N2=6 turns of #32 wire on the secondary. Measured inductances were 2.9 μH and 10 μH respectively. An additional or separate magnetizing inductance (Lm) was not used.

D. *Schottky Diode*

The Agilent Technologies picosecond switching Schottky diode was chosen. Its low junction capacitance Co~7 pF at zero volts, short carrier lifetime $\tau = 100$ ps, low series resistance Rd ~ 0.7 Ohm, and small size make it usable in Flyback configuration at 60 MHz and above.

IV. PERFORMANCE MEASUREMENTS

Intensive tests showed that high efficiencies (60 to 70 percent) can be achieved at a wide range of input and output voltages. A summary of measurements is presented in Tables 1 and 2. Figures 2 and 3 show source to drain and diode voltages (waveforms) at 20 MHz and 63 MHz respectively. The voltage waveforms are slightly distorted by capacitances and resistances (impedances) of the oscilloscope probes (Tektronics).

V. CONCLUSIONS

This paper describes a recent advance in RF (radio frequency) dc-dc converters. The small size of surface mount components and circuitry described here, makes it possible to prototype a compact and efficient flyback dc-dc converter. All components are low cost and commercially available from mentioned manufacturers. To our knowledge, this is the first paper describing a successfully developed and tested 63 MHz dc-dc converter which is fully adjustable, hard switched, 60 to 70 percent efficient and can provide 1 Watt of dc output power.

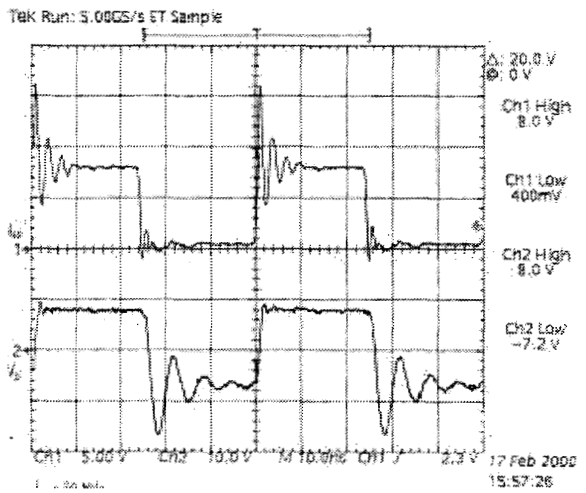

Fig. 2. Drain (Q3) and diode (D2) waveforms at 20 MHz.

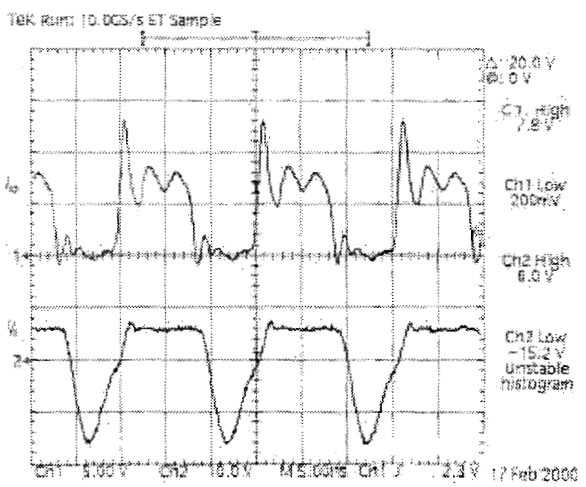

Fig. 3. Drain (Q3) and diode (D2) waveforms at 63 MHz.

Is	0.1	0.1	0.1	0.2	0.2	0.2	0.2	0.2	0.3	0.3	0.3	0.4
Vo	4	5	6	7	7.5	8	8.5	9	9.5	10	11	11
Ps	0.3	0.4	0.6	0.8	0.8	0.9	1.1	1.2	1.4	1.5	1.7	2
Po	0.16	0.26	0.37	0.50	0.57	0.65	0.74	0.83	0.92	1.02	1.13	1.23
Eff	54	57	61	66	68	69	70	69	68	68	65	63

Table 1.
Fsw=63 MHz, Vs=4.5 V, RL=98 ohms, Q3 – SHF-0589, D2-HSMS-270

Is	0.05	0.06	0.09	0.13	0.14	0.15	0.18	0.2	0.24	0.27	0.35
Vo	3.5	4	5	6	6.5	7	7.5	8	8.5	9	10
Ps	0.21	0.29	0.42	0.56	0.63	0.68	0.8	0.88	1.07	1.21	1.58
Po	0.13	0.16	0.26	0.37	0.43	0.50	0.57	0.65	0.74	0.83	1.02
Eff	60	57	60	65	68	74	72	74	69	69	65

Table 2.
Fsw=63 MHz; Vs=5 V; RL=98 ohms; Q3 –SHF-0589; D2-HSMS-270

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