# ALGO
# MCQ

0 = correct answer

1. **A graph can be ?**
   - (a) Directed
   - (b) Undirected
   - (c) Half-oriented
   - (d) Disoriented

2. **In a directed graph, the vertex x is adjacent to the vertex y if ?**
   - (a) There exists an arc (x,y)
   - (b) There exists an arc (y,x)
   - (c) There exists a path (x,..,y)
   - (d) There exists a path (y,..,x)

3. **In a directed graph, a vertex with degree zero is called?**
   - (a) unique vertex
   - (b) isolated vertex
   - (c) null vertex
   - (d) lost vertex

4. **A directed graph G generated by G=<S,A,C> is ?**
   - (a) labeled
   - (b) weighted
   - (c) valued
   - (d) numbered

5. **In a directed graph, we say that the arc $U = y \rightarrow x$ is ?**
   - (a) an x outgoing edge
   - (b) an x outcoming edge
   - (c) an x incoming edge
   - (d) an x ingoing edge

6. **In a directed graph the number of arcs coming into a vertex $x$ is called?**
   - (a) the outdegree of x
   - (b) the degree of x
   - (c) the indegree of x

7. **In an directed graph, if there is an arc between each pair of vertices $\{x, y\}$, the graph is ?**

   (a) complete
   (b) partial
   (c) perfect

8. **Two arcs of a digraph are considered adjacent if ?**

   (a) there exist two arcs connecting them
   (b) the graph is complete
   (c) they have at least one common end-point

9. **The order of a directed graph is?**

   (a) its number of arcs
   (b) its number of vertices
   (c) its cost
   (d) the ordered list of its arcs

10. **In a weighted directed graph G=<S,A,C>, the costs are given by ?**

    (a) the arcs
    (b) the vertices

# MCQ N°4

Monday, 21 October 2019

## Question 11

Which of the series below are power series ?

a. $\sum \ln(n+1)2^n$

b. $\sum e^n x^n$

c. $\sum 2^n x^{2n}$

d. none of the above

## Question 12

Consider a power series and let $R$ be its radius of convergence. Then

a. $R$ can be equal to $+\infty$

b. For any $x \in \mathbb{R}$ such that $|x| < R$, the series converges absolutely

c. For any $x \in \mathbb{R}$ such that $|x| > R$, the series converges absolutely

d. For any $x \in \mathbb{R}$ such that $|x| > R$, the series diverges

e. none of the above

## Question 13

Consider the power series $\sum \frac{x^n}{n!}$. Its radius of convergence is

a. $R = 2$

b. $R = 0$

c. $R = +\infty$

d. $R = 1$

e. none of the above

## Question 14

Consider the power series $\sum x^n$. Its radius of convergence is

a. $R = 2$

b. $R = 0$

c. $R = +\infty$

d. $R = 1$

e. none of the above

## Question 15

Let $\sum a_n x^n$ be a power series, $R \neq 0$ its radius of convergence and $f : \begin{cases} ]-R, R[ & \longrightarrow & \mathbb{R} \\ x & \longmapsto & \sum_{n=0}^{+\infty} a_n x^n \end{cases}$. Then

a. $f$ is continuous on $]-R, R[$

b. $f$ is differentiable on $]-R, R[$ and, for any $x \in ]-R, R[$, $f'(x) = \sum_{n=1}^{+\infty} n a_n x^{n-1}$

c. for any $x \in ]-R, R[$, $\int_0^x f(t)\mathrm{d}t = \sum_{n=0}^{+\infty} \frac{a_n}{n+1} x^{n+1}$

d. none of the above

## Question 16

Let $X$ be a random variable taking its values in $\{0, \ldots, n\}$. Then

a. $E(X) = G_X(1)$

b. $G_X(1) = 1$

c. $E(X) = G'_X(1)$

d. $E(X) = G''_X(1)$

e. none of the above

## Question 17

Let $X$ be a random variable taking its values in $\{0, \ldots, n\}$. Then its generating function is, for any $t \in \mathbb{R}$ :

a. $G_X(t) = E(t^X)$

b. $G_X(t) = \sum_{k=0}^{n} P(X = k)$

c. $G_X(t) = E(X^t)$

d. $G_X(t) = \sum_{k=0}^{n} t^k P(X = k)$

e. none of the above

## Question 18

Let $X$ be an integer-valued random variable whose generating function is $G_X(t) = a(2t+1)^2$. Then

a. $a = \frac{1}{9}$

b. $a = \frac{1}{3}$

c. $a = 1$

d. we cannot deduce the value of $a$ from these data

e. none of the above

## Question 19

Let $(u_n)$ be a strictly positive numerical sequence such that $\frac{u_{n+1}}{u_n} \xrightarrow[n\to+\infty]{} \frac{1}{4}$. Then

a. $\sum u_n$ converges

b. $\sum u_n$ diverges

c. we cannot say anything about the nature of $\sum u_n$

## Question 20

When $x$ tends to 0, one has

a. $\frac{1}{1+x} = 1 + x + x^2 + x^3 + o(x^3)$

b. $\frac{1}{1+x} = 1 - x + x^2 - x^3 + o(x^3)$

c. $\frac{1}{1-x} = 1 + x + x^2 + x^3 + o(x^3)$

d. $\frac{1}{1-x} = 1 - x + x^2 - x^3 + o(x^3)$

e. none of the above



5

QCM 4 Azar Chap13 (Adjecclause exs2, 3, 7)

Choose **all** possible pronouns that can be used to complete these sentences (21 – 23)

21. I paid the plumber ___ repaired my shower.
a. which
b. who
c. that
d. B and C.

22. Where is the newspaper __ has the article about online theft?
a. who
b. that
c. it
d. B and C.

23. Did you hear about the singer ___ won the Nobel Prize for literature?
a. that
b. which
c. he
d. whom

In 24 and 25, the two sentences have been combined for you, with the second sentence as an adjective clause. Which is the correct combination? (**Punctuation is taken into account**.)

24. I saw the boy. He forgot to buy the grammar book.
a. I saw the boy which forgot to buy the grammar book.
b. I saw the boy that forgot to buy the grammar book.
c. I saw the boy, he forgot to buy the grammar book.
d. I saw the boy who, forgot to buy the grammar book.

25. The student is angry. She missed her math test.
a. The student who missed her math test is angry.
b. The student that missed her math test is angry.
c. The student which missed her math test is angry.
d. A and B.

Choose the answer that includes **all** possible completions for each sentence below.

26. Tell me about the writers ___ you read when you were in college.
a. that
b. who
c. whom
d. – no change
e. All of the above.

27. Did John ask to see the video ___ my dad made when he was a boy?

a. who
b. which
c. that
d. – no change
e. B, C and D.

28. The people ___ I miss the most when I travel are my friends.

a. they
b. which
c. whom
d. None of the above.

29. The building ___ George Soros wanted to buy was no longer available.

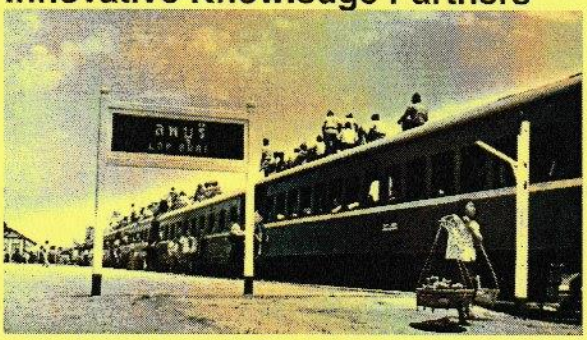
a. what
b. that
c. – no change
d. B and C.

30. The economists ___ supported Hillary Clinton in 2016 are quite well known.

a. that
b. who
c. — no change
d. A and B.
e. A, B and C.

WORLDBANK.ORG MAY 7 2019

## 70 Years in Thailand: From Traditional Development to Innovative Knowledge Partners



*One of the first loans to Thailand was for the rehabilitation of the Royal State Railways in October 1950. Improving the railway system helped connect all regions within Thailand and played a vital role in providing inland transportation and facilitating foreign trade.*

**STORY HIGHLIGHTS**

- The World Bank celebrates its 70th Anniversary on May 3 with Thailand, a partnership that has evolved from traditional lending and analytical services into an innovative-knowledge based partnership.

- In November 2018, the Bank launched a new Country Partnership Framework (CPF). Over the next 3 years, the Bank's focus will be to support reforms in Thailand to revive high growth and to help the country transform itself into a high-income economy.

- *"What I would like other countries and colleagues to know is that the development path of Thailand was never unidimensional, and neither was our partnership. The Bank always remains engaged, and together we learned and adapted our partnership,"* says Country Manager Birgit Hansl.

Back in 1952, third President of the World Bank, Eugene Black, visited Thailand for the first time and surveyed the Chaophraya River where a water control system was being built to irrigate farmlands in the Central Plain areas. Since becoming a member of the World Bank in 1949, Thailand's first World Bank engagements were made in the form of loans in 1950. In fact, these were also the World Bank's first loans in Southeast Asia. It was a time when the international institution's direct financial assistance to Thai development concentrated on the building of basic infrastructure – roads, dams, irrigation works, electricity, rail transport and port facilities – all of which helped enable the upsurge in production and commercial activity in the country. Today, seventy years later, Thailand has grown into a dynamic middle-income country, changing its relationship with the Bank from traditional lending and analytical services into an innovative knowledge-based partnership.

We checked in with Birgit Hansl, the new Country Manager for Thailand, on her plans for this time of transition and how other countries can learn from Thailand's growth story. Birgit's interview also comes as two significant events take place this month for the second largest economy in Southeast Asia – the crowning of a new King, an event that has not taken place since 1950, and the announcement of official election results.

As a trained economist with experience around the world, what about Thailand do you find the most intriguing, interesting or different?
Today, Eugene Black would have a hard time to recognize the Bangkok skyline, and I am sure he would be in awe of the development that happened along the Chaophraya River since his visit in 1952. Thailand is a development success story, with sustained strong growth and impressive poverty reduction. Now, Thailand's GNI per capita is around US$5,690, and extreme poverty is negligible.

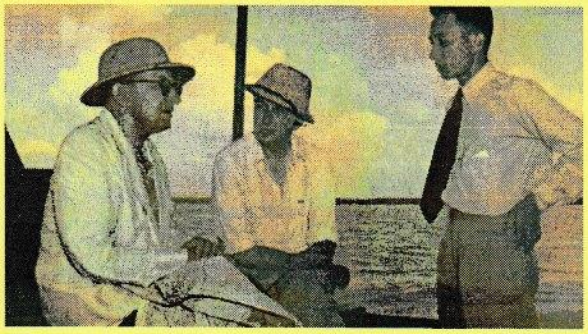
What is most fascinating to me is that Thailand's government and people are not content with these achievements, but they are focused on how to overcome key challenges for the country's next transition to a high-income country, and most of all, they are focused on how to ensure that all of society will be part of this transition. While in the past the government of Thailand and the World Bank Group's (WBG) had a traditional lending partnership with heavy focus on infrastructure investments, today, Thailand looks for our advice and expertise in a knowledge-based program. This provides us with a unique partnership with an ambitious upper middle-income country.

**What part of the seven-decade history of the World Bank in Thailand do you think people should know about?**

When we hear about development success stories like Thailand we often assume all went well all the time. But that is of course not true and there are many lessons to learn from how difficult times were overcome. What I would like other countries and colleagues to know is that the development path of Thailand was never unidimensional, and neither was our partnership. The WBG always remained engaged and a steadfast partner for Thailand even through difficult times, such as the period of economic turbulence following the first oil crisis in 1972-74, or the global financial crisis and the following recent period of political instability between 2008 and 2014. Together, we learned and adapted our partnership.

"Thailand is at the cusp of a new demographic transition as its population is rapidly aging. With the abundance of labor disappearing, productivity improvements by fostering an innovation-friendly competitive economy and equipping the young with the right skills will be of vital importance to sustain growth. "

Birgit Hansl
*Country Manager for Thailand*



*Back in 1952, third President of the World Bank, Eugene Black, visited Thailand for the first time and surveyed the Chaophraya River where a water control system was being built to irrigate farmlands in the Central Plain area.*

**Tell us about the plans for the Thailand office over the next 3 years, what are the opportunities for the most impactful World Bank engagement?**

Our current knowledge-based partnership with Thailand consists of reimbursable and trust-funded advisory services. Thailand signed its first-ever Reimbursable Advisory Services (RAS) agreement with the World Bank in late 2016, and the RAS program has been growing rapidly since then. Over the next 3 years, I would like the WBG to become a more strategic knowledge partner of the Thai government, especially for the future's most complex development challenges the country will face. Thailand is at the cusp of a new demographic transition as its population is rapidly aging.

With the abundance of labor disappearing, productivity improvements by fostering an innovation-friendly competitive economy and equipping the young with the right skills will be of vital importance to sustain growth. At the same time the need to finance pension systems and health services will rise fast. Our unique global knowledge and experience makes us the natural partner to lead the dialogue on such multifaceted development challenges of our middle-income clients.

In addition, our Bangkok office already plays an important role in supporting the WBG's operations in the region. Most of our staff based here is working on several countries in East Asia and the Pacific and South Asia. Our Bangkok office will need to evolve further to provide opportunities for more knowledge exchange among staff based here and for further strengthening the program support to neighboring countries.

**What could the political transition and royal coronation mean for Thailand?**

The upcoming royal coronation on May 4-6 is a rare event and provides the country with a new beginning to consider its future aspirations under Thailand's new King Maha Vajiralongkorn, Rama X. It follows another major milestone, the first elections since 2014, which took place peacefully on March 24, 2019. In my view, these are hopeful signs of a period of sustained stability for Thailand and the entire region.

Thailand is this year the ASEAN Chairman, promoting an agenda of sustainable development, with focus on human capital development, better connectivity and less pollution. Other countries acknowledge the development success of Thailand and look increasingly to Thailand for leadership in regional integration. These important events can be catalysts for Thailand's success in defining its new role and aspiration of sharing its development experience and promoting regional cooperation.

31) On Black's initial 1952 visit, the control system _____
a) had already been built.
b) was yet to be built.
c) had already been dismantled.
d) No information is given.

32) The World Bank's first loan to Thailand was the first of its kind _____.
a) globally
b) in the APAC region
c) in the EMEA region
d) in the AMER region

33) Thailand's economy rates ____ in the region.
a) as number two
b) as being premier
c) equal to other nations
d) as leader

34) The number of people living below the globally recognized poverty line is said to be _____.
a) down slightly
b) reduced
c) slight
d) significant

35) Thailand is categorized in _____ income bracket.
a) the upper-middle
b) the high
c) the middle
d) the low

36) The article indicates _____.
a) 4 unstable periods
b) 3 unstable periods
c) just one period of instability
d) No information is given

37) The first loan the country received was geared at _____.
a) improving agriculture
b) improving its transport infrastructure
c) Both (a) and (b)
d) Neither (a) nor (b)

38) The challenges hinted at in the text include: _____.
a) the young
b) retirees
c) health
d) All of the above

39) Thailand is very _____ sharing its experience with others.
a) open to
b) against
c) protective about
d) unwilling to move towards

40) In terms of development Thailand is being _____ as a success story.
a) derided
b) hailed
c) jeered
d) rallied against

*EPITA- S3*
*2019/2020*

# *M.C.Q test n°4 Physics*

Notes: the values q and Q are considered positive.

41 - Consider a charge $q$ at point O and a charge Q at point M. How can the electric potential energy $E_{pe}(M)$ on the point M be written ?

a) $E_{pe}(M) = k.\frac{q.Q}{OM}$
b) $E_{pe}(M) = k.\frac{q.Q}{OM^2}\overrightarrow{u_r}$, where $\overrightarrow{u_r}$ is the unit vector oriented from O to M.
c) $E_{pe}(M) = k.\frac{q}{OM^2}$

42 – The opposite of the electric potential gradient at a point M is :
a) A scalar
b) An absolute value
c) A vector

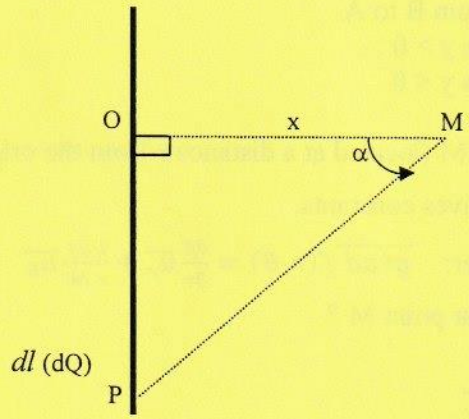
43- In polar coordinates $(r, \theta)$, which infinitesimal element $\overrightarrow{dl}$ doesn't exist ?

a) $\overrightarrow{dl} = rd\theta.\overrightarrow{u_\theta}$ b) $\overrightarrow{dl} = d\theta.\overrightarrow{u_\theta}$ c) $\overrightarrow{dl} = dr.\overrightarrow{u_r}$

44- The infinitesimal element of volume $dV$ in cylindrical is :

a) $dV = r.d\theta.dr.dz$
b) $dV = dx.dy.dz$
c) $dV = dr.d\theta.dz$

45- It can be proven that an infinitesimal element centered at point P on some wire, with a lineic charge $\lambda$, creates an electric field at some point M outside the wire which reads $dE_x(x) = \frac{k.\lambda}{x}\cos(\alpha)d\alpha$, where $\alpha$ is defined below.




The electric field created by an infinite wire is:

a) $E(x) = \frac{k\lambda}{x}$ b) $E(x) = \frac{2k\lambda}{x}$ c) $E(x) = 2\sin(\alpha)\frac{k\lambda}{x}$

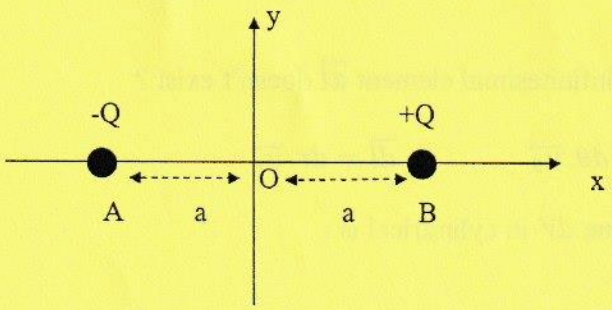
46 – How is the load element $dQ$ expressed as a function of the lineic charge $\lambda$ and the infinitesimal element of length $dl$?

a) $dQ = \frac{\lambda}{dl}$
b) $dQ = \lambda\, dl$
c) $dQ = -\lambda\, dl$

47- - A spherical charge distribution generates at point M an electric potential V(r, θ). It can thus be claimed that the electric field vector reads:

a) $\vec{E}\begin{pmatrix} E_r \\ 0 \\ E_\varphi \end{pmatrix}$ b) $\vec{E}\begin{pmatrix} 0 \\ E_\theta \\ E_\varphi \end{pmatrix}$ c) $\vec{E}\begin{pmatrix} E_r \\ E_\theta \\ 0 \end{pmatrix}$

48 – The following dipole is considered, the point O being located at the middle of AB:




The electric potential at the point A is:

a) $V(A) = k\frac{Q}{a}$ b) $V(A) = k\frac{Q}{2a}$ c) $V(A) = -k\frac{Q}{2a}$

49 - The situation in question 48 is considered. The electric field created by B on A is :

a) collinear to (AB), with orientation from A to B
b) collinear to (AB), with orientation from B to A
c) orthogonal to (AB), pointing towards y > 0
d) orthogonal to (AB), pointing towards y < 0

50 – A charge distribution creates at a point M (located at a distance r from the origin 0) a potential :

$V(r) = \frac{q}{4\pi\varepsilon_0}.\frac{1}{r}\, e^{-\frac{r}{a_0}}$ ; with $a_0$, q and $\varepsilon_0$ positives constants.

WTF IS THIS

Gradient expression in polar system reminder: $\overrightarrow{grad}\, f(r,\theta) = \frac{\partial f}{\partial r}\overrightarrow{u_r} + \frac{1}{r}\frac{\partial f}{\partial \theta}\overrightarrow{u_\theta}$

What is the electric field expression $\overrightarrow{E(M)}$ at point M ?

a) $\overrightarrow{E(M)} = \frac{q}{4\pi\varepsilon_0}.\left(\frac{1}{r^2} + \frac{1}{a_0\, r}\right) e^{-\frac{r}{a_0}}.\overrightarrow{u_r}$
b) $\overrightarrow{E(M)} = \frac{q}{4\pi\varepsilon_0}.\left(\frac{1}{r^3} + \frac{1}{a_0\, r^2}\right) e^{-r}.\overrightarrow{u_r}$
c) $\overrightarrow{E(M)} = \frac{1}{4\pi\varepsilon_0}.\left(\frac{a_0}{r^2} + \frac{1}{a_0\, r}\right) e^{-\frac{r}{a_0}}.\overrightarrow{u_r}$

12

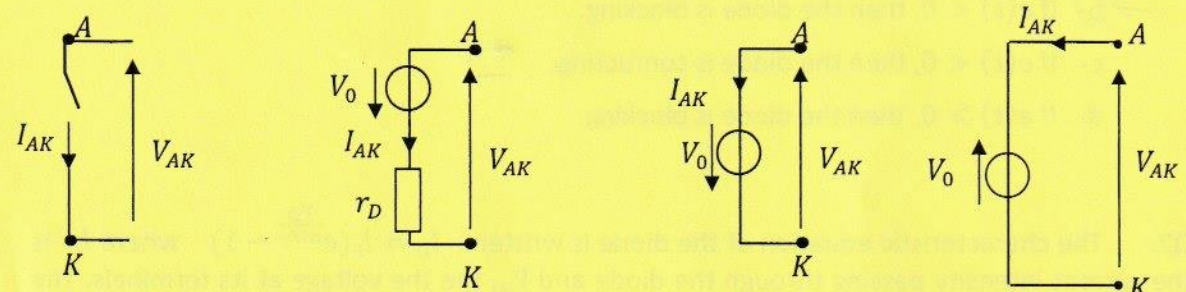
# MCQ test n°4 Electronics – InfoS3 ENG

Mind to well read the questions AND the answers suggested (be carreful about the answers numbering).

**Q1.** The doping allows the semi-conductor resistivity increase

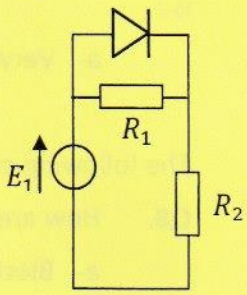
→ a- TRUE (b- FALSE)

**Q2.** By what would you replace the blocking diode if the threshold model is considered (ideal voltage source model) ?




→ a- b- c- d-

The following circuit is considered (Q 3 & 4) :




**Q3.** Choose the correct affirmation if $E_1 = 1V$, $R_1 = 50\Omega$, $R_2 = 100\Omega$ and if the diode is modelised by the threshold model (ideal voltage source) with $V_0 = 0{,}6V$ :

→ a- The diode is blocking and the voltage at its terminals is equal to $\frac{1}{3}V$.

b- The diode is conducting and the current passing through it is equal to $100mA$.

c- The diode is conducting and the current passing through it is equal to $5A$.

d- The diode is conducting and the current passing through it is equal to $200\ mA$.

**Q4.** Choose the correct affirmation if $E_1 = 10V$, $R_1 = 100\Omega$, $R_2 = 100\Omega$ and if the diode is considered as ideal :

a- The diode is blocking and the voltage at its terminals is equal to $5V$.

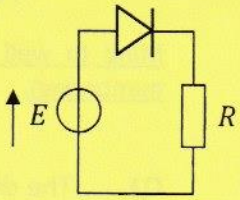
b- The diode is conducting and the current passing through it is equal to $50\ mA$.

→ c- The diode is conducting and the current passing through it is equal to $100mA$

d- The diode is conducting and the current passing through it is equal to $5A$

13

The following circuit in which the diode is assumed ideal (switch) is considered :




**Q5.** What is the voltage at the terminals of $R$ if $E = 10V$, $R = 100\Omega$.

a- $0\ V$
b- $1\ kV$
c- $10\ V$
d- $0{,}1\ V$

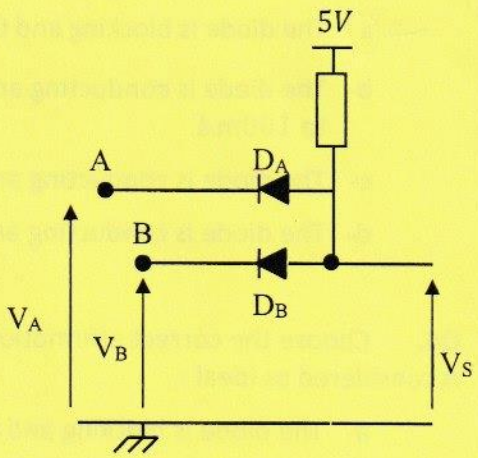
**Q6.** We consider now $e(t) = E_0\sqrt{2}.\sin(\omega.t)$. Choose the correct affirmation :

a- The diode is blocking and the voltage at its terminals is equal to $\frac{E_0.\sqrt{2}}{R}V$.
b- If $e(t) < 0$, then the diode is blocking.
c- If $e(t) < 0$, then the diode is confucting.
d- If $e(t) > 0$, then the diode is blocking.

**Q7.** The characteristic equation of the diode is written : $I_D = I_S(e^{\frac{V_D}{mV_T}} - 1)$ where $I_D$ is the current intensity passing through the diode and $V_D$, the the voltage at its terminals. The current and voltage arrows are in receiver convention. $I_S$ is the reverse current. This $I_S$ curent is :

a- Very high (several dozen of ampers )
b- Very low (quelqa few nano ampers)

The following circuit is considered :




**Q8.** How are the diodes if $V_A = V_B = 0V$ ?

a- Blocking
b- Conducting

**Q9.** How are the diodes if $V_A = V_B = 5V$ ?

a- Conducting
b- Blocking

**Q10.** What type of logic gate does this circuit realise ?

a- OR
b- AND
c- NAND
d- NOR

# Test 4
# Computer Architecture

**Monday 21 October 2019**

**For all the questions, one or more answers are possible.**

11. Let us consider the following instruction: `MOVE.W (A0)+,D0`
    A. A0 does not change.
    B. A0 is incremented by 4.
    C. A0 is incremented by 2.
    D. A0 is incremented by 1.

12. Let us consider the following instruction: `MOVE.W $50,D0`. What is the value `$50`?
    A. A 32-bit address.
    B. 32-bit immediate data.
    C. 8-bit immediate data.
    D. A 16-bit address.

13. Which instruction(s) can be used to call a subroutine?
    A. JMP
    B. GSR
    C. BSR
    D. BRA

14. After the execution of the `RTS` instruction, the stack pointer is:
    A. Decremented by two.
    B. Decremented by four.
    C. Incremented by two.
    D. Incremented by four.

15. The steps to pop an item off the stack are:
    A. Read the item from (A7) then increment A7.
    B. Write the item to (A7) then decrement A7.
    C. Increment A7 then read the item from (A7).
    D. Decrement A7 then write the item to (A7).

15

16. Let us consider the two following instructions:

```
CMP.L D1,D2
BLO   NEXT
```

Branch to NEXT if:

A. D1 = $FF0000FF and D2 = $FF0000FF
B. D1 = $00FFFF00 and D2 = $FF0000FF
C. D1 = $FF0000FF and D2 = $00FFFF00
D. D1 = $00FFFF00 and D2 = $00FFFF00

17. Let us consider the two following instructions:

```
CMP.L D1,D2
BLT   NEXT
```

Branch to NEXT if:

A. D1 = $FF0000FF and D2 = $FF0000FF
B. D1 = $00FFFF00 and D2 = $FF0000FF
C. D1 = $FF0000FF and D2 = $00FFFF00
D. D1 = $00FFFF00 and D2 = $00FFFF00

18. Let us consider the two following instructions:

```
CMP.W D1,D2
BLE   NEXT
```

Branch to NEXT if:

A. D1 = $FF0000FF and D2 = $FF0000FF
B. D1 = $00FFFF00 and D2 = $FF0000FF
C. D1 = $FF0000FF and D2 = $00FFFF00
D. D1 = $00FFFF00 and D2 = $00FFFF00

19. Let us consider the two following instructions:

```
CMP.B D1,D2
BLE   NEXT
```

Branch to NEXT if:

A. D1 = $FF0000FF and D2 = $FF0000FF
B. D1 = $00FFFF00 and D2 = $FF0000FF
C. D1 = $FF0000FF and D2 = $00FFFF00
D. D1 = $00FFFF00 and D2 = $00FFFF00

20. Let us consider the two following instructions:

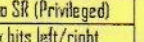
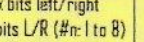
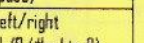
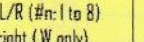
```
CMP.B D1,D2
BNE   NEXT
```

Branch to NEXT if:

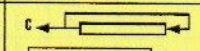
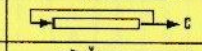
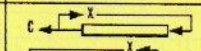
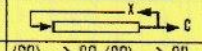
A. D1 = $FF0000FF and D2 = $FF0000FF
B. D1 = $00FFFF00 and D2 = $FF0000FF
C. D1 = $FF0000FF and D2 = $00FFFF00
D. D1 = $00FFFF00 and D2 = $00FFFF00

16

**EASy68K Quick Reference v1.8** http://www.wowgwep.com/EASy68K.htm 

| Opcode | Size | Operand | CCR | Effective Address s=source, d=destination, e=either, i=displacement | | | | | | | | | | | | Operation | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | BWL | s,d | XNZVC | Dn | An | (An) | (An)+ | -(An) | (i,An) | (i,An,Rn) | abs.W | abs.L | (i,PC) | (i,PC,Rn) | #n | | |
| ABCD | B | Dy,Dx | *U*U* | e | - | - | - | - | - | - | - | - | - | - | - | $Dy_{10} + Dx_{10} + X \rightarrow Dx_{10}$ | Add BCD source and eXtend bit to |
| | | -(Ay),-(Ax) | | - | - | - | - | e | - | - | - | - | - | - | - | $-(Ay)_{10} + -(Ax)_{10} + X \rightarrow -(Ax)_{10}$ | destination. BCD result |
| ADD [4] | BWL | s,Dn | ***** | e | s | s | s | s | s | s | s | s | s | s | s[4] | s + Dn → Dn | Add binary (ADDI or ADDQ is used when |
| | | Dn,d | | e | d[4] | d | d | d | d | d | d | d | - | - | - | Dn + d → d | source is #n. Prevent ADDQ with #n.L) |
| ADDA [4] | WL | s,An | ------ | s | e | s | s | s | s | s | s | s | s | s | s | s + An → An | Add address (.W sign-extended to .L) |
| ADDI [4] | BWL | #n,d | ***** | d | - | d | d | d | d | d | d | d | - | - | s | #n + d → d | Add immediate to destination |
| ADDQ [4] | BWL | #n,d | ***** | d | d | d | d | d | d | d | d | d | - | - | s | #n + d → d | Add quick immediate (#n range: 1 to 8) |
| ADDX | BWL | Dy,Dx | ***** | e | - | - | - | - | - | - | - | - | - | - | - | Dy + Dx + X → Dx | Add source and eXtend bit to destination |
| | | -(Ay),-(Ax) | | - | - | - | - | e | - | - | - | - | - | - | - | -(Ay) + -(Ax) + X → -(Ax) | |
| AND [4] | BWL | s,Dn | -**00 | e | - | s | s | s | s | s | s | s | s | s | s[4] | s AND Dn → Dn | Logical AND source to destination |
| | | Dn,d | | e | - | d | d | d | d | d | d | d | - | - | - | Dn AND d → d | (ANDI is used when source is #n) |
| ANDI [4] | BWL | #n,d | -**00 | d | - | d | d | d | d | d | d | d | - | - | s | #n AND d → d | Logical AND immediate to destination |
| ANDI [4] | B | #n,CCR | ===== | - | - | - | - | - | - | - | - | - | - | - | s | #n AND CCR → CCR | Logical AND immediate to CCR |
| ANDI [4] | W | #n,SR | ===== | - | - | - | - | - | - | - | - | - | - | - | s | #n AND SR → SR | Logical AND immediate to SR (Privileged) |
| ASL | BWL | Dx,Dy | ***** | e | - | - | - | - | - | - | - | - | - | - | - |  | Arithmetic shift Dy by Dx bits left/right |
| ASR | | #n,Dy | | d | - | - | - | - | - | - | - | - | - | - | s | | Arithmetic shift Dy #n bits L/R (#n: 1 to 8) |
| | W | d | | - | - | d | d | d | d | d | d | d | - | - | - |  | Arithmetic shift ds 1 bit left/right (.W only) |
| Bcc | BW [3] | address [2] | ------ | - | - | - | - | - | - | - | - | - | - | - | - | if cc true then | Branch conditionally (cc table on back) |
| | | | | | | | | | | | | | | | | address → PC | (8 or 16-bit ± offset to address) |
| BCHG | B L | Dn,d | --*-- | e[1] | - | d | d | d | d | d | d | d | - | - | - | NOT(bit number of d) → Z | Set Z with state of specified bit in d then |
| | | #n,d | | d[1] | - | d | d | d | d | d | d | d | - | - | s | NOT(bit n of d) → bit n of d | invert the bit in d |
| BCLR | B L | Dn,d | --*-- | e[1] | - | d | d | d | d | d | d | d | - | - | - | NOT(bit number of d) → Z | Set Z with state of specified bit in d then |
| | | #n,d | | d[1] | - | d | d | d | d | d | d | d | - | - | s | 0 → bit number of d | clear the bit in d |
| BRA | BW [3] | address [2] | ------ | - | - | - | - | - | - | - | - | - | - | - | - | address → PC | Branch always (8 or 16-bit ± offset to addr) |
| BSET | B L | Dn,d | --*-- | e[1] | - | d | d | d | d | d | d | d | - | - | - | NOT( bit n of d ) → Z | Set Z with state of specified bit in d then |
| | | #n,d | | d[1] | - | d | d | d | d | d | d | d | - | - | s | 1 → bit n of d | set the bit in d |
| BSR | BW [3] | address [2] | ------ | - | - | - | - | - | - | - | - | - | - | - | - | PC → -(SP); address → PC | Branch to subroutine (8 or 16-bit ± offset) |
| BTST | B L | Dn,d | --*-- | e[1] | - | d | d | d | d | d | d | d | d | d | - | NOT( bit Dn of d ) → Z | Set Z with state of specified bit in d |
| | | #n,d | | d[1] | - | d | d | d | d | d | d | d | d | d | s | NOT(bit #n of d ) → Z | Leave the bit in d unchanged |
| CHK | W | s,Dn | -*UUU | e | - | s | s | s | s | s | s | s | s | s | s | if Dn<0 or Dn>s then TRAP | Compare Dn with 0 and upper bound [s] |
| CLR | BWL | d | -0100 | d | - | d | d | d | d | d | d | d | - | - | - | 0 → d | Clear destination to zero |
| CMP [4] | BWL | s,Dn | -**** | e | s[4] | s | s | s | s | s | s | s | s | s | s[4] | set CCR with Dn - s | Compare Dn to source |
| CMPA [4] | WL | s,An | -**** | s | e | s | s | s | s | s | s | s | s | s | s | set CCR with An - s | Compare An to source |
| CMPI [4] | BWL | #n,d | -**** | d | - | d | d | d | d | d | d | d | - | - | s | set CCR with d - #n | Compare destination to #n |
| CMPM [4] | BWL | (Ay)+,(Ax)+ | -**** | - | - | - | e | - | - | - | - | - | - | - | - | set CCR with (Ax) - (Ay) | Compare (Ax) to (Ay); Increment Ax and Ay |
| DBcc | W | Dn,addres [2] | ------ | - | - | - | - | - | - | - | - | - | - | - | - | if cc false then { Dn-1 → Dn | Test condition, decrement and branch |
| | | | | | | | | | | | | | | | | if Dn <> -1 then addr →PC } | (16-bit ± offset to address) |
| DIVS | W | s,Dn | -***0 | e | - | s | s | s | s | s | s | s | s | s | s | ±32bit Dn / ±16bit s → ±Dn | Dn= [ 16-bit remainder, 16-bit quotient ] |
| DIVU | W | s,Dn | -***0 | e | - | s | s | s | s | s | s | s | s | s | s | 32bit Dn / 16bit s → Dn | Dn= [ 16-bit remainder, 16-bit quotient ] |
| EOR [4] | BWL | Dn,d | -**00 | e | - | d | d | d | d | d | d | d | - | - | s[4] | Dn XOR d → d | Logical exclusive OR Dn to destination |
| EORI [4] | BWL | #n,d | -**00 | d | - | d | d | d | d | d | d | d | - | - | s | #n XOR d → d | Logical exclusive OR #n to destination |
| EORI [4] | B | #n,CCR | ===== | - | - | - | - | - | - | - | - | - | - | - | s | #n XOR CCR → CCR | Logical exclusive OR #n to CCR |
| EORI [4] | W | #n,SR | ===== | - | - | - | - | - | - | - | - | - | - | - | s | #n XOR SR → SR | Logical exclusive OR #n to SR (Privileged) |
| EXG | L | Rx,Ry | ------ | e | e | - | - | - | - | - | - | - | - | - | - | register ←→ register | Exchange registers (32-bit only) |
| EXT | WL | Dn | -**00 | d | - | - | - | - | - | - | - | - | - | - | - | Dn.B → Dn.W \| Dn.W → Dn.L | Sign extend (change .B to .W or .W to .L) |
| ILLEGAL | | | ------ | - | - | - | - | - | - | - | - | - | - | - | - | PC→-(SSP); SR→-(SSP) | Generate Illegal Instruction exception |
| JMP | | d | ------ | - | - | d | - | - | d | d | d | d | d | d | - | ↑d → PC | Jump to effective address of destination |
| JSR | | d | ------ | - | - | d | - | - | d | d | d | d | d | d | - | PC → -(SP); ↑d → PC | push PC, jump to subroutine at address d |
| LEA | L | s,An | ------ | - | e | s | - | - | s | s | s | s | s | s | - | ↑s → An | Load effective address of s to An |
| LINK | | An,#n | ------ | - | - | - | - | - | - | - | - | - | - | - | - | An → -(SP); SP → An; | Create local workspace on stack |
| | | | | | | | | | | | | | | | | SP + #n → SP | (negative n to allocate space) |
| LSL | BWL | Dx,Dy | ***0* | e | - | - | - | - | - | - | - | - | - | - | - |  | Logical shift Dy, Dx bits left/right |
| LSR | | #n,Dy | | d | - | - | - | - | - | - | - | - | - | - | s | | Logical shift Dy, #n bits L/R (#n: 1 to 8) |
| | W | d | | - | - | d | d | d | d | d | d | d | - | - | - |  | Logical shift d 1 bit left/right (.W only) |
| MOVE [4] | BWL | s,d | -**00 | e | s[4] | e | e | e | e | e | e | e | s | s | s[4] | s → d | Move data from source to destination |
| MOVE | W | s,CCR | ===== | s | - | s | s | s | s | s | s | s | s | s | s | s → CCR | Move source to Condition Code Register |
| MOVE | W | s,SR | ===== | s | - | s | s | s | s | s | s | s | s | s | s | s → SR | Move source to Status Register (Privileged) |
| MOVE | W | SR,d | ------ | d | - | d | d | d | d | d | d | d | - | - | - | SR → d | Move Status Register to destination |
| MOVE | L | USP,An | ------ | - | d | - | - | - | - | - | - | - | - | - | - | USP → An | Move User Stack Pointer to An (Privileged) |
| | | An,USP | | - | s | - | - | - | - | - | - | - | - | - | - | An → USP | Move An to User Stack Pointer (Privileged) |
| | BWL | s,d | XNZVC | Dn | An | (An) | (An)+ | -(An) | (i,An) | (i,An,Rn) | abs.W | abs.L | (i,PC) | (i,PC,Rn) | #n | | |

17

| Opcode | Size | Operand | CCR | Effective Address s=source, d=destination, e=either, i=displacement | | | | | | | | | | | | Operation | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | BWL | s,d | XNZVC | Dn | An | (An) | (An)+ | -(An) | (i,An) | (i,An,Rn) | abs.W | abs.L | (i,PC) | (i,PC,Rn) | #n | | |
| MOVEA[4] | WL | s,An | ----- | s | e | s | s | s | s | s | s | s | s | s | s | s → An | Move source to An (MOVE s,An use MOVEA) |
| MOVEM[3] | WL | Rn-Rn,d | ----- | - | - | d | - | d | d | d | d | d | - | - | - | Registers → d | Move specified registers to/from memory |
| | | s,Rn-Rn | | - | - | s | s | - | s | s | s | s | s | s | - | s → Registers | (.W source is sign-extended to .L for Rn) |
| MOVEP | WL | Dn,(i,An) | ----- | s | - | - | - | - | d | - | - | - | - | - | - | Dn → (i,An)...(i+2,An)...(i+4,A. | Move Dn to/from alternate memory bytes |
| | | (i,An),Dn | | d | - | - | - | - | s | - | - | - | - | - | - | (i,An) → Dn...(i+2,An)...(i+4,A. | (Access only even or odd addresses) |
| MOVEQ[4] | L | #n,Dn | -**00 | d | - | - | - | - | - | - | - | - | - | - | s | #n → Dn | Move sign extended 8-bit #n to Dn |
| MULS | W | s,Dn | -**00 | e | - | s | s | s | s | s | s | s | s | s | s | ±16bit s * ±16bit Dn → ±Dn | Multiply signed 16-bit; result: signed 32-bit |
| MULU | W | s,Dn | -**00 | e | - | s | s | s | s | s | s | s | s | s | s | 16bit s * 16bit Dn → Dn | Multiply unsig'd 16-bit; result: unsig'd 32-bit |
| NBCD | B | d | *U*U* | d | - | d | d | d | d | d | d | d | - | - | - | 0 - $d_{10}$ - X → d | Negate BCD with eXtend, BCD result |
| NEG | BWL | d | ***** | d | - | d | d | d | d | d | d | d | - | - | - | 0 - d → d | Negate destination (2's complement) |
| NEGX | BWL | d | ***** | d | - | d | d | d | d | d | d | d | - | - | - | 0 - d - X → d | Negate destination with eXtend |
| NOP | | | ----- | - | - | - | - | - | - | - | - | - | - | - | - | None | No operation occurs |
| NOT | BWL | d | -**00 | d | - | d | d | d | d | d | d | d | - | - | - | NOT( d ) → d | Logical NOT destination (1's complement) |
| OR[4] | BWL | s,Dn | -**00 | e | - | s | s | s | s | s | s | s | s | s | s[4] | s OR Dn → Dn | Logical OR |
| | | Dn,d | | e | - | d | d | d | d | d | d | d | - | - | - | Dn OR d → d | (ORI is used when source is #n) |
| ORI[4] | BWL | #n,d | -**00 | d | - | d | d | d | d | d | d | d | - | - | s | #n OR d → d | Logical OR #n to destination |
| ORI[4] | B | #n,CCR | ===== | - | - | - | - | - | - | - | - | - | - | - | s | #n OR CCR → CCR | Logical OR #n to CCR |
| ORI[4] | W | #n,SR | ===== | - | - | - | - | - | - | - | - | - | - | - | s | #n OR SR → SR | Logical OR #n to SR (Privileged) |
| PEA | L | s | ----- | - | - | s | - | - | s | s | s | s | s | s | - | ↑s → -(SP) | Push effective address of s onto stack |
| RESET | | | ----- | - | - | - | - | - | - | - | - | - | - | - | - | Assert RESET Line | Issue a hardware RESET (Privileged) |
| ROL | BWL | Dx,Dy | -**0* | e | - | - | - | - | - | - | - | - | - | - | - |  | Rotate Dy, Dx bits left/right (without X) |
| ROR | | #n,Dy | | d | - | - | - | - | - | - | - | - | - | - | s | | Rotate Dy, #n bits left/right (#n: 1 to 8) |
| | W | d | | - | - | d | d | d | d | d | d | d | - | - | - |  | Rotate d 1-bit left/right (.W only) |
| ROXL | BWL | Dx,Dy | ***0* | e | - | - | - | - | - | - | - | - | - | - | - |  | Rotate Dy, Dx bits L/R, X used then updated |
| ROXR | | #n,Dy | | d | - | - | - | - | - | - | - | - | - | - | s | | Rotate Dy, #n bits left/right (#n: 1 to 8) |
| | W | d | | - | - | d | d | d | d | d | d | d | - | - | - |  | Rotate destination 1-bit left/right (.W only) |
| RTE | | | ===== | - | - | - | - | - | - | - | - | - | - | - | - | (SP)+ → SR; (SP)+ → PC | Return from exception (Privileged) |
| RTR | | | ===== | - | - | - | - | - | - | - | - | - | - | - | - | (SP)+ → CCR, (SP)+ → PC | Return from subroutine and restore CCR |
| RTS | | | ----- | - | - | - | - | - | - | - | - | - | - | - | - | (SP)+ → PC | Return from subroutine |
| SBCD | B | Dy,Dx | *U*U* | e | - | - | - | - | - | - | - | - | - | - | - | $Dx_{10}$ - $Dy_{10}$ - X → $Dx_{10}$ | Subtract BCD source and eXtend bit from |
| | | -(Ay),-(Ax) | | - | - | - | - | e | - | - | - | - | - | - | - | $-(Ax)_{10}$ - $-(Ay)_{10}$ - X → $-(Ax)_{10}$ | destination, BCD result |
| Scc | B | d | ----- | d | - | d | d | d | d | d | d | d | - | - | - | If cc is true then 1's → d | If cc true then d.B = 11111111 |
| | | | | | | | | | | | | | | | | else 0's → d | else d.B = 00000000 |
| STOP | | #n | ===== | - | - | - | - | - | - | - | - | - | - | - | s | #n → SR; STOP | Move #n to SR, stop processor (Privileged) |
| SUB[4] | BWL | s,Dn | ***** | e | s | s | s | s | s | s | s | s | s | s | s[4] | Dn - s → Dn | Subtract binary (SUBI or SUBQ used when |
| | | Dn,d | | e | d[4] | d | d | d | d | d | d | d | - | - | - | d - Dn → d | source is #n. Prevent SUBQ with #n.L) |
| SUBA[4] | WL | s,An | ----- | s | e | s | s | s | s | s | s | s | s | s | s | An - s → An | Subtract address (.W sign-extended to .L) |
| SUBI[4] | BWL | #n,d | ***** | d | - | d | d | d | d | d | d | d | - | - | s | d - #n → d | Subtract immediate from destination |
| SUBQ[4] | BWL | #n,d | ***** | d | d | d | d | d | d | d | d | d | - | - | s | d - #n → d | Subtract quick immediate (#n range: 1 to 8) |
| SUBX | BWL | Dy,Dx | ***** | e | - | - | - | - | - | - | - | - | - | - | - | Dx - Dy - X → Dx | Subtract source and eXtend bit from |
| | | -(Ay),-(Ax) | | - | - | - | - | e | - | - | - | - | - | - | - | -(Ax) - -(Ay) - X → -(Ax) | destination |
| SWAP | W | Dn | -**00 | d | - | - | - | - | - | - | - | - | - | - | - | bits[31:16] ← → bits[15:0] | Exchange the 16-bit halves of Dn |
| TAS | B | d | -**00 | d | - | d | d | d | d | d | d | d | - | - | - | test d → CCR; 1 → bit7 of d | N and Z set to reflect d, bit7 of d set to 1 |
| TRAP | | #n | ----- | - | - | - | - | - | - | - | - | - | - | - | s | PC → -(SSP);SR → -(SSP); | Push PC and SR. PC set by vector table #n |
| | | | | | | | | | | | | | | | | (vector table entry) → PC | (#n range: 0 to 15) |
| TRAPV | | | ----- | - | - | - | - | - | - | - | - | - | - | - | - | If V then TRAP #7 | If overflow, execute an Overflow TRAP |
| TST | BWL | d | -**00 | d | - | d | d | d | d | d | d | d | - | - | - | test d → CCR | N and Z set to reflect destination |
| UNLK | | An | ----- | - | d | - | - | - | - | - | - | - | - | - | - | An → SP; (SP)+ → An | Remove local workspace from stack |
| | BWL | s,d | XNZVC | Dn | An | (An) | (An)+ | -(An) | (i,An) | (i,An,Rn) | abs.W | abs.L | (i,PC) | (i,PC,Rn) | #n | | |

| Condition Tests (+ OR, ! NOT, ⊕ XOR; [u] Unsigned, [a] Alternate cc) | | | | | |
|---|---|---|---|---|---|
| cc | Condition | Test | cc | Condition | Test |
| T | true | 1 | VC | overflow clear | !V |
| F | false | 0 | VS | overflow set | V |
| HI[u] | higher than | !(C + Z) | PL | plus | !N |
| LS[u] | lower or same | C + Z | MI | minus | N |
| HS[u], CC[a] | higher or same | !C | GE | greater or equal | !(N ⊕ V) |
| LO[u], CS[u] | lower than | C | LT | less than | (N ⊕ V) |
| NE | not equal | !Z | GT | greater than | ![(N ⊕ V) + Z] |
| EQ | equal | Z | LE | less or equal | (N ⊕ V) + Z |

An Address register (16/32-bit, n=0-7)
Dn Data register (8/16/32-bit, n=0-7)
Rn any data or address register
s Source, d Destination
e Either source or destination
#n Immediate data, i Displacement
BCD Binary Coded Decimal
↑ Effective address

1 Long only; all others are byte only
2 Assembler calculates offset
3 Branch sizes: .B or .S -128 to +127 bytes, .W or .L -32768 to +32767 bytes
4 Assembler automatically uses A, I, Q or M form if possible. Use #n.L to prevent Quick optimization

SSP Supervisor Stack Pointer (32-bit)
USP User Stack Pointer (32-bit)
SP Active Stack Pointer (same as A7)
PC Program Counter (24-bit)

SR Status Register (16-bit)
CCR Condition Code Register (lower 8-bits of SR)
N negative, Z zero, V overflow, C carry, X extend
* set according to operation's result, = set directly
- not affected, 0 cleared, 1 set, U undefined

Revised by Peter Csaszar, Lawrence Tech University – 2004-2006



18