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Interface state density evaluation of high quality hetero-epitaxial 3C–SiC(0 0 1) for high-power MOSFET applications

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ABSTRACT

The effects of the crystal quality and surface morphology on the electrical properties of MOS capacitors have been studied in devices manufactured on 3C–SiC epitaxial layers grown on silicon (1 0 0) substrate. The interface state density, which represents one of the most important parameters, has been determined through capacitance measurements. A cross-correlation between high resolution X-ray diffraction, AFM analysis and electrical conductance measurements has allowed to determine the relationship between the crystalline quality and the interface state density. A decrease of the interface state density down to about 10^{11} cm^{-2} eV^{-1} was observed with improving the crystalline quality.

1. Introduction

Silicon carbide is a wide bandgap material, which has excellent properties for devices operating under extreme conditions, such as high temperature, high power, and high frequency [1–3]. SiC is a promising material for the device/sensor fabrication due to high critical electric field, high saturation electron velocity, good thermal conductivity as well as the higher bandgap energy (from 2.36 eV for 3C–SiC to 3.23 eV for 4H–SiC polytype) [4]. In power applications, SiC large bandgap translates into a high electrical breakdown field allowing device designs with lower series resistance and lower power dissipation [5]. SiC has the unique potential to be thermally oxidized to form a SiO_2 film. This provides the opportunity to develop metal oxide semiconductor (MOS) power devices [6].

In comparison to 4H–SiC, which is commonly adopted for the fabrication of power electronic devices, the use of cubic polytype (3C–SiC) has several advantages. The first one is a lower density of traps at the SiO_2/3C–SiC interface, the second is a higher channel electron mobility [7,8]. Indeed, despite lower breakdown field than 4H–SiC polytype (due to the lower bandgap), the inversion channel mobility observed in 3C–SiC lateral MOSFETs is more than one order of magnitude higher compared to 4H–SiC [9]. This can be explained by the near interface traps which, for 4H–SiC, are located in the bandgap close to the conduction band and limit the transport of electrons in the channel. The traps at the SiO_2/3C–SiC interface are instead located in the conduction band of 3C–SiC and therefore they have no effect on the transport properties of the channel [10,11]. Furthermore, it has also been shown that, unlike the 4H polytype, 3C–SiC is not affected by the expansion of single Shockley stacking faults during forward bias of p–n diodes [12], which can alter the stability on-state resistance of the devices and thus, reduce their reliability. They are also expected to be more cost effective due to the availability of large substrate sizes since the 3C–SiC material is grown on silicon wafers [13]. For all these reasons, 3C–SiC could be very suitable for applications such as medium power MOS field effect transistor (MOSFET) with blocking voltage up to 1500 V, p–n diodes for medium voltage (~1200 V) and high frequency devices. Considerable progress has been made in controlling the oxide/SiC interface in recent years, through optimized annealing and passivation experiments. In almost of these applications it is important to assess the interface state densities (D_{it}) at the oxide/SiC interface. For SiO_2/SiC (4H and 6H polytype) system the interface defect densities obtained to date are relatively high (>10^{11} cm^2 eV^{-1}) and it is believed that formation of carbon containing byproducts and/or suboxides at the interface could be the reason. Low value of D_{it} (about 10^{10} D_{it} cm^{-2} eV^{-1} has been reported in literature for 13 μm thick 3C–SiC(1 1 1) oriented film [15].

Although the possibility to grow the film hetero-epitaxially on Si wafers allows the use of large silicon substrates, reducing the

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manufacturing costs, the process optimization still represents a crucial issue.

The main blocking factors to the development of 3C–SiC devices on silicon are the large lattice mismatch, which is about 20% (a_{SiC} = 0.436 nm [4], a_{Si} = 0.543 nm [16]) and the different thermal expansion coefficients (about 8%) between the two dissimilar materials, which are blamed for the generation of defects as misfit dislocations and stacking faults at the interface.

It is known that the crystal quality (defect density) of the 3C–SiC films epitaxially grown on silicon may be improved by increasing the film thickness [17,18].

In this work the growth process has been optimized and the 3C–SiC/oxide interface has been studied as a function of thickness for relatively thin films, in the range 3–7 μm. The purpose of the work was to obtain low interface state density in high quality 3C–SiC films with reduced thickness, since this would significantly reduce the device fabrication costs.

2. Experimental

The epitaxial films were grown in a hot-wall chemical vapour deposition (CVD) reactor on 4-inches Si(0 0 1) oriented substrate. The entire deposition process constituted of four different steps (multistep process), as commonly adopted to reduce the defect density in the growing layer and to improve its crystalline quality [19]. After the introduction of the samples inside the reaction chamber and a first bake out of the chamber at 500 °C in vacuum (0.013 Pa), hydrogen (H_2 as gas carrier) and ethylene (C_2H_4 as carbon supply) were introduced into the reactor at a pressure of 10,000 Pa and the temperature increased to 1120 °C for the carbonization step. This process was optimized to reduce the formation of voids underneath the interface between 3C–SiC and Si due to the selective out diffusion of silicon from the substrate by a reaction of silicon with a suitable hydrocarbon gas. The carbonization process was completed by holding the temperature at 1120 °C for 5 min. After that, the temperature was then increased up to the growth temperature of 1350 °C. After the heating ramp, silane (SiH_4 as silicon supply) and HCl were introduced into the chamber and the growth was carried out with a Si/C ratio fixed at 1.4, Si/H_2 ratio at 0.02% and a growth rate of 3 μm/h. In addition, the presence of chlorine during the growth should suppress the homogeneous nucleation of silicon droplets in the gas phase [20]. After the growth, the precursor flows were stopped and the temperature was decreased to 200 °C in an Ar environment, thus avoiding the introduction of hydrogen to reduce the probability of any etch damage [21]. In order to study the influence of film thickness on the defect density and on the electrical properties of the material, four films with different thicknesses have been grown only by changing the growth time and leaving unchanged the other parameters. 3C–SiC film thickness values, measured with FT-IR (Fourier transform infra-red spectroscopy), were found constant along the entire wafer as: 2.9 ± 0.1 μm, 3.7 ± 0.1 μm, 5 ± 0.1 μm and 7.1 ± 0.1 μm.

For the SiO_2/SiC (4 and 6H polytype) system the interface defect densities obtained to date using thermal oxidation are relatively high and one limiting factor is considered to be a carbon containing by-product at the interface [22,23]. For this reason, in order to improve the oxide quality on the SiC substrate, several oxidation processes different from thermal growth of SiO_2 have been developed. In this work, an oxidation process usually adopted for 4H–SiC was employed: gate oxides were deposited by plasma-enhanced chemical vapour deposition (PE-CVD) of SiO_2 from SiH_4 and N_2O precursor gases at 300 °C for 45 s, followed by rapid thermal annealing (RTA) post-oxidation process at 950 °C for 2′ in O_2:N ambient under atmospheric pressure (nominal thickness 20 nm). The MOS structure was completed by DC sputtering of 500 nm Al film. Laser lithography/wet etching process were used for the MOS definition with an area of 0.04 mm^2. For comparison, the same process has been also used to manufacture MOS capacitors on n-type Si(0 0 1) with an average resistivity of 15 Ω cm.

The crystal structure was investigated by high resolution X-ray diffraction (Bruker AXS), using 2θ–ω scan and rocking curves (rc). The diffractometer is equipped with an Eulerian cradle using Cu–Kα source at a wavelength of 1.54 Å and operating at 40 kV and 40 mA. High-resolution optics, consisting of a two-bounced Ge022 monochromator and a very narrow variable slit system before the zero-dimensional detector, has been adopted in order to obtain accurate data about the structural information of the samples.

The surface morphology was studied by atomic force microscopy (AFM) using a Dimension 3100 AFM. The microscope was operating in contact mode and equipped with a single crystal silicon tip having a length of 125 μm, with a spring constant of 42 N/m, at a piezodrive frequency of 330 kHz. The scan size was 50 μm × 50 μm with the scan rate of 1.0 Hz. Measurements were performed in air at room temperature in the XYZ mode.

The capacitors have been characterized by high frequency CV measurements and AC conductance measurements using a HP 4284A precision LCR meter.

3. Results and discussion

To determine the relationship between defect density and surface morphology with the electrical properties of the studied 3C–SiC MOS structures, several methods have been applied (CV measurements, high-resolution X-ray diffraction, atomic force microscopy analysis).

3.1. Electrical measurements

The interface trap density has been determined from CV measurements at 1 MHz, using the Terman method and from the AC conductance measured in the range from 50 kHz to 1 MHz. Fig. 1 shows the normalized capacitance (C/C_{OX}) versus voltage (V) measured at 1 MHz for the MOS capacitors on 3 μm, 7 μm thick 3C–SiC films and silicon (as reference), respectively. From the C–V curves the dielectric thickness (t_{OX}), the dopant concentration (N_D) and the Fermi potential (Φ_F) have been extracted [24]. The results of the extraction are shown in Table 1.

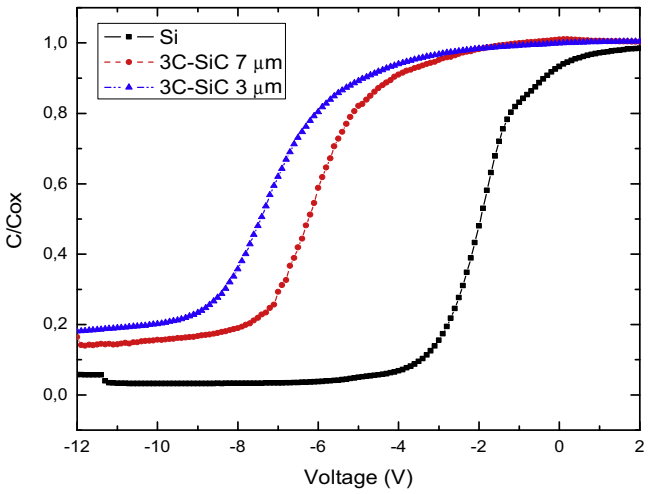

Fig. 1. Normalized capacitance (C/C_{OX}) as a function of voltage, for silicon (squares), 7 μm and 3 μm thick hetero-epitaxial 3C–SiC films (circles and triangles respectively).

Table 1
Electric properties of 3C–SiC MOS capacitor.

Sample	ΔV_{FB} [V]	Q_{eff} [C/cm^2]	T_{OX} [nm]	D_{it} [cm^2 eV^{-1}]	N_D [at/cm^3]	Φ_F [eV]
SiC 3 μm	−7 ± 1.2	7.0×10^{12}	21 ± 2	4×10^{13}–2×10^{14}	2.9×10^{16}	1.04
SiC 5 μm	−5.2 ± 1.0	6.3×10^{12}	18 ± 2	~10^{11}	3.0×10^{16}	1.03
SiC 7 μm	−4.5 ± 0.7	5.7×10^{12}	22 ± 2	4×10^{10}–2×10^{13}	2.6×10^{16}	1.03
Silicon	−2.7 ± 0.4	4.0×10^{12}	21 ± 2	~3×10^{9}	6.0×10^{14}	0.28

The dielectric thickness t_{OX} can be determined from the capacitance–voltage characteristics taking into account the maximum capacitance (C_{OX}) for the accumulation state of the structure [25]:

$$t_{OX} = \frac{\varepsilon_{OX}\varepsilon_0}{C_{OX}} A \tag{1}$$

where A is the device area (cm^2), C_{OX} is the capacitance for the accumulation state, ε_{OX} and ε_0 are the relative electrical permittivity of the dielectric and vacuum permittivity, respectively.

Transforming the measured capacitance (C) characteristic into $1/C^2$ plot, the slope of the linear range was used to calculate the doping concentration N_D from the following formula [25]:

$$N_D = \frac{2}{q\varepsilon_S\varepsilon_0 |\text{slope}| A^2} \tag{2}$$

where q is the electron charge and ε_S is the relative electrical permittivity of the semiconductor. From the N_D value, the Fermi potential (Φ_F) can be calculated as follow [25]:

$$\Phi_F = -\frac{kT}{q} \ln\left(\frac{N_D}{n_i}\right) \tag{3}$$

where k is the Boltzmann constant, T is the temperature, n_i is the intrinsic concentration in the substrate given by the following formula:

$$n_i = \sqrt{N_C N_V} \exp\left(-\frac{E_G}{2kT}\right) \tag{4}$$

where E_G is the energy bandgap, N_C and N_V are the effective density of states in the conduction and valence bands, respectively. For 3C–SiC $N_C = 1.353 \times 10^{19}$ and $N_V = 1.063 \times 10^{19}$ cm^{-3} [26].

In an ideal MOS capacitor, knowing the doping concentration N_D, the semiconductor electron affinity χ and the metal work function φ ($\chi_{3C\text{–}SiC} = 3.8$ eV and $\varphi_{Al} = 4.1$ eV), the ideal flat-band semiconductor voltage (V_{FB}) can be calculated [25].

The total capacitance at the flat-band (C_{FB}) condition is a series combination of the oxide capacitance (C_{OX}) and the semiconductor depletion-layer capacitance (C_S):

$$C_{FB} = \frac{C_{OX} C_S}{C_{OX} + C_S} \tag{5}$$

where C_S can be written as:

$$C_S = \frac{\varepsilon_S}{L_D} \tag{6}$$

being ε_S the permittivity of the semiconductor and L_D the Debye length. L_D can be expressed as:

$$L_D = \sqrt{\frac{kT\varepsilon_S}{N_D q^2}} \tag{7}$$

where N_D is the doping concentration of the semiconductor. The total capacitance at the flat-band condition, for a p-doped semiconductor is given by:

$$C_{FB} = \frac{\varepsilon_{OX}\varepsilon_S}{\varepsilon_S t_{OX} + \varepsilon_{OX} L_D} = \frac{\varepsilon_{OX}\varepsilon_S}{\varepsilon_S t_{OX} + \varepsilon_{OX}\sqrt{kT\varepsilon_S/N_D q^2}} \tag{8}$$

Then, the V_{FB} voltage is obtained from the measured capacitance by finding the bias (V) value corresponding to the calculated C_{FB}.

In Table 1 the shift between the ideal and experimental value of V_{FB} has been reported for silicon reference, 7 μm-SiC, 5 μm-SiC and 3 μm-SiC. The shift ΔV_{FB} in respect to the ideal value is due to the presence of fixed and/or trapped charge in the oxide and interface trapped charge, due to the presence of interface states of density D_{it}, located at the semiconductor/oxide interface [25].

From the data shown in Table 1, the lowest flat-band voltage is obtained for silicon and corresponds to an effective oxide charge density of 4×10^{12}/cm^2. The effective charge density has been calculated from the flatband voltage shift ΔV_{FB} as $C_{OX} \sim \Delta V_{FB}/q$ and includes both the fixed and the oxide trapped charge. The measured value is very high compared to typical gate oxide values, of less than 10^{11}/cm^2, but this is due to the fabrication process, i.e. oxide deposition at low temperature (300 °C) and then annealing at 950 °C [27]. The well-known *Deal triangle* shows that the fixed oxide charge can be reduced by annealing at higher temperature [28].

The AC conductance method is commonly accepted as the most accurate method for the determination of the interface trap density [29]. It requires the comparison of several parallel conductance (G_p) curves at a given gate bias over a range of frequencies (ω). The conductance of the interface-trap branch is given by:

$$\frac{G_P}{\omega} = \frac{C_{it}\tau_{it}\omega R_{it}}{1 + \omega^2 \tau_{it}^2} \tag{9}$$

where C_{it} and R_{it} are the capacitance and resistance associated with the interface traps and, thus, are also functions of energy. The product $C_{it}R_{it}$, is defined as the interface-trap lifetime τ_{it} which determines the frequency behavior of the interface traps.

Fig. 2a and b shows G_P/ω as a function of omega (ω) measured at different voltages in the samples with the thickness of 7 μm and 3 μm, respectively. In general, the G_p/ω curves versus ω are quite broad. This is generally attributed to the dispersion of trap time constant caused by surface potential fluctuations due to non-uniformities in oxide charge and interface traps. However, for voltages above −4 V, the superimposition between the effect of traps continuously distributed in energy and the presence of an interface trap with a single energy level in the bandgap is observed, as indicated by a sharp peak. In the case of 3 μm thick films (Fig. 2b), sharp peaks have been observed for all the measured voltages. We also observe in both the samples some noise at low frequency values. This is in general related to slow states, which may increase the conductance on the low frequency side [30]. Therefore, the contribution of slow interface states cannot be excluded. From the peak of G_p/ω curve the density of interface traps can be evaluated as $D_{it} = 2.5/q\,(G_p/\omega)_{max}$.

Fig. 3 shows the D_{it} values obtained as a function of interface trap energy $E_c - E_t = Eg/2 + q\Phi_F - q\Phi_S$ (being E_t the trap energy, E_c the conduction band and Φ_S the surface potential, obtained from the high frequency C–V curve [31]). In Fig. 3 open and full symbols refer to data obtained by employing the Terman method or AC conductance, respectively [25]. In order to make the graph more readable, the 5 μm-SiC sample was not shown because the trend is close the 7 μm-SiC sample.

According to Fig. 2, the defect density determined from conductance in the case of 3 μm is around 10^{14} cm^{-2} eV^{-1}, while lower

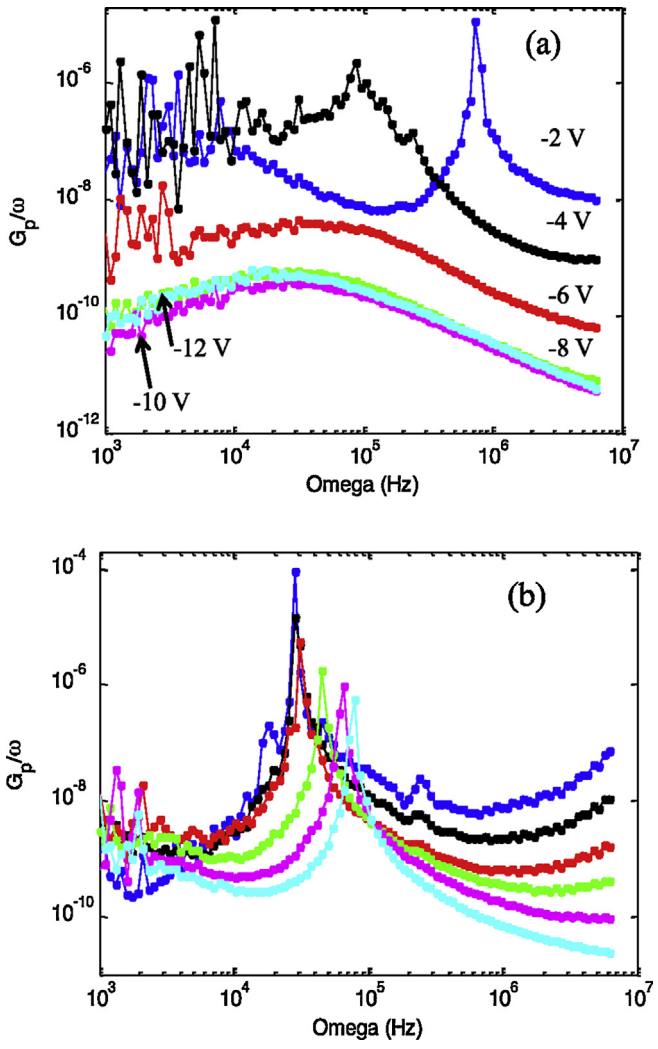

Fig. 2. G_p/ω as a function of frequency measured at different voltage for a MOS on a (a) 7 μm thick and 3 μm thick (b) 3C–SiC layer. (b) The voltage used is the same of (a).

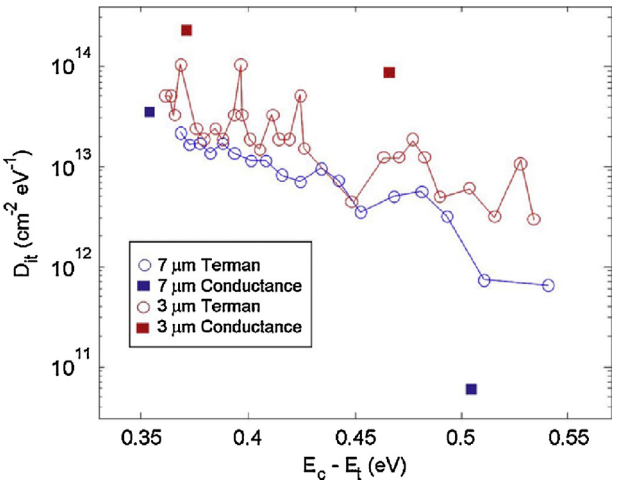

Fig. 3. Interface state density obtained from conductance measurements (full symbols) and high frequency *C–V* (open symbols), as a function of trap energy.

values are obtained for thicker films, in which no high contribution of single energy trap levels has been observed (see Fig. 2).

The minimum value of the measured interface trap density is $\approx 7 \times 10^{12}$ and $\approx 5 \times 10^{11}$ cm^{-2} eV^{-1} for 3 and 7 μm thick films, respectively. D_{it} values obtained using the two methods have been reported in Table 1.

Interface trap density of about 10^{10} D_{it} cm^{-2} eV^{-1} has been previously reported in literature for 3C–SiC(1 1 1) oriented and 13-μm thick [32]. Probably due to lower surface dandling bounds (one and two dandling bonds per atom, respectively, for (1 1 1) and (0 0 1) surfaces) [33] that lead to a different semiconductor/oxide interface. Despite the increased stress of the epi-layer grown on Si(0 0 1), compared to the growth on Si(1 1 1) or 6H–SiC(0 0 1) substrate [34], the 3C–SiC(0 0 1)-oriented studied in this paper shows the almost the same electrical properties of the 3C–SiC(1 1 1), but with a lower film thickness, i.e. a significantly saving of gas precursor during the growth process. Indeed, in the case of 4H–SiC, D_{it} is frequently high (>10^{11} cm^2 eV^{-1}) [35,36]. This is attributed to the presence of carbon rich clusters at the SiC/SiO_2 interfaces which creates states inside the bandgap, located close to the conduction band. In the case of 3C–SiC, the carbon clusters states are located inside the conduction band so that they do not contribute to the D_{it}. This is a clear

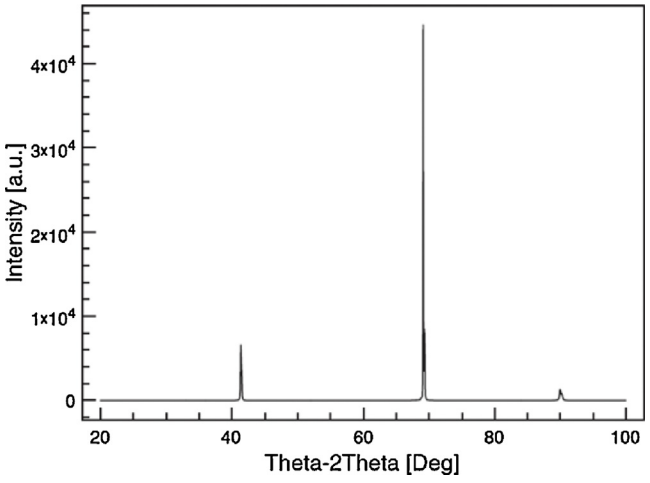

Fig. 4. X-ray diffraction θ–2θ line scan of the 3C–SiC film on silicon substrate. It is possible to observe the peak related to the (2 0 0) and (4 0 0) 3C–SiC planes ($2\theta = 41.3°$ and 90.1 respectively) and the (2 0 0) Si plane ($2\theta = 69.1°$).

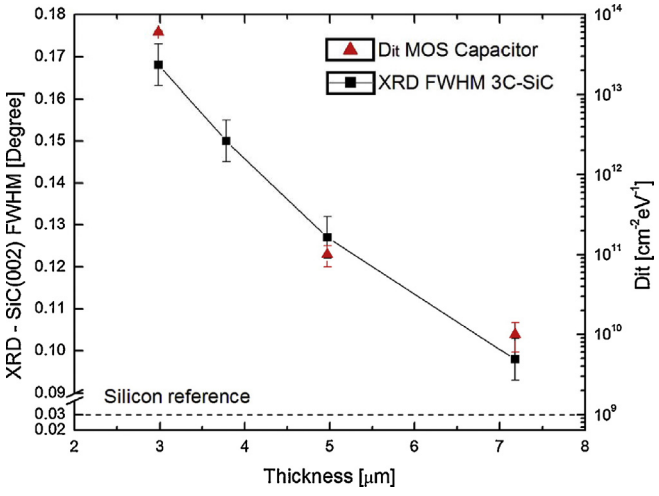

Fig. 5. X-ray diffraction rocking curve FWHM of 3C–SiC(0 0 2) peak as a function of film thickness (squares) and FWHM of Si(0 0 4) peak as reference. Interface states density D_{it}, as a function of the film thickness (triangles).

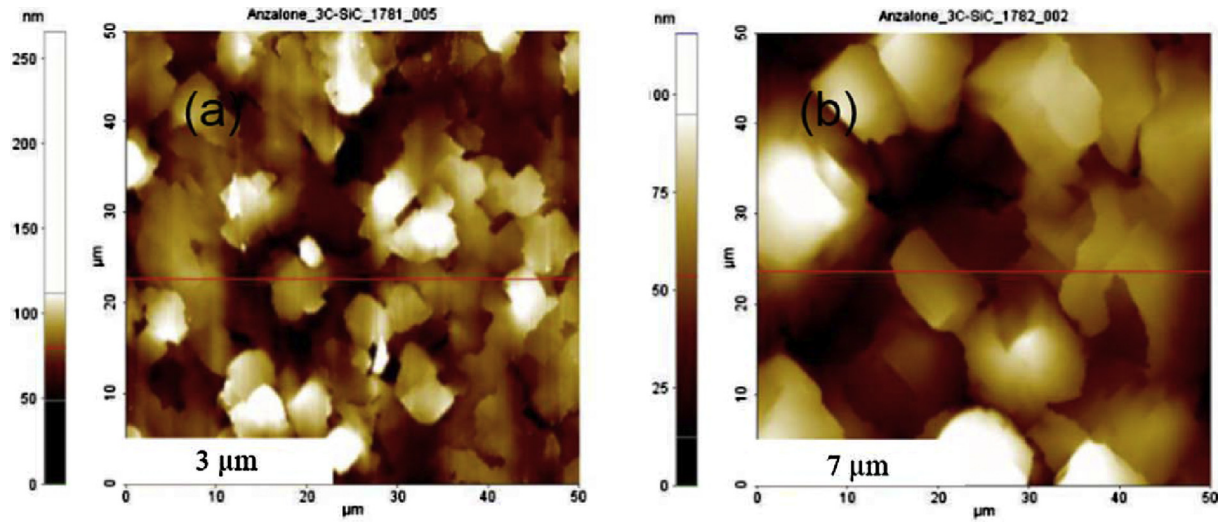

Fig. 6. Atomic force microscopy image of the 3C–SiC film. Different surface morphology has been observed for 3 μm thick (a) and 7 μm thick (b) 3C–SiC film.

advantage of 3C polytype ([0 0 1] over [1 1 1] orientation) over 4H, since it significantly simplifies the oxidation recipe.

3.2. Structural and surface characterization

Prior to oxidation and contact definition steps, XRD measurements were performed, using a symmetric configuration (i.e. using the incident angle equals to the exit angle), through a θ–2θ scan. A typical diffraction pattern related to the 3C–SiC(0 0 1) orientation was observed, as shown in Fig. 4. In the diffractogram, in addition to the (0 0 2) silicon peak ($2\theta = 69.1^\circ$) only the SiC(0 0 2) peak ($2\theta = 41.3^\circ$) and the second-order SiC(0 0 4) peaks ($2\theta = 90.1^\circ$), corresponding to the [0 0 1] orientation, were detected, therefore indicating a good epitaxial relationship.

The full width of half maximum (FWHM) of the rocking curve (via X-ray ω-scan) of the 3C–SiC(0 0 2) peak and 3C–SiC(0 0 4) peak as a function of film thickness is shown in Fig. 5. The 1/FWHM is related to the crystal quality and defect density (mainly stacking faults) [37].

As previously observed and reported in literature [17] the crystalline quality of the 3C–SiC film depends on the film thickness and improves as the film thickness increases (FWHM decrease). Fig. 5 also reports on the right axis the measured interface defect density D_{it} (minimum value) as a function of thickness. The MOS interface state density seems to be dependent on the crystalline quality of the 3C–SiC material.

The AFM scan shows different surface morphology for 3 μm thick (Fig. 6a) and 7 μm thick (Fig. 6b) 3C–SiC film. The regions detected in the AFM images can be associated to planar defects, such as stacking faults and twins, as well as anti-phase boundaries. The images show that the size of free-defects domains increases by increasing the film thickness [17]: Fig. 6a shows a surface full of domains with a size of about 5 nm while, increasing the film thickness (Fig. 6b) larger domains are observed (around 10 nm).

On the base of the structural characterization the D_{it} appears to be affected by both the crystalline quality (evaluated by the rocking curve) and by the size of anti-phase domains.

4. Conclusion

In conclusion, the effect of the film thickness, crystal quality and surface morphology on the electrical properties of the 3C–SiC MOS capacitor was studied. X-ray FWHM of the 3C–SiC(0 0 2) peak and AFM measurement showed an increase of film quality by increasing the film thickness. The *C–V* and conductance measurements showed a decrease of the interface state density (D_{it}) as a function of film thickness, evidencing the existence of a strong relationship between the defect density and electrical properties has been shown. In details, increasing the crystal quality a decrease of the interface state density (down to 10^{10} D_{it} cm^{-2} eV^{-1}) was observed.

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