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Production of large-area single-crystal wafers of cubic SiC for semiconductor devices

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A reproducible process is described for growing a thick single-crystal layer of cubic SiC on a single-crystal Si wafer by chemical vapor deposition. A buffer layer, grown *in situ*, is used between the cubic SiC and the Si substrate to minimize the effect of lattice mismatch. Layers of up to 34 μm thick and several cm^2 in area have been grown. Wafers are obtained by chemically removing the Si substrates from the grown layers. Excellent electron channeling patterns produced by these wafers indicate very good crystal quality. Preliminary electrical measurements have yielded electron mobilities up to 380 cm^2/Vs.

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Recently there has been an increased effort to develop high-temperature electronic devices for advanced turbine engines, geothermal wells, and other applications.[1] For many years, SiC has been a prime candidate for use as a high-temperature electronic material because of its large band gap, good carrier mobility, and excellent physical stability.[2] But its development has been hampered by the lack of a reproducible process for producing the single-crystal substrates necessary for device fabrication. This letter reports significant progress in the search for such a process. Basically, the approach consists of growing a single-crystal layer of cubic SiC on a single-crystal Si wafer by chemical vapor deposition (CVD). This has been tried many times previously,[3–7] but the results have never been satisfactory, largely because of the 20% lattice mismatch between SiC and Si ($a_{SiC} = 0.436$ nm, $a_{Si} = 0.543$ nm).

The first author and his colleagues at Kyoto University recently achieved single-crystal growth up to 4 μm thick on Si wafers.[8] In this work, an intermediate buffer layer was used between the cubic SiC and the Si wafer. The buffer layer was sputtered SiC. This approach was extended further[9,10] by growing the buffer layer *in situ* in the CVD system. Layers up to 20 μm thick were grown but the extent of single-crystal growth was limited to a small area.

This letter describes recent work at the Lewis Research Center where the buffer layer approach has been improved such that the process is reproducible and yields single-crystal layers that are thicker, larger in area, and of higher quality than has been reported for any previous process.

The CVD system is of conventional design with special attention to system cleanliness and reproducibility of growth conditions. Deposition takes place at atmospheric pressure. The sources of silicon and carbon are SiH_4 (3% in H_2) and C_3H_8 (0.3% in H_2), respectively. Hydrogen, purified by passage through a palladium diffusion cell, is the carrier gas. Hydrogen chloride is used as an etching gas. Diborane (100 ppm in H_2) and phosphine (100 ppm in H_2) are included as doping gases. In order to minimize contamination and enhance reproducibility from run to run, the CVD system features pneumatically operated bellows-seal valves and electronic mass flow controllers for all six gases. All valves and flow controllers are operated remotely from a single control panel.

The reaction tube is a horizontal water-cooled quartz tube with an inside diameter of 50 mm. The Si substrate is placed on an rf-heated, rectangular, graphite susceptor that is 60 mm long by 30 mm wide by 10 mm thick. The susceptor is supported by a quartz boat tapered on the upstream end. This tapered shape provides for smooth flow over the susceptor. The temperature of the susceptor is measured with an automatic optical pyrometer. The pyrometer sights through a window in an end cap at the downstream end of the reaction tube and into a 35-mm-deep hole in the end of the susceptor. All substrate temperatures in this letter are actually susceptor temperatures that were measured in this manner and then corrected for items in the optical path. A temperature calibration check is the observation that a Si wafer (m.p. 1420 °C) on the susceptor begins to melt at a corrected temperature of 1425 °C. The pyrometer also provides a signal for a temperature control system that maintains the susceptor temperature constant to within 2 °C during a run.

A rotary vacuum pump with a molecular sieve trap is used to evacuate the reaction tube. During a run the effluents from the reaction tube are passed through a water scrubber before entering the hood ventilation system. Between runs all tubing and other flow components, starting with the regulator cross-purge assemblies, are continually purged. The purging gas is high-purity Ar that is passed through a commercial inert gas purifier.

Before being used with a Si substrate, each susceptor is first etched with HCl and then coated with SiC. This etching/coating is done under the conditions described in steps (1) and (3) below. The Si substrates are prepared from commercially available polished (100) Si wafers, 76 mm in diameter by 0.375 mm thick. Rectangular substrates, 50 × 22 mm, are cut from these wafers and used with no further preparation.

The buffer layer method for growing a SiC layer on a Si substrate consists of three distinct steps. During each of the steps the H_2 carrier gas flow is maintained at 3 l/min and the desired process gases are added. The concentration of each

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gas constituent is given as a mole % of the total flow of H_2. The steps are as follows:

Step (1) *Etching*. In order to prepare the Si substrate surface for subsequent growth, it is etched by heating to 1200 °C in a mixture of 4.0 mole % HCl and H_2 for 10 min. The HCl flow is then shut off and the susceptor returned to near room temperature.

Step (2) *Buffer layer growth*. This step provides the buffer layer necessary to obtain good SiC crystal growth on the Si substrate. A flow of 0.03 mole % C_3H_8 in the H_2 is established with the susceptor at room temperature. The susceptor temperature is then raised to 1400 °C in less than a minute and held at this temperature for about a minute. Then the C_3H_8 flow and rf power are shut off and the susceptor allowed to cool to near room temperature.

Step (3) *Crystal growth*. The susceptor and Si wafer are again heated to 1400 °C. After waiting one minute for temperature equilibration, a concentration of 0.04 mole % silane and 0.02 mole % propane (Si/C ratio of 0.7) is established in the H_2 flow. Under these conditions, a cubic SiC single-crystal layer can be grown on the buffer layer. When the desired growth time has been achieved, the silane and propane flows are shut off, the reaction tube allowed to flush with H_2, and then the susceptor temperature is returned to room temperature.

The buffer layer grown in the manner of step (2) was determined to be about 20 nm thick by ellipsometry. The exact nature and role of this layer are not fully understood at present. Silicon has been observed[5,7] to be chemically converted to polycrystalline cubic SiC when heated to about 1200 °C in the presence of H_2 and a hydrocarbon. So, it is probable that the buffer layer is mostly polycrystalline cubic SiC.

The porosity of the graphite susceptors and the SiC coating on the susceptors play a role in the growth rate and the quality of the SiC layers grown on the Si substrates. With no SiC coating on the graphite, the grown layers tend to be rough and polycrystalline, especially around the edges of the Si substrate. The susceptor coating process usually lasted about two hours, but this was not sufficient to produce a gas-tight coating. In early growth runs, the graphite used to make the susceptors was noticeably more porous than the dense high-purity graphite of later runs. In all runs a similar coating process was used for the susceptor and similar conditions were used to grow the SiC layer on the Si substrate. However, the use of porous susceptors yielded layers about 28 μm thick in a 6-h run, while the use of denser susceptors yielded layers about 15 μm thick for the same deposition time. The SiC coating on even the denser graphite susceptors did not appear to be uniform and certainly was not completely gas tight. The use of commercial SiC-coated susceptors would probably improve the crystal growth process even further.

The temperature in the reaction tube upstream of the susceptor was found to be an important factor in achieving high-quality single-crystal growth. If the hot susceptor heats the quartz boat sufficiently (to greater than 600 °C), deposition can occur on the boat. This apparently can change the composition of the gas sufficiently to adversely affect the deposition achieved on the Si wafer. The result is various bands of obviously different kinds of growth (some nonstoichiometric) occurring on the Si substrate. Although some single-crystal growth takes place, the surface is generally rough. The greater the amount of deposition upstream of the susceptor, the greater is this effect.

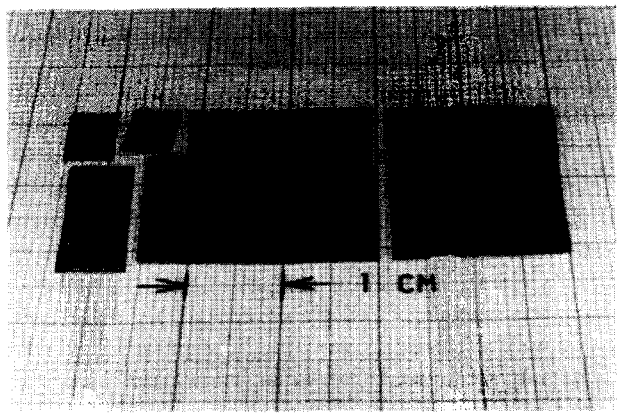

FIG. 1. 16-μm-thick cubic SiC single-crystal wafer (broken into five pieces).

When care was taken to avoid the detrimental conditions described above, the process consistently yielded high-quality single-crystal cubic SiC layers that are uniform over the whole substrate. Typical growth rates were about 2.5 μm/h. The Si substrate can be removed by etching in an HF-HNO_3 solution, leaving a thin cubic SiC wafer. Thinner wafers tend to curl, but wafers thicker than about 15 μm remain flat when removed from the substrate. An example is shown in Fig. 1 where the wafer has broken into several pieces. The wafers are transparent and yellow (the color of intrinsic cubic SiC). Since they are thin (up to 34 μm so far), they are fragile and will crack if not handled carefully. The crystals nearly always break in rectangular pieces. This is to be expected since they are grown on (100) Si.

X-ray diffraction measurements and Laue photographs have verified that the crystals are cubic SiC single crystals with a (100) orientation. There was no indication that any of the other SiC polytypes were present. The Laue photographs

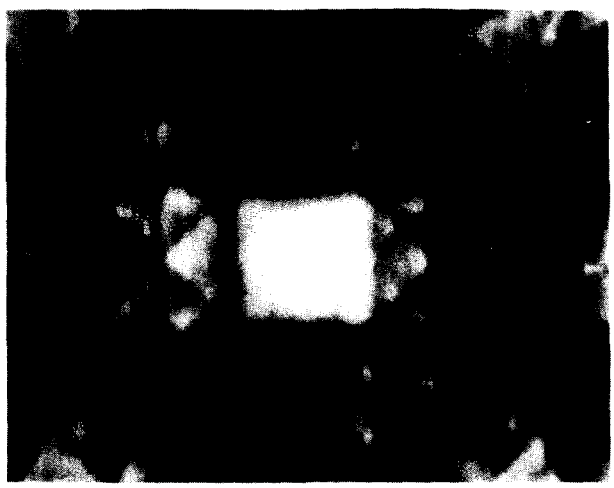

FIG. 2. Electron channeling pattern of a 20-μm-thick cubic SiC single crystal.

have also shown that the ⟨100⟩ directions of the cubic SiC layer and the Si substrate are parallel.

Additional evidence of the high quality of the cubic SiC crystals obtained by the above process is shown in Fig. 2. This is an electron channeling pattern[11] obtained for a 20-μm-thick cubic SiC crystal that had been removed from the Si substrate. The good contrast and sharpness of the pattern indicate very good crystal quality. It was found that although excellent channeling patterns could be obtained from the top surface of the grown crystal, no discernible pattern could be obtained from the bottom surface. Probably, the polycrystalline buffer layer is included in the bottom surface.

Preliminary Hall measurements were made at room temperature on some undoped and boron-doped wafers using the van der Pauw technique.[12] Since N_2 produces donor atoms in SiC, the undoped wafers were *n* type as expected. The boron-doped wafers were *p* type and probably heavily compensated. Four undoped samples, 28 μm thick and from the same run, yielded values of 0.29–0.41 Ω cm for resistivity, 250–380 cm^2/V for the electron mobility, and 3.9×10^{16}–7.4×10^{16} cm^{-3} for the electron carrier concentration. Five boron-doped samples, 18 μm thick and from the same run, yielded values of 190–670 Ω cm for the resistivity, 15–21 cm^2/V for the hole mobility, and 5.6×10^{14}–1.6×10^{15} cm^{-3} for the hole carrier concentration.

In summary, this letter has described improvements in the buffer layer method of growing cubic SiC on Si. The essential improvements are as follows. The CVD system was designed to be extremely clean and to provide for precise flow and temperature control. A procedure was used whereby the complete gas handling system is continually purged with high-purity Ar between growth runs. A Si/C ratio of less than 1 was used. And, finally, the quartz support for the graphite susceptor was designed to minimize premature deposition on the support upstream of the susceptor.

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