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Fabrication and Characterization of 3C-SiC-Based MOSFETs

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In this article, the electrical properties of 3C-SiC are described and its potential for metal-oxide semiconductor field-effect transistors (MOSFETs) is demonstrated. The density of traps, D_{IT}, at the interface of 3C-SiC/SiO_2 capacitors is determined by the conductance method subsequent to various processing steps; the origin of the interface traps is discussed. Lateral and vertical 3C-SiC MOSFET devices of varying cell and device size are designed with hexagonal and squared cell geometry, and are fabricated side by side with MOS Hall bar structures. The electrical parameters of the MOSFETs are determined, and the free electron areal density and Hall mobility are measured in the channel of the MOS Hall bar structures. Based on the charge-sheet model, D_{IT} is also obtained from the Hall investigations.

Keywords: 3C-SiC, Channel mobility, Hall effect, Interface traps, MOSFETs

1. Introduction

Cubic silicon carbide (3C-SiC) has the advantage that it can be heteroepitaxially grown on silicon (Si) using CVD.[1] With this deposition technique, 3C-SiC wafers with large diameters can be achieved at low cost. The physical properties of 3C-SiC are superior for power electronic devices in the medium to high voltage range (up to approximately 1 kV). More especially, MOSFETs benefit from these superior properties.

Compared to the 4H- and 6H-SiC polytype, the band gap of 3C-SiC is narrower ($\Delta E_{gap} = 2.3$ eV, at room temperature), which results in two advantages. Firstly, it requires smaller electric field strengths to achieve inversion and secondly the density of traps, D_{IT}, at the interface of 3C-SiC/SiO_2 is much lower than in the case of 4H-SiC MOS structures. D_{IT} of MOS capacitors based on silicon and on three different SiC polytypes, respectively, is schematically shown in Figure 1. In Si/SiO_2 structures, D_{IT} is only composed of dangling bonds, which can partially be terminated by hydrogen (hatched area). In SiC/SiO_2 capacitors, in addition carbon clusters (grey area) and acceptor-like near interface traps (NITs, black triangle), which are located in the oxide close to the SiC/SiO_2 interface, contribute to D_{IT}.[2] Due to the fact that the upper valence band edges of different SiC polytypes (E_V(SiC)) are energetically aligned,[3] the energy positions of the lower SiC conduction band edges (E_C(SiC)) scale with the corresponding band gaps, as is indicated on the *x*-axis in Figure 1. Further, results of internal photoemission of electrons (IPE) provide an energy spacing of approximately 6 eV between the lower conduction band edge of SiO_2 ($E_C(SiO_2)$) and E_V(SiC), whilst photon-stimulated electron tunneling (PST) investigations reveal that the ground state level of NITs is separated from $E_C(SiO_2)$ by 2.77 eV.[3,4] Consequently, the large density of NITs is located high in the conduction band of Si and of 3C-SiC, where these acceptor-like states cannot be filled with electrons and cannot, therefore, deteriorate the current in the channel of corresponding MOSFETs. This means that the free electron concentration and electron

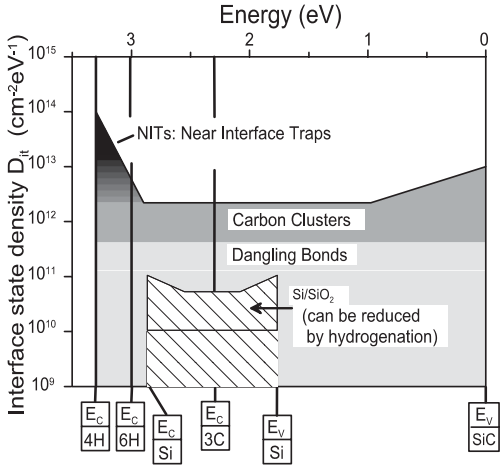

Fig. 1. Scheme of the composition and distribution of the interface state density, D_{IT}, as observed in Si, 3C-SiC, 6H-SiC, and 4H-SiC MOS capacitors. In Si-based MOS capacitors, D_{IT} is only dominated by dangling bonds, while in SiC-based MOS capacitors, it is composed of dangling bonds, carbon clusters, and near interface traps (NITs).

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mobility in the channel of 3C-SiC inversion MOSFETs are not affected by NITs. Moreover, the electron Hall mobility in the bulk of 3C-SiC is isotropic and assumes a value of about 800 $cm^2\ V^{-1}\ s^{-1}$ at room temperature,[5] which is comparable to the values determined in 4H-SiC.[6]

Neudeck et al.[7] measured the breakdown field in 3C-SiC p-n junction diodes doped at concentrations between 10^{16} cm^{-3} and 10^{18} cm^{-3}, and obtained values ranging from 1 MV cm^{-1} to 2.5 MV cm^{-1}, which constitute the upper limit for high voltage applications.

In the present paper, we report on the fabrication and characterization of 3C-SiC MOS devices. The interface state density, D_{IT}, in n- and p-type 3C-SiC capacitors prepared by various processing steps was measured with the conductance technique. Further several types of MOSFET devices with varying size were fabricated side by side with Hall bar MOSFET structures on 3C-SiC epilayers. The device parameters were determined and Hall effect investigations were conducted in the channel of the Hall bar MOSFETs.

2. Traps at the Interface of 3C-SiC/SiO_2 Structures

Freestanding, 200 μm thick, n-type 3C-SiC wafers grown on undulating Si (001) by HAST[1] were used for a systematic investigation of D_{IT} (see Table 1). On samples #3 to #6, n- and/or p-type epilayers were deposited at 1600 °C using CVD.[8] Nitrogen and trimethylaluminum were employed to adjust the donor and acceptor concentration, respectively, to values ~10^{16} cm^{-3}. Prior to the oxidation, samples #1 to #6 were subjected to a standard RCA clean and part of the samples (see Table 1) was exposed to UV light ($hN \leq 10$ eV) for about 12 h, in order to oxidize residual carbon at the sample surface by the nascent ozone.[9] The gate oxide of samples #1 to #5 was grown in nominally dry oxygen at 1120 °C for 1 h followed by a post-oxidation anneal at the same temperature; the oxide thickness was 70 nm. Samples #6/n and #6/p were grown in 100 % NO at 1175 °C for 4 h resulting in an oxide thickness of 20 nm.[10] Sample #5/n was additionally annealed in ambient hydrogen at 800 °C for 30 min. The density of interface traps was monitored by the AC conductance method using probe frequencies from 1 kHz to 1 MHz, and varying the temperature from 100 K to 500 K; the sweep rate was 0.2 V s^{-1}.

Table 1. Processing steps applied to the investigated 3C-SiC MOS capacitors.

3C-SiC sample no.	Conductivity type	Processing			
		Additional 3C-SiC epilayer	Ozone pre-clean	Oxidation	H_2 anneal (800 °C)
#1	n	no	no	dry O_2	no
#2	n	no	yes	dry O_2	no
#3	n/p	yes	no	dry O_2	no
#4	n/p	yes	yes	dry O_2	no
#5	n	yes	yes	dry O_2	yes
#6	n/p	yes	yes	NO-oxide	no

In Figure 2a and b, the *C–V* and *G–V* characteristics of two n-type MOS capacitors (#1/n and #6/n) are compared, demonstrating that suitable processing can greatly improve the interface properties. The MOS capacitor fabricated just on the 3C-SiC substrate with the gate oxide grown under ambient O_2 (solid curve, sample #1/n) shows a large shift of the flat-band voltage ($V_{FL} = -6.5$ V) caused by a positive fixed charge ($Q_{FC} = 4.6 \times 10^{12}$ e cm^{-2}) and a huge conductance peak caused by a high density of interface traps. The positive charge may be located either at the interface or in the oxide. Both the shift of the flat band voltage ($V_{FL} = -2.8$ V) and the height of the conductance peak are distinctly reduced in capacitor #6/n (dashed curves), which is fabricated on an additional epilayer and exposed to a UV-ozone surface clean; the oxide is grown in ambient NO.

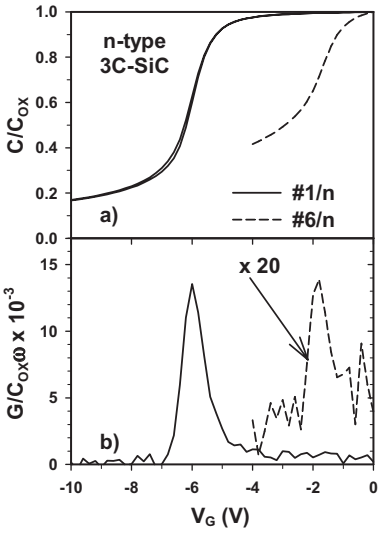

Fig. 2. a) Capacitance and b) conductance characteristics of MOS capacitors #1/n (solid curves) and #6/n (dashed curves) taken at 100 K with a probe frequency of 1 kHz.

The processing-dependent D_{IT} values are summarized in Figure 3a and b. In n-type MOS capacitors (see Fig. 3a), the conducted additional processing steps – with the exception of the anneal under hydrogen (see Table 1) – lead in general to a reduction of D_{IT}. It turns out especially that the process applied to MOS capacitor #6/n is extremely effective; it reduces D_{IT} close to the conduction band edge by one order of magnitude ($D_{IT} = 10^{11}$ cm^{-2} eV^{-1}). The anneal under hydrogen at 800 °C for 30 min results in a slight increase of D_{IT} in the upper part of the band gap (compare samples #4/n and #5/n). The interface states under investigation are apparently related to stable atomic configurations but not to dangling bonds typical of Si/SiO_2 interfaces. We suggest that the origin of these defects is related to chemically stable carbon clusters. Comparing samples

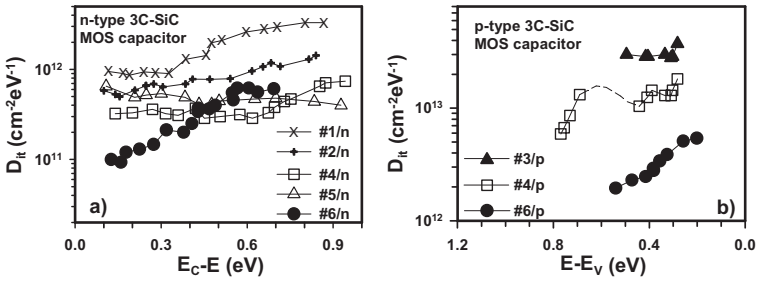

Fig. 3. Interface state density, D_{IT}, as a function of energy for differently processed a) n-type and b) p-type 3C-SiC MOS structures.

#4/n and #6/n, it turns out that the NO oxidation process is more effective in reducing D_{IT} close to the conduction band edge than the pure O_2 oxidation.

Similar observations are made for p-type 3C-SiC MOS capacitors (see Fig. 3b). Because of the lack of p-type substrates, the reference capacitor (sample #3/p, triangles) is composed of an n-type 3C-SiC substrate with an additional p-type 3C-SiC epilayer on top. A pre-clean using ozone (sample #4/p, open squares), as well as oxidation in ambient NO (sample #6/p, filled circles), reduce D_{IT}; however, the D_{IT} values determined close to the valence band edge are about one order of magnitude higher than in the upper half of the bandgap.

We have demonstrated that oxidation in ambient NO reduces D_{IT} in the entire bandgap of 3C-SiC. We assume that nitrogen either breaks π-bonded carbon clusters (resulting in smaller cluster sizes) which leads to a redistribution of D_{IT}, or terminates directly dangling bonds of carbon atoms.

3. Fabrication of 3C-SiC MOSFET Devices

Lateral and vertical MOSFET devices with varying size from a single unit cell (about 40 μm × 40 μm, depending on the channel length and design) to 3 mm × 3 mm containing several thousend unit cells were fabricated on 2″ 3C-SiC (001) substrates manufactured by HAST.[1] Figure 4 shows the cross sections and optical microscopy images of the different processed MOSFET types. For vertical MOSFET devices, unit cells with hexagonal or squared cell geometry were designed. The lateral MOSFET devices contain 220 and 1980 unit cells for 1 mm × 1 mm and 3 mm × 3 mm devices, respectively. The vertical MOSFET devices contain up to 976 and 12000 hexagonal, and up to 660 and 8000 square unit cells for 1 mm × 1 mm and 3 mm × 3 mm devices, respectively. Besides the varyiously sized MOSFET devices the wafer layout included, among other test structures, MOS-controlled Hall effect structures. The MOS-controlled Hall effect structures allow the direct measurement of the channel mobility and these investigations are subject of Section 5 in this paper.

Lateral MOSFET (LTMOS and LDDMOS) devices were processed on 2 μm thick, epitaxially grown, p-type layers; the aluminum (Al) acceptor concentration is 7×10^{16} cm^{-3}. The source and drain regions were formed either by a 0.3 μm thick epitaxially grown, N–doped ([N] = 1×10^{19} cm^{-3}) layer (LTMOS) structured by reactive ion etching, or by nitrogen implantation at 500 °C (LDDMOS). The nitrogen implantation for the LDDMOSFET devices consists of two box profile implantations. First, a box profile with a doping level of 1×10^{18} cm^{-3} was implanted to form the low-doped drain region, and then a second box profile was implanted with a doping level of 1×10^{20} cm^{-3} for the source and drain contact regions.

The vertical MOSFETs (VDMOS) were processed on 10 μm thick, N-doped ([N] = 5×10^{15} cm^{-3}), n-type epilayers with Al-implanted p-body regions and N- or phosphorus (P)-implanted source. An Al-implanted box profile (about 1 μm deep) combining five energies from 30 keV to 700 keV with maximum doping 1×10^{18} cm^{-3} was used to define the

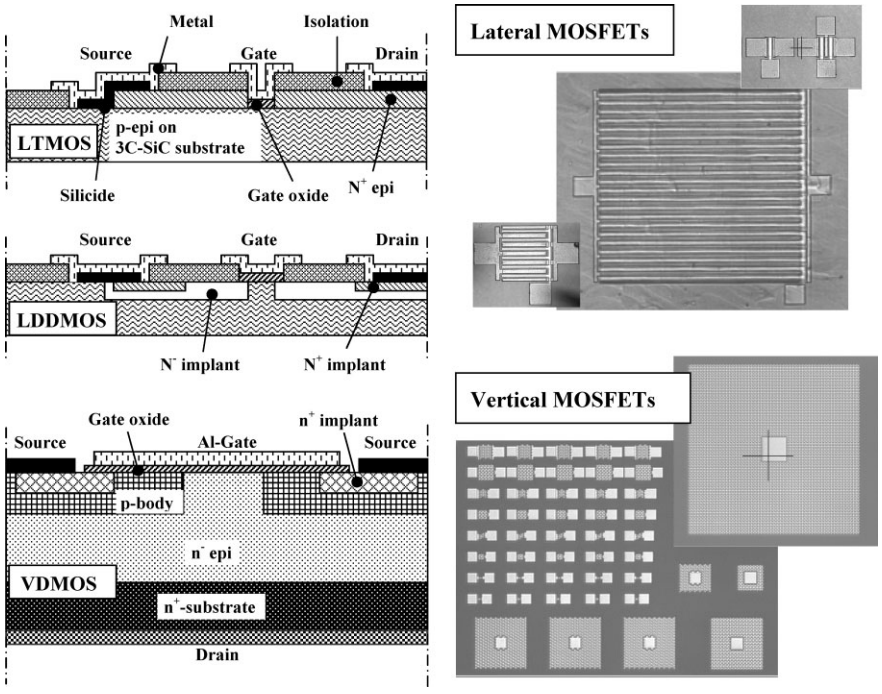

Fig. 4. Cross sections and optical microscopy images of the different lateral (LTMOS and LDDMOS) and vertical (VDMOS) MOSFET device structures. Each cross section represents a single cell. Multiple cells are obtained by mirroring the structure at their planes of symmetry (dash–dotted lines).

p-body region and the termination. A N- or P-implanted box profile (0.4 μm deep) combining the three following energies (50, 90, and 150 keV, or 70, 120, and 200 keV) with a maximum doping concentration of 4×10^{19} cm^{-3} defines the n^+ source region. All implantations of the VDMOSFET processing were done at room temperature.

The fabricated MOSFET devices had a gate oxide, which was thermally grown over 90 min at 1100 °C in dry oxygen, followed by a post-oxidation anneal for 3 h at 950 °C in wet oxygen. The resulting oxide thickness was about 60 nm. Some of the processed wafers had a shallow nitrogen implantation (30 keV, 5×10^{12} cm^{-2}) in the gate oxide region prior to the thermal oxidation, which has been reported to reduce the density of SiO_2/SiC interface states.[11] The MOSFET devices have a two level metallization with oxide/nitride isolation layers between gate and source interconnections. The ohmic source contacts were initially formed by nickel silicidation at 950 °C for 5 min. It was found that the high temperature silicidation degrades the 3C-SiC/SiO_2 interface (see Sec. 4). The nickel silicide ohmic contacts were replaced by sputtered titanium-tungsten (TiW) contacts. The TiW contacts prepared on highly P- or N-implanted 3C-SiC gave good as-deposited ohmic contacts, and hence high temperature treatments after gate oxide formation could be avoided.

4. Device Parameters of 3C-SiC MOSFETs

The purpose for processing lateral MOSFET devices was mainly to establish the technology for the vertical 3C-SiC MOSFET device processing. The lateral MOSFETs were not designed for high blocking voltages and the focus was on verifying the high channel mobility values of up to 260 cm^2 V^{-1} s^{-1} reported in the literature.[12-14] A summary of the results from the lateral 3C-SiC MOSFET devices is given in the literature.[15] Despite the determined low channel mobility, the high density of interface traps of more than 1×10^{13} cm^{-2} eV^{-1}, and the high number of crystalline defects (mainly stacking faults) in the 3C-SiC substrates, it was encouraging to see that functioning large-area 3C-SiC MOSFET devices can be processed and the output current is linearly scaling with the number of unit cells in the device. But it also became clear that the process technology for 3C-SiC and the 3C-SiC substrate quality have to be improved in order to achieve high performance vertical MOSFET devices suitable for power electronics.

The processing of the vertical MOSFET devices included several tests to develop further and to improve the established 3C-SiC processing technology. The high temperature silicidation process necessary to form ohmic contacts on source and drain was assumed to cause a degradation of the thermally grown gate oxide as the silicidation temperature of 950 °C is the same as the temperature during the post-oxidation anneal in wet oxygen. Therefore we tried as-deposited TiW contacts. The improvement can be seen from the comparison of the channel mobility of MOSFETs processed in the same batch with the same design and material quality (Fig. 5). There is an improvement by a factor of six in the channel mobility using an as-deposited TiW source and drain contacts with N-implanted source regions. The channel mobility improvements are attributed to a

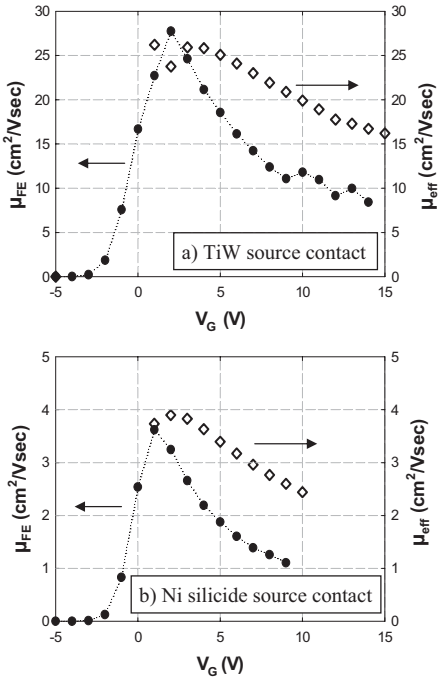

Fig. 5. Effective channel mobility, μ_{eff}, (open diamonds) and field-effect mobility μ_{FE} (filled circles) obtained from a hexagonal unit cell, vertical 3C-SiC MOSFET device with a) TiW and b) nickel-silicide source and drain contacts. The source region was formed by nitrogen ion implantation. The channel length is 2 μm.

quality improvement of the 3C-SiC/SiO_2 interface and a corresponding decrease in the density of interface traps. The higher channel mobility for MOSFETs with TiW contacts results in an increase in the output current of about one order of magnitude compared to MOSFETs with silicidiced Ni contacts. 1 mm × 1 mm MOSFETs could handle currents in the 1 A range indicating that the as-deposited TiW contacts are ohmic with a sufficiently low contact resistance.

A further improvement of the on-state characteristic of 3C-SiC MOSFETs was achieved by replacing the nitrogen source implantation by phosphorus implantation. The energy and dose parameters for the phosphorus implantation were calculated to give the same box profile as the previously used nitrogen implantation. Figure 6 shows a comparison of the output characteristics for 102 unit cell 3C-SiC MOSFETs with phosphorus (Fig. 6a) and nitrogen (Fig. 6b) source implantations. The channel length was 2 μm and the ohmic contacts were formed by as-deposited TiW. There is a 50 % increase in the output current for

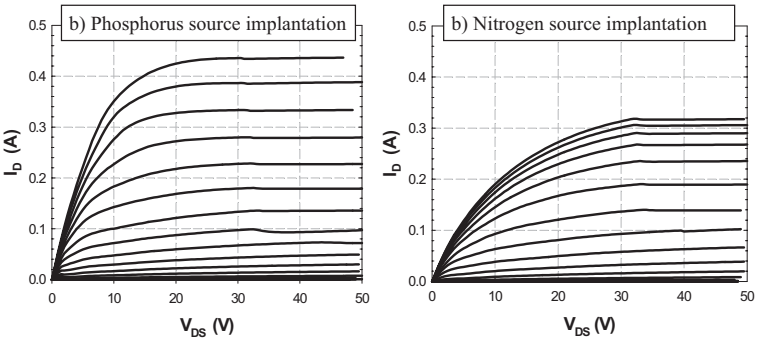

Fig. 6. Output characteristics of vertical 3C-SiC MOSFET devices with a) phosphorus source implantation or b) nitrogen source implantation. The MOSFETs have 102 hexagonal unit cells and 2 μm channel length. The ohmic contacts on source and drain were formed by as-deposited TiW.

P-implanted source MOSFETs compared to the N-implanted ones at the same gate voltage of 15 V. In addition, the I_D–V_D characteristcs of P-implanted source MOSFETs show at a certain gate voltage a steeper increase at lower drain voltages, and the saturation current is reached at drain voltages of 20 V indicating a higher degree of activation of the phosphorus and hence a lower sheet resistance of the implanted source regions.

In spite of the encouraging on-state characteristics of 3C-SiC MOSFETs, the present challenge to achieve high performance devices is on the off-state side. With the currently best processing technology, blocking voltages of 100 V were achieved with leakage currents below 1 mA for devices with about 100 unit cells. The hexagonal unit-cell geometry was showing higher blocking voltages compared to the square unit-cell design. The blocking capability deteriorates with increasing number of cells due to increasing device leakage. The blocking characteristics must be improved and blocking voltages in the range of 600 V to 1200 V with leakage currents below 100 μA should be achieved in order to make 3C-SiC MOSFETs useful for commercial applications. The present limitation of the device performance is determined by the available substrate quality; it has been shown that the presence of a high number of crystalline defects (of the order of 5000 defects per cm^2) like stacking faults increases the leakage current at a certain drain voltage by several orders of magnitude.[16] It is expected that the number of crystalline defects must be reduced to about 10 per square centimeter to achieve the desired blocking performance.

In summary, the present stage of the vertical 3C-SiC MOSFET development results in a good on-state performance using phosphorus source implantation and TiW ohmic contacts on source and drain. The prediction of the measured output characteristics to a higher number of unit cells indicates that 3 mm × 3 mm devices are capable of handling currents of up to 15 A. However, to make full use of the potential 3C-SiC can offer for vertical MOSFETs, the off-state characteristic must be improved. A blocking voltage of 600 to 1200 V is desired for commercial applications. To achieve such blocking voltages, the material quality has to be improved and the number of crystalline defects in the substrate must be reduced by approximately two orders of magnitude.

5. Hall-Effect Investigations in the Channel of 3C-SiC MOSFETs

Hall-effect investigations in the channel of n-MOSFETs allow the independent determination of both the free electron areal density, n_{inv}, and the electron Hall mobility, μ_H. This is essential for the analysis of SiC MOSFETs, because at the present state the density of interface traps D_{IT} of these devices is not negligible as is usually the case for silicon MOSFETs. Other methods, which are based on two-terminal (drain-to-source) measurements, reveal large errors due to the missing information on the free electron areal density, electron trapping at the interface, and fixed oxide charges.

In order to perform Hall-effect measurements on MOSFETs, special Hall structures are required, which allow potential measurements inside the channel. A typical configuration is the MOS Hall-bar design with a channel width to length ratio W:L < 1 and four additional voltage probes connected to the channel (see Fig. 7). The Hall-bar MOSFETs used for the investigations reported in this article were fabricated side by side with device-optimized

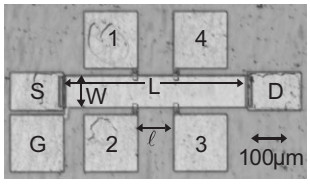

Fig. 7. Optical microscopy image of a 3C-SiC Hall bar LDDMOSFET with 4 additional voltage pads (indicated as 1 to 4) for 4-terminal resistivity and Hall-effect measurements (S = source, D = drain, G = gate). The dimensions of the structure are: gate length L = 500 μm, gate width W = 80 μm, distance between voltage probes ℓ = 100 μm.

LDDMOSFETs (see Sec. 3). Gate length, L, and gate width, W, were 500 μm and 80 μm, respectively. The distance, ℓ, of each voltage probe pair was ℓ = 100 μm.

The Hall-effect setup used is optimized for low current (<1 pA) and high resistivity measurements (>10 TΩ), which is required for Hall-effect and resistivity measurements in the channel of MOSFETs.[17] In order to reduce noise, the sourcemeters/electrometers are connected to a common ground at low plugs; the cable connections to the sample are triaxially shielded and guarded; the source-drain sourcemeter is connected to the sample holder by the cardboard-box principle. During a measurement sequence a positive gate bias, V_G, is applied to drive the MOSFET

into inversion. Then, while a small drain voltage, V_D, is applied, the source–drain current, I_D, as well as the voltage drop, V_{23}, between the voltage probes 2 and 3 parallel to the channel are measured. The small drain voltage, V_D, ensures that the MOSFET is operated in the linear region of the output characteristic I_D–V_D. A magnetic field, $B = 0.66$ T, is then applied perpendicular to the channel and the Hall voltage, V_{12}, is measured between the two voltage probes 1 and 2 on opposite sides of the Hall bar. In order to eliminate DC voltage offsets, the measurement is repeated with reversed magnetic field and different V_D. From the results, the free electron areal density, n_{inv}, the channel sheet resistance, R_S, and the electron Hall mobility, μ_H, in the inversion layer can be calculated:

$$n_{inv} = \frac{r_H}{e|R_H|} \text{ with Hall coefficient } R_H = \frac{1}{B} \cdot \frac{\partial V_H}{\partial I_D}, \text{ and}$$

$$V_H = \frac{1}{2}\left(V_{12}^{+B} - V_{12}^{-B}\right) \quad (1)$$

$$R_S = \frac{W}{\ell} \cdot \frac{\partial V_{23}}{\partial I_D} \quad (2)$$

$$\mu_H = \frac{|R_H|}{R_S} \quad (3)$$

The Hall scattering factor, r_H, for channel electrons in 3C-SiC is unknown. Experimental measurements show that $r_{H,bulk} \approx 1$ for bulk electrons in SiC.[18] In analogy to silicon technology,[19,20] the Hall scattering factor, r_H, for channel electrons is assumed to be comparable to $r_{H,bulk}$.

Figure 8a and b show the output characteristic, I_D–V_D, and the transfer characteristic, I_D–V_G, of the LDDMOSFET Hall structure, respectively. Due to the large gate length, the measured drain currents are only in the μA range. The rounded shape of the transfer characteristic is ascribed to the influence of interface traps.[21] From the extrapolation of the linear part of the slope[22] ($V_G > 25$ V), a threshold voltage, $V_T = 13.8$ V, is determined. The Hall mobility, μ_H, of the LDDMOSFET Hall structure at

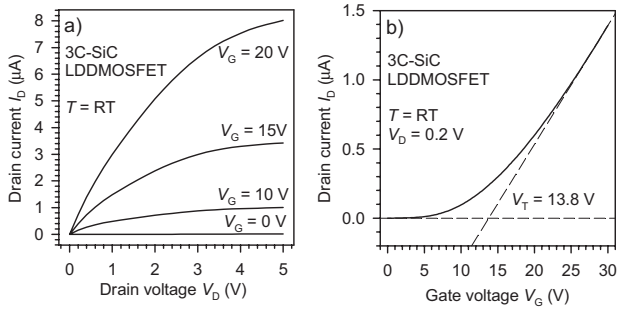

Fig. 8. a) Output characteristics I_D–V_D taken at room temperature for different gate voltages V_G. b) Transfer characteristic I_D–V_G taken at room temperature for $V_D = 0.2$ V. A threshold voltage of $V_T = 13.8$ V is obtained from the linear extrapolation.

$V_G = 25$ V as a function of temperature, T, the effective mobility[23]

$$\mu_{eff} = \frac{L/W}{C_{ox}(V_G - V_T)} \frac{\partial I_D}{\partial V_D} \quad (4)$$

and the field-effect mobility[23]

$$\mu_{FE} = \frac{L/W}{C_{ox} V_D} \frac{\partial I_D}{\partial V_G} \quad (5)$$

calculated from two-terminal measurements on the same structure are displayed in Figure 9. $C_{ox} = \varepsilon_{ox}\varepsilon_0/d$ is the oxide capacitance (oxide thickness $d = 60$ nm). Strictly speaking, μ_{FE} is a differential mobility associated with an incremental

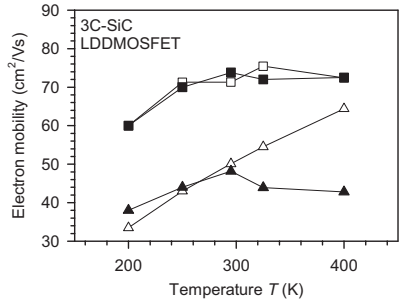

Fig. 9. Inversion electron Hall mobility, μ_H (open squares), differential Hall mobility, $\mu_{H,diff}$ (filled squares), effective mobility, μ_{eff} (open triangles), and field-effect mobility, μ_{FE} (filled triangles), as a function of the temperature. μ_H, $\mu_{H,diff}$, and μ_{eff} were obtained at $V_G = 25$ V; μ_{FE} was calculated from the slope of the linear part of the transfer characteristic. A maximum value of $\mu_H = 75$ cm^2 V^{-1} s^{-1} is reached at $T = 325$ K.

change in the electron density, δn_{inv}, when increasing the gate bias by an infinitesimal amount δV_G. Consequently, μ_{FE} values must be compared to the differential Hall mobility[24]

$$\mu_{H,diff}(V_G) = \frac{\mu_H(V_G + \delta V_G) n_{inv}(V_G + \delta V_G) - \mu_H(V_G) n_{inv}(V_G)}{n_{inv}(V_G + \delta V_G) - n_{inv}(V_G)} \quad (6)$$

which is also shown in Figure 9. A maximum value of $\mu_H = 75$ cm^2 V^{-1} s^{-1} is reached at $T = 325$ K. Both effective mobility, μ_{eff}, and field-effect mobility, μ_{FE}, obviously deviate from the Hall mobility, μ_H, and differential Hall mobility, $\mu_{H,diff}$, which is due to the fact that μ_{eff} and μ_{FE} are calculated neglecting any interface traps and oxide charges. The concordant decrease of all mobilities to lower temperatures is caused by scattering at charged impurities.[25]

Figure 10 shows the free electron areal density, n_{inv}, as a function of gate voltage, V_G, taken at different temperatures. n_{inv} grows with increasing V_G and increasing temperature. The solid and dashed curves are calculated for different temperatures on the basis of the charge-sheet model,[21] $Q_{inv}(\Phi_S) = Q_{SC}(\Phi_S) - Q_{dep}(\Phi_S)$. Q_{SC} is the total charge in

the semiconductor, including free charge carriers and fixed charges, and Q_{dep} is the total charge in the depletion layer, excluding free charge carriers. Q_{SC} and Q_{dep} are determined by integrating Poisson's equation and taking partial ionization of donors and acceptors into account. Φ_S is the surface potential, which is linked to the gate bias[26]

$$V_G(\Phi_S) = V_{FB} + \Phi_S - \frac{Q_{SC}(\Phi_S) + Q_{tot}(\Phi_S)}{C_{ox}} \quad (7)$$

V_{FB} is the flat-band shift of the MOS structure and $Q_{tot} = Q_{it} + Q_{ox}$ is the total fixed charge, which contains the interface traps and the fixed oxide charge. In general, $Q_{inv} = e \cdot n_{inv}$ as a function of V_G must be numerically solved. The simulations in Figure 10 have been calculated assuming $Q_{tot} \equiv 0$. It is clearly seen that n_{inv} is almost independent of T in the relevant temperature range for this

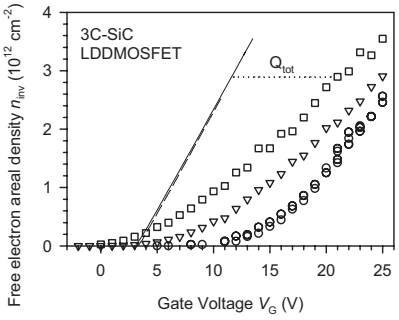

Fig. 10. Free electron areal density, n_{inv}, in the inversion layer obtained from Hall effect measurements as a function of the gate voltage, V_G, taken at various temperatures; $T = 200$ K (circles), $T =$ room temperature (triangles), $T = 400$ K (squares). The solid straight line is calculated on the basis of the charge-sheet model.

ideal case. From the horizontal shift, $V_{G,ideal}$–$V_{G,exp}$, of the experimental n_{inv} values compared to the simulation, the total fixed charge can be derived (horizontal dotted line in Fig. 10) as $Q_{tot}(\Phi_S) = C_{ox}(V_{G,ideal} - V_{G,exp})$. It is displayed in Figure 11a as a function of energy, $E - E_V = e\Phi_S + E_i$ (E_i: intrinsic level). Q_{tot} changes its sign; the positive charge at smaller energies (E–E_V) and/or in the oxide is overcompensated by acceptor-like negatively charged interface states close to the conduction band edge.[17]

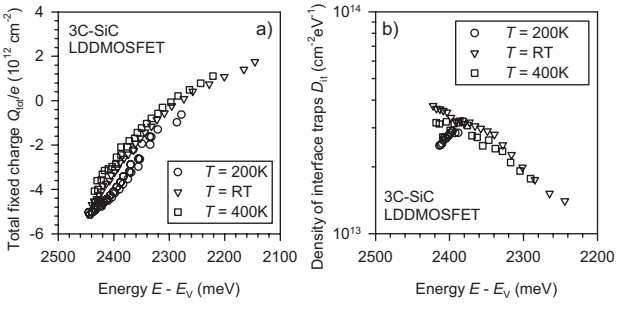

Fig. 11. a) Total fixed charge $Q_{tot} = Q_{ox} + Q_{it}$ and b) density of interface traps, D_{IT}, as a function of the energy (E–E_V) related to the valence band edge of 3C-SiC, and taken at various temperatures; $T = 200$ K (circles), $T =$ room temperature (triangles), $T = 400$ K (squares).

Assuming that Q_{ox} is independent of the surface potential, Φ_S, the derivation

$$D_{IT}(\Phi_S) = \frac{1}{e^2}\frac{\partial Q_{tot}}{\partial \Phi_S} \quad (8)$$

results in the density of interface states, D_{IT}. This quantity as a function of energy related to the valence band edge, E_V, is shown in Figure 11b. Note that the measured, small, Hall voltages cause an uncertainty in the determination of the energy position (E–E_V), which is responsible for the shift of the x-scale in Figure 11a and b. D_{IT} is largely independent of the temperature and increases exponentially towards the conduction band edge E_C. It reaches an unexpectedly high value of $(3\text{–}4) \times 10^{13}$ cm^{-2} eV^{-1} at E_C. This value (determined in the inversion layer of a p-type 3C-SiC MOSFET) is about two orders of magnitude greater than corresponding D_{IT}-values determined in n-type 3C-SiC MOS capacitors (cf. Sec. 2). This observation gives rise to our suggestion that the device processing or the quality of the deposited p-type 3C-SiC epilayer does not yet meet the required quality and has to be improved. Hall structures fabricated with the latest process parameters (cf. Sec. 3) have not been tested yet. The increased performance of the device-optimized state-of-the-art 3C-SiC VDMOSFETs (Sec. 4) compared to previous LDDMOSFETs indicates a promising reduction of D_{IT}.

6. Conclusions

At the interface of n-type 3C-SiC/SiO_2 MOS capacitors, the density of traps close to the conduction band edge reached values in the range of 10^{11} cm^{-2} eV^{-1} by suitable processing. Interface traps are predominantly ascribed to carbon clusters and near interface traps located in the oxide close to the interface.

Lateral and vertical MOSFET devices with varying size containing several thousand unit cells were fabricated on 2 inch 3C-SiC (001) substrates manufactured by HAST. The encouraging result is that operating, large area, 3C-SiC MOSFET devices could be processed and that the output current scaled linearly with the number of unit cells. Several processing steps were tested and optimized. For example, the substitution of silicide contacts on source and drain by TiW contacts resulted in an increase of the output current at a gate voltage of 15 V by two orders of magnitude. Further replacing the nitrogen source implantation by phosphorus implantation brought a clear improvement of the on-state characteristic. The obstacle of the device performance is still the blocking behavior. With the currently best processing technology, blocking voltages of 100 V were reached with leakage currents below 1 mA. The leakage current is probably caused by extended crystal defects

(e.g., stacking faults) in the substrates, which have to be distinctly reduced.

Hall-effect measurements were conducted in specially designed MOS Hall-bar structures. The electron Hall mobility, μ_H, and free electron areal density, n_{inv}, were independently determined as a function of the temperature, T, and the gate voltage, V_G. A maximum value of $\mu_H = 75$ cm^2 V^{-1} s^{-1} was obtained at $T = 325$ K. Comparing the measured with a calculated ideal $n_{inv}(V_G)$ curve, an unexpectedly high value of the interface trap density of $(3–4) \times 10^{13}$ cm^{-2} eV^{-1} is obtained, about two orders of magnitude higher than the corresponding value determined in n-type 3C-SiC/SiO_2 MOS capacitors. The origin for this discrepancy is under investigation.

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