Recent developments in SiC single-crystal electronics

1992 Semicond. Sci. Technol. 7 863

(http://iopscience.iop.org/0268-1242/7/7/001)

Semicond. Sci. Technol. 7 (1992) 863–880. Printed in the UK

REVIEW ARTICLE

Recent developments in SiC single-crystal electronics

P A Ivanov and V E Chelnokov

A F Ioffe Physico-Technical Institute, 26 Polytekhnicheskaya st.,
St Petersburg 194021, Russia

Received 27 February 1992, accepted for publication 15 April 1992

Abstract. The present paper is an analytical review of the last five or six years of research and development in SiC. It outlines the major achievements in single-crystal growth and device technology. Electrical performance of SiC devices designed during these years and some new trends in SiC electronics are also discussed.

During the 1980s the studies on sublimation and liquid-phase epitaxial growth of SiC single crystal were continued successfully. At that time, such methods as chemical vapour deposition, thermal oxidation, 'dry' plasma etching and ion implantation, which yielded good results with silicon, came into use. As a result of the technological progress, discrete devices appeared, which incorporated the potential advantages of SiC as a wide bandgap material. Among these were high temperature (500–600 °C) rectifier diodes and field-effect transistors, high-efficiency light-emitting diodes for the short-wave region of the visible spectrum, and detectors of ultraviolet radiation. It should be stressed that the devices were of commercial quality and could be applied in various fields (control systems of automobile engines, aerospace apparatus, geophysical equipment, colour displays in information systems, etc).

The developments in technology and the promising results of research on electrical performance of the devices already available give us hope that in the near future SiC may become the basic material for power microwave devices, and for thermo- and radiation-resistant integrated circuits. This process can be stimulated by further perfection of single-crystal substrates of large area, by development of stable high temperature ohmic contacts, micro- and heterostructures.

1. Introduction

The present review aims at introducing the reader to some of the recent developments in the field of electronics based on single-crystalline silicon carbide, a semiconductor possessing a unique combination of properties for device applications.

Silicon carbide is the only binary compound of carbon and silicon existing in a solid phase. It crystallizes in either sphalerite (β-SiC) or wurtzite (α-SiC) structure to form an ion-covalent bond. The high Si–C bonding energy in silicon carbide ($\simeq$ 5 eV) makes it resistant to high temperature and radiation, imparts it mechanical strength and chemical stability and is the cause of low diffusion rates of dopants and host atoms. Among materials in which impurity conduction, both n- and p-type, can be controlled in wide ranges, SiC is the one possessing the widest bandgap, varying from 2.3 eV in a cubic polytype β-SiC up to 3.4 eV in a hexagonal polytype 2H α-SiC. Therefore, an undoped SiC single crystal is in fact an insulator at room temperature. For example, the intrinsic carrier concentration at $T = 300$ K in one of the most common hexagonal polytypes 6H α-SiC is as low as $10^{-6}\,\mathrm{cm}^{-3}$. On the other hand, the solubility limit of dopants in SiC amounts to 10^{20}–$10^{21}\,\mathrm{cm}^{-3}$, which provides resistivities of 10^{-2}–$10^{-1}\,\Omega\,\mathrm{cm}$ in the n-type material and 10^{-1}–$10^{0}\,\Omega\,\mathrm{cm}$ in the p-type material. Owing to good impurity conduction, all classical types of semiconductor devices can be fabricated in SiC. A comparison of electrical and physical properties of SiC with those of Si, GaAs and GaP (table 1) shows that SiC devices may have a number of advantages.

One of the most important advantages of SiC devices is high operating temperature. This is due to the fact that the intrinsic carrier concentration does not exceed $10^{14}\,\mathrm{cm}^{-3}$ at 1300 K in 6H α-SiC and at 1100 K in β-SiC because of the wide bandgap, i.e. a p–n junction can exist up to these high temperatures. SiC is superior to Si and GaAs in possessing an avalanche breakdown

0268-1242/92/070863+18$04.50

Table 1. Comparison of semiconductors.

Property	Si	GaAs	GaP	β-SiC	6H α-SiC
Bandgap (eV)	1.1	1.4	2.3	2.3	3.0
Maximum operating temperature (K)	600	760	1250	1200	1580
Melting point (K)	1690	1510	1740	sublimation at 2100	
Physical stability	good	fair	fair	excellent	excellent
Electron mobility ($cm^2 V^{-1} s^{-1}$)	1400	8500	350	1000	400
Hole mobility ($cm^2 V^{-1} s^{-1}$)	600	400	100	40	40
Breakdown field (10^5 V cm^{-1})	3	4	7	—	40–60
Thermal conductivity (W $cm^{-1} K^{-1}$)	1.5	0.5	0.8	3	5
Saturated electron drift velocity (10^7 cm s^{-1})	1	2	—	2.5	2.5
Dielectric constant	11.8	12.8	11.1	10.0	10.0

field (E_b) an order of magnitude higher, high thermal conductivity (κ), which is close to that of copper, and a somewhat higher saturation value of the electron drift velocity (v_s). With this combination of parameters, much higher output power and/or operating frequency can be achieved in SiC devices. Ultimately, because of the wide bandgap of SiC, light-emitting diodes covering the entire visible spectrum and photodiodes for the ultraviolet are feasible.

High chemical and physical stability of silicon carbide has caused considerable technological difficulties in high temperature growth of single crystals and in chemical and mechanical treatments. Therefore, in spite of the unique properties of SiC as a material for device applications, systematic studies in the field of SiC electronics have been undertaken only in the last several years, following successful solution of the technological problems by improving the available methods and developing new techniques specific to SiC. The most intensive studies have been carried out in the former USSR, the USA and Japan. It is to be stressed that the technological standard attained as a result of these efforts makes possible commercial production of some types of semiconductor devices in SiC. Growing interest in silicon carbide is evident from the fact that several international conferences have already been organized since the late 1980s (Silicon Carbide: at the 176th Meeting of the Electrochemical Society, 1988; Amorphous and Crystalline Silicon Carbide: Santa Clara, CA, 1988 and 1991, Hollywood, FL, 1990; Silicon Carbide: at the European Materials Research Society Symposium, Strasbourg, France; at the 1st High Temperature Electronics Conference, Albuquerque, NM, 1991).

2. Single-crystal growth

2.1. Sublimation

At atmospheric pressure SiC does not melt but it undergoes sublimation at temperatures above 1800 °C, producing Si, SiC_2 and Si_2C vapours. This property of SiC is now widely used for growing bulk single crystals and epitaxial layers as well as for high-quality polishing etching prior to epitaxy.

The sublimation process still remains the only growth method providing large bulk SiC crystals. Before the 1980s, the Lely method of sublimation growth was the only one in use [1], in which spontaneous crystallization proceeds from the sublimation products of polycrystalline SiC. The process is carried out in an argon atmosphere at temperatures of about 2500 °C in a tight graphite container to prevent an escape of sublimation vapours from the growth cell. As the source polycrystalline SiC sublimes, the vapours penetrate a porous graphite cylinder to produce lamellar crystals on its inner surface. The most serious drawback of the Lely method is uncontrollable nucleation, which causes simultaneous growth of several SiC polytypes (6H polytype dominating over 15R and 4H), and a small size of the crystals obtained, $5 \times 7\,mm^2$ on the average.

Tairov and Tsvetkov [2, 3] and Ziegler *et al* [4] have modified the sublimation method of growing SiC single crystals. Using the results of thermodynamic calculations of SiC–C and SiC–Si systems and the studies on mass transfer kinetics and crystallization of sublimation products, Tairov and Tsvetkov [3] established the conditions necessary for growing SiC boules following the classical scheme of condensation of oversaturated vapour onto a seed crystal. The cross section of a reaction chamber for the modified sublimation growth [4] is shown schematically in figure 1. A seed crystal and a polycrystalline source material are placed at opposite ends of a container, along which a temperature gradient

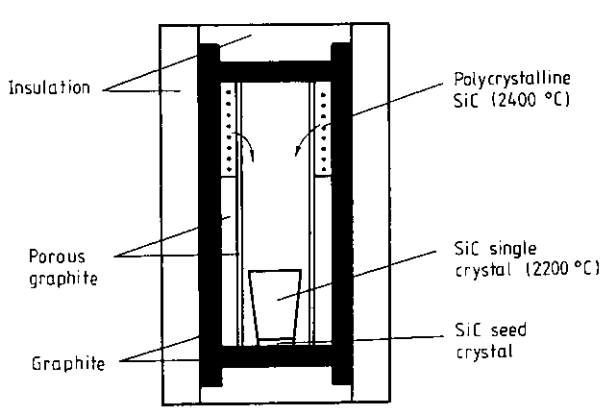

Figure 1. Growth chamber for the modified sublimation process [4].

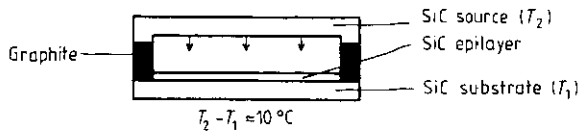

Figure 2. Growth cell for the epitaxial 'sandwich' method [7].

of 10–20 °C cm^{-1} is established (2300–2500 °C at the source and 2100–2200 °C at the seed). SiC sublimes from the source and the products condense onto the cooler seed. The process is carried out at a low argon pressure, allowing one to grow boules of 20 mm in length and up to 30 mm in diameter at a rate of about 4 mm h^{-1} [5, 6].

Apart from the growth of bulk crystals, the sublimation process is being successfully applied to grow thin epitaxial films. Vodakov *et al* [7, 8] have developed a so-called 'sandwich' method of SiC sublimation epitaxy (figure 2). In this method a single-crystalline or polycrystalline source is separated from the substrate by a small gap of about 1 mm. The growth conditions with this arrangement turn out to be nearer to equilibrium ones, allowing the growth to be carried out in wider ranges of temperature and pressure, even in vacuum. The layer quality is found to depend critically on the tightness of the growth cell: even minute deficiency in silicon in the vapour phase leads to formation of voids and/or increased dislocation density.

The 'sandwich' method has been modified by Anikin *et al* [9, 10]. First, an additional silicon vapour source is introduced to maintain equilibrium conditions in the growth cell. This measure permits significant reduction of the amount of graphite rigging and, hence, a higher vacuum in the system. Second, sublimation etching of the substrate under conditions of reversed temperature gradient is performed prior to epitaxy. This makes it possible to grow, at low rates, thin (1–20 μm) homoepitaxial layers of 6H and 4H α-SiC with the residual impurity concentration of less than 10^{16} cm^{-3} and the density of dislocations less than 10^2 cm^{-2} [10]. This method proved to be very effective when applied to fabrication of 6H α-SiC devices (see section 4).

2.2. Liquid-phase epitaxy

As noted above, SiC cannot exist in a molten state at atmospheric pressure, yet it can dissolve in the melts of silicon and some metals. The ability of SiC to dissolve in the Si melt allows SiC growth by liquid-phase epitaxy (LPE). This method does not differ in principle from the well known technique of liquid-phase epitaxy of III–V compounds. When compared with sublimation epitaxy, liquid-phase epitaxy has the advantages of lower growth temperature (1500–1700 °C) and growth conditions nearer to equilibrium ones. The growth of SiC layers may occur both in isothermal conditions (at a temperature gradient) and in non-isothermal conditions (on forced cooling of the melt). Doping of the layers is performed by introducing a dopant host in the

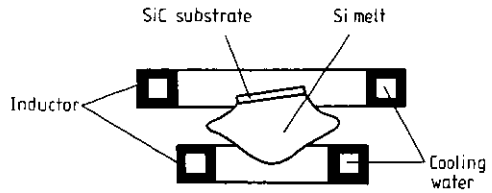

Figure 3. Container-free scheme of liquid-phase epitaxial growth [16].

melt or by feeding a dopant gas into the reaction chamber. Choosing a crucible for the chemically aggressive silicon melt, which interacts with practically all construction materials, poses a serious problem. In earlier studies [11–14] graphite containers were used. In this case the Si melt happened to be automatically saturated with carbon from the crucible walls, simultaneously producing uncontrollable contamination.

Dmitriev *et al* [15] have modified the liquid-phase epitaxy of SiC from the Si melt. In their method the melt is held suspended in an electromagnetic field, so no container is required (figure 3). The carbon source for saturating the silicon melt is silicon carbide introduced into the melt. The method has proved very convenient for investigating SiC crystallization from the liquid phase. Studies on doping with nitrogen [16] and aluminium [17] have been carried out and doping procedures developed which permit one to grow multilayer SiC structures with several p–n junctions in a single epitaxial run [18]. The junctions have been used successfully for fabrication of various types of device.

2.3. Chemical vapour deposition

For a long time the potential advantages of SiC in device applications attracted little attention because of the difficulties in growing large-area single crystals. Interest in SiC greatly increased in the mid-1980s when a chemical vapour deposition (CVD) process was developed and thin single-crystalline films of cubic β-SiC were grown on large-area silicon substrates [19–21] at relatively low (compared with sublimation and LPE) temperatures of about 1300 °C. This success stimulated a large number of studies of CVD growth of silicon carbide, using Si and 6H α-SiC substrates. The number of publications dealing with CVD growth of silicon carbide and with various aspects of device application is now well above two hundred.

It was shown in the earlier studies [22–26] that thermodynamic equilibrium is possible between SiC and various gaseous mixtures of Si- and C-containing gases, such as SiH_4, $SiCl_4$, CH_4, C_2H_2, C_3H_8, $C_3H_3SiCl_3$ and H_2. It was also shown that SiC could be deposited from gaseous mixtures only at a certain silicon-to-carbon ratio. In particular, at atmospheric pressure the ratio $Si/(Si+C) < 0.5$ should be maintained [22, 24, 26]. For larger values of this ratio, deposition of SiC requires lower pressures and higher temperatures. The main problems with growth of single-crystalline β-SiC films on Si substrates are those arising from a mismatch of

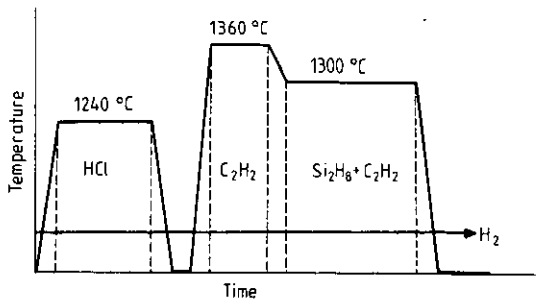

Figure 4. Temperature programme for CVD growth with a 'buffer' layer [29].

the lattice constants (about 20%) and thermal expansion coefficients (about 8%) for these materials. Nishino *et al* [19] were the first to solve this problem by developing a 'buffer' CVD process. According to the 'buffer' technique, a typical sequence of monocrystalline β-SiC(100) layer growth on Si(100) substrates includes three steps (figure 4). First, a heated Si substrate is etched in a flow of HCl and H_2. Then the system is cooled down to room temperature and a C-containing gas is introduced. During the subsequent heating the Si substrate is 'carbonized'. Ultimately, the system is cooled to the growth temperature and a Si-containing gas is introduced to start the growth of the monocrystalline β-SiC layer. The nature of the β-SiC/Si interface is not yet fully understood. No 'buffer' layer as a region separating the two lattices and structurally different from both has been observed [27]. It is interesting to note that in later studies [28, 29] monocrystalline β-SiC layers were grown on Si substrates without resorting to the 'buffer' technique.

Various types of defect have been identified in transmission electron microscopic studies of β-SiC layers grown on silicon [30–32]: mismatch dislocations, stacking faults (SF), antiphase boundaries (APB). In contrast to heteroepitaxial systems, such as GaAs/Si in which mismatch dislocations dominate in the neighbourhood of the interface, in the β-SiC/Si system the dominant defects are stacking faults, whose small energy (GaAs: 55 mJ m^{-2}; SiC: 2.5 mJ m^{-2}) is responsible for SiC growth in various polytypes, which is revealed in an arbitrary sequence of close-packed planes. Attempts have been made to eliminate or reduce the densities of all types of defect. It has been established with certainty that APBs can be eliminated if inclined Si substrates are used with the surface tilted 1–4° from the [100] axis towards [011] [33, 34]. The SF planes are along the {111} faces. Their density drops exponentially away from the interface [35] and may be reduced by using properly patterned Si(100) substrates [36]. In addition, the lower SF density in crystals grown on inclined substrates can be accounted for by the SF length being controlled by the surface steps. Successful growth of large 6H α-SiC single crystals by the modified sublimation method has raised interest in β-SiC layer growth on 6H α-SiC substrates, because in this case the lattice constants and thermal expansion coefficients differ less than in the growth on Si(100). The (0001) planes of 6H α-SiC are close-packed, hence the surfaces of β-SiC layers grown on α-SiC should also be close-packed or (111) planes [39]. The growth of β-SiC layers on the (0001) plane of 6H α-SiC under certain conditions may proceed through lateral outgrowth of the nuclei. If two differently oriented nuclei meet on the growth surface (one at an angle of 60° with respect to the other), a defect is formed called a double position boundary (DPB), along which stacking faults develop to accommodate mechanical strain [37]. In an attempt to preclude the DPB formation the film growth was tried on inclined substrates, but instead, homoepitaxial growth of 6H α-SiC took place [38, 40]. High quality of the films was confirmed by excellent characteristics of various types of devices produced with these films (see section 4.3)

3. Device technology

3.1. Reactive ion etching

To produce a relief on a silicon carbide surface, some difficulties arising from chemical inertness of SiC should be overcome. Chemical etching can proceed only at high temperatures: in molten alkali (at 500 °C), in a flow of chlorine or chlorine-containing gases (at 1000 °C), and in gaseous hydrogen (at 1300 °C). Besides, polishing etching is possible in silicon vapours at sublimation temperatures (1800 °C and higher). The main requirements of the etching process, when used to make a device, are as follows: (i) low temperatures, (ii) high quality of the surface treatment, (iii) high selectivity of etching with respect to the mask material and (iv) high resolution and anisotropy. To solve this problem, an etching study of SiC was undertaken using Ar plasma [41] and plasmas of fluorine-containing gases, such as CF_4 [42, 43], CF_4+O_2 [41, 45], NF_3 [44], SF_6 [43, 46], SF_6+O_2, CHF_3+O_2 and $CBrF_3+O_2$ [47]. The etching experiments were carried out in a parallel plate reactor with RF plasma (E-mode or H-mode). Etching with Ar ions, by means of direct physical removal of SiC, provides high anisotropy and resolution, but the slow rates (less than 1 μm h^{-1}) and the low selectivity make this process unattractive for device fabrication. Rates higher by two orders of magnitude were achieved by Syrkin *et al* [43] with an H-mode RF plasma of fluorine-containing molecular gases, in which free atomic fluorine was produced as a result of plasma-assisted dissociation. The etching mechanisms involved were discussed in detail by Pan and Steckl [47]. It was found that the etching rate of SiC increased with increasing free fluorine concentration and DC bias, whereas the etching rate of silicon showed no variation with bias and was dependent solely on the concentration of fluorine atoms. It was concluded from these observations that the etching of SiC proceeded according to a reactive ion mechanism, which is a combination of chemical reactions and direct physical removal. The removal of silicon and carbon

Table 2. Reactive ion etching of silicon carbide.

Gases	Etching rate (nm min^{-1})	Anisotropic ratio†	Selectivity
	E-mode		SiC:Si [47]
CHF_3 + 90% O_2	75	17:1	2:1
$CBrF_3$ + 90% O_2	38	6:1	2:1
SF_6 + 35% O_2	53	10:1	1:26
SF_6 + 90% O_2	40	11:1	1:2
	H-mode		SiC:Al [43]
SF_6	1700	10:1	15:1
CF_4	500	5:1	10:1

†Vertical/lateral.

atoms is assumed to be occurring in different ways: the Si atoms react with fluorine to form volatile SiF_4 and the C atoms are removed in a physical way. The second process is much slower than the first, therefore the SiC surface becomes rich in carbon and the etching rate of SiC drops to a lower value than that for Si under the same conditions. The 'carbon-blocking' model proposed by Pan and Steckl [47] can account for a rather high anisotropy observed in the etching of SiC: the vertical carbonized surface formed in mask etching is not subjected to ion bombardment, so it blocks etching in the lateral direction perpendicular to the ion beam. The data on the rates, selectivities and anisotropy obtained in the reactive ion etching of SiC with different gaseous mixtures are given in table 2.

3.2. Thermal oxidation

Thermal oxidation is one of the most important processes in the fabrication of silicon devices. SiO_2 layers thermally grown on Si are used as a mask in diffusion doping of silicon, for passivation of p–n junctions and in the preparation of MOS structures. SiC offers higher resistance to thermal oxidation than Si. Under the conditions usual in silicon oxidation procedures (an oxygen atmosphere, wet or dry, and temperatures 800–1200 °C) it takes up to several hours to obtain a sufficiently thick oxide film on SiC [48–51]. Auger electron spectroscopy (AES) of thick oxide films on SiC [48, 50] has shown that these are homogeneous and close in composition to stoichiometric SiO_2. Experiments with SiC oxidation revealed great differences in the oxidation rates between various polytypes [50, 52, 53] as well as between the crystal faces of the same polytype, e.g. (0001)C and (0001)Si faces of 6H α-SiC [51, 54, 57, 58] (figure 5). At the same time, the growth of SiO_2 on SiC follows predictions of a generalized linear-parabolic model of Deal and Grove [55]. According to this model, diffusion of either the oxidizing agent or the oxidation reaction products through a thick oxide layer is a rate-limiting process resulting in a parabolic law variation of the oxide thickness with time. The activation energy of the parabolic rate constant (about 50 kCal mol^{-1}) varies insignificantly from one polytype to another [50, 51]. It is considered that the growth of a thick oxide film is limited by diffusion through the film of CO produced in a chemical reaction of carbon and oxygen. On the other hand, the growth of thin oxide films (short oxidation times) is limited by the oxidation kinetics at the oxide/semiconductor interface. In this case the oxide thickness grows linearly in time. The activation energy of the linear rate constant varies with the polytype and orientation. It is found that for β-SiC(100) layers this energy is approximately 74 kCal mol^{-1} [50] and for the polar (0001)C and (0001)Si faces of 6H α-SiC it equals 26 and 80 kCal mol^{-1}, respectively [51, 56]. The above assumption about different kinetic oxidation rates for these faces was confirmed in experiments on linear oxidation of atomically clean polar faces of 6H α-SiC in ultra-high vacuum [54].

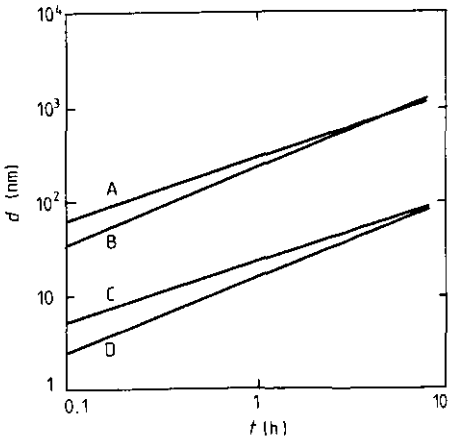

Figure 5. Oxide thickness versus time for SiC wet oxidation at 1420 K: C face of 6H α-SiC (A) and β-SiC (B); Si face of β-SiC (C) and 6H α-SiC (D) [57].

3.3. Ion implantation

In commercial technology of Si devices, great importance is attached to diffusion and ion implantation. These processes play a key role in the local doping performed through windows in a thermally grown oxide film. Because the diffusion coefficients for most dopants in SiC are negligible at temperatures below 1800 °C, the development of ion implantation for SiC microtechnology is of major importance.

Following ion implantation, the damage of the crystal structure induced in the process has to be healed and the dopants introduced electrically should be activated. This is achieved in a high-temperature anneal of the doped layers. Thermal annealing investigations of SiC layers implanted with N^+ [59, 61], P^+ [61], Al^+ [60, 62, 63] and Ga^+ [63, 64] have revealed a number of problems typical for thermal annealing of room-temperature implanted SiC. These are (i) incomplete recovery of the crystalline structure in samples doped with large ion doses exceeding a critical dose for transition to the amorphous state [65]; (ii) surface carbonization during high-temperature annealing in vacuum [59, 67]; (iii) redistribution and/or out-diffusion of dopants away from

the implanted layer [64, 65]. Thermal annealing investigations of SiC implanted with a 4×10^{14} cm^{-2} dose of nitrogen at room temperature [61] have shown that during the anneal at temperatures of 1100–1300 °C the relative concentration of the electrically active impurity continuously rises (by 20–80% for an annealing time of 0.5 h). Particular difficulties were encountered in the ion doping of silicon carbide with acceptors, which cause transition to the amorphous state at doses $\sim 10^{15}$ cm^{-2} [63], while the losses due to out-diffusion of ions are as great as 90% [64, 65]. The first good-quality abrupt p^+–n junctions in SiC were fabricated by Suvorov *et al* [68] by implanting large doses of aluminium (10^{16}–10^{17} cm^{-2}) with subsequent high-temperature (1800 °C) short-duration (10 s) annealing of the implanted layer. Because high-temperature annealing is not always compatible with other technological processes of device fabrication, methods have been developed for ion doping of SiC with nitrogen and aluminium, which represent a combination of hot implantation (550 °C) and annealing at a rather low temperature (1200 °C) [69]. It is to be noted that the implantation temperature should be optimized. So, the use of very high temperatures (1400 °C) leads to considerable deviations from the stoichiometry and to the polytype transformations [66].

3.4. Ohmic contacts

As noted above, the properties of silicon carbide make feasible SiC devices for high-temperature, high-power and high-frequency applications. One of the problems in the realization of such devices is the production of highly stable low-resistance ohmic contacts to silicon carbide. Some compromises have to be found in solving this problem. For example, better adhesion is achieved through chemical reactions between the metal and the semiconductor and/or diffusion of the atoms. Besides, diffusion of the metal atoms into the semiconductor may lower the contact resistance if it results in additional doping of the semiconductor region adjacent to the surface. However, if chemical reactions and diffusion were to occur during the device operation, this might adversely affect the long-term stability of the device characteristics. Additional complications arise if gold is used as a high-conductivity coating of the contact metal because of its high diffusion rate at elevated temperatures.

A compromise solution to the problem of obtaining stable high-temperature ohmic contacts to SiC is being sought in appropriate combinations of refractory metals with gold and various doping admixtures. Refractory metals capable of forming carbides and silicides play the role of a contact metal and/or a diffusion barrier for gold, the latter providing a good current spread over the contact area. Studies of contact systems based on refractory metals, such as chromium [70, 71], nickel [71, 72], titanium [73, 74], tantalum [74] and tungsten [74–76], have demonstrated that physical and chemical properties and electrical characteristics of the contacts are affected by the following factors: (i) enrichment of the SiC surface with either silicon or carbon as a result of various treatments; (ii) orientation and doping level of the substrate; (iii) temperature and duration of the anneal of the deposited metals. Fairly good physical and chemical stability at high temperatures was shown by Ti/SiC and Cr/SiC contacts to a SiC surface enriched with carbon in a prior treatment. In this case carbides were formed at the interface [70, 73]. Still higher stability was exhibited by W/SiC contacts. In AES studies of the W/SiC interface the presence of both WC and WSi_2 was detected [75, 76]. According to the data of Geib *et al* [75], no appreciable changes occurred in the interfacial chemistry in the W/β-SiC system up to an annealing temperature of 650 °C. The AES data by Syrkin *et al* [76] for a W/(0001)C 6H α-SiC interface annealed at a high temperature (1600 °C) gave evidence for silicon diffusion from SiC into tungsten. The contact structure was represented as follows: tungsten/WSi_2–WC/partially disordered SiC deficient in Si/stoichiometric silicon carbide. It should be noted that the annealing temperature at which the contact was formed varied in a wide range from 800 to 1800 °C; it was determined by the extent to which the composition of 6H α-SiC deviated from the stoichiometric composition, as well as by the orientation and doping level of the substrate and by the disorder in the near-surface region.

Table 3. Contact resistance of some metal systems deposited onto SiC.

Semiconductor	Metal system	Resistance (Ω cm^2)	Ref.
n-type β-SiC	Au/Ta	2×10^{-3}	[74]
	Au/W	8×10^{-4}	[74]
	Au/Ti	1×10^{-3}	[74]
	Au/Ni	2×10^{-3}	[72]
	W	8×10^{-2}	[75]
n-type 6H α-SiC	Al/W	1×10^{-4}	[76]
	Ni, Cr	3×10^{-4}	[71]
p-type 6H α-SiC	Al/W–Au/W/Al	2×10^{-4}	[76]

The contact resistance values for some systems based on refractory metals are listed in table 3. In thermocycling tests of Au/Ta/SiC, Au/Ti/SiC and Au/W/SiC contacts at 600 °C, the Au/W/SiC contact was found to have the highest electrical stability [74]. This fact can be accounted for by high stability of the W/SiC interface and by tungsten presenting a good barrier to diffusion of gold. It should be remarked that although some progress in high-temperature contacts to SiC has been achieved, the resistance of the contacts to both n- and p-SiC is still no better than 10^{-4} Ω cm^2. It will be seen in subsection 5.1 that this value is not sufficient to exploit fully the potential advantages of SiC in power microwave devices.

4. Discrete devices

4.1. Diodes

Lately, various types of diode have been demonstrated in silicon carbide. These are rectifier diodes with p–n

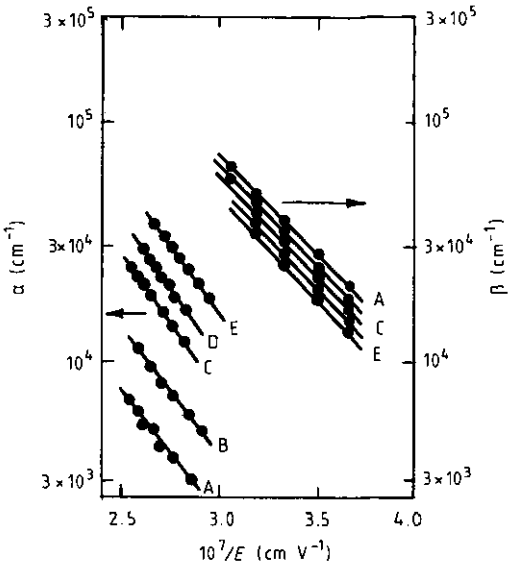

Figure 6. Electron (α) and hole (β) coefficients of impact ionization in 6H α-SiC versus electric field at $E \parallel C$: (A) 294 K, (B) 370 K, (C) 470 K, (D) 570 K, (E) 670 K [99].

junctions [77–83] or Schottky barriers [84–88], diodes with N- [89] and S-shaped [90] I–V characteristics, voltage stabilizers with reverse-biased [91, 92] and forward-biased [91] junctions. Progress in SiC technology has paved the way to systematic studies of electronic processes in diode structures and their applicability to various devices.

Experimental studies of static electrical characteristics of epitaxial 6H α-SiC p–n junctions [93] and Schottky barriers [84] in the temperature range 300–800 K have shown that they can be described by a complete depletion model. The built-in potential decreases with temperature in the same way as does the Fermi level position in the quasi-neutral regions of the structure.

The avalanche breakdown of microplasma-free p^+–n junctions had a number of anomalies for the electric field orientation $E \parallel C$: (i) a high value of the breakdown field $(3\text{–}6)\times10^6$ V cm^{-1} [94, 95], in excess of estimates by Sze [96]; (ii) a negative temperature coefficient of the breakdown voltage [95, 97]; (iii) current filamentation in the avalanche breakdown [98]. To explain these anomalies, Konstantinov [99] studied the temperature variation of electron and hole coefficients of impact ionization in 6H α-SiC p^+–n junctions and found the impact ionization coefficient for electrons α to be much smaller than the coefficient for holes β; α increased with temperature whereas β did not (figure 6). (Note that the impact ionization coefficients for both holes and electrons in cubic semiconductors drop as the temperature increases due to inelastic scattering by optical phonons.) Such a unipolar character of impact ionization is ascribed to the conduction band splitting into a number of narrow subbands. The effect is produced by the crystal potential of a superlattice naturally occurring in α-SiC polytypes along the C-axis. As a result, heating of electrons in the narrow allowed subbands is inhibited, to be resumed only at temperatures high enough for the elastic carrier scattering by phonons to become important. The proposed model is supported by the observation that the anomalies do not appear at the electric field orientation $E \perp C$. In this case impact ionization is a bipolar process; the breakdown field is 2–3 times lower and the temperature coefficient of the breakdown voltage turns out to be positive.

Strelchuk *et al* [78, 100] studied the current–voltage characteristics of 6H α-SiC p^+–n junctions prepared by sublimation and liquid-phase epitaxy, as well as by ion implantation, in a wide temperature range from 300 to 800 K. Because of the wide bandgap of 6H α-SiC, the pre-breakdown current at room temperature was negligible. For example, in implanted diodes with a breakdown voltage of 300 V [78] noticeable reverse current, 10^{-9} A, appeared only at temperatures above 600 K (figure 7(*a*)). It was concluded from the voltage and temperature variation of the reverse current that the current was due to thermal carrier generation in the space-charge region via a deep level at the middle of the bandgap. The effective lifetime of non-equilibrium charge carriers was 10^{-9}–10^{-8} s. The forward current–voltage characteristics of p^+–n junctions with a donor concentration of $(5\text{–}10)\times10^{16}$ cm^{-3} could be described as a sum of thermal injection current components: $J = J_0 \exp(qV/nkT)$, where n is constant over several orders of magnitude of current values. The component dominating at current densities up to 10^{-5}–10^{-2} A cm^{-2} (in different structures) had $n = 2$ and was due to recombination via a deep level near the mid-gap, as described by the Saah–Noyce–Shockley model. At higher current densities the components with fractional n values between 1 and 2 (3/2 or 6/5 [100])

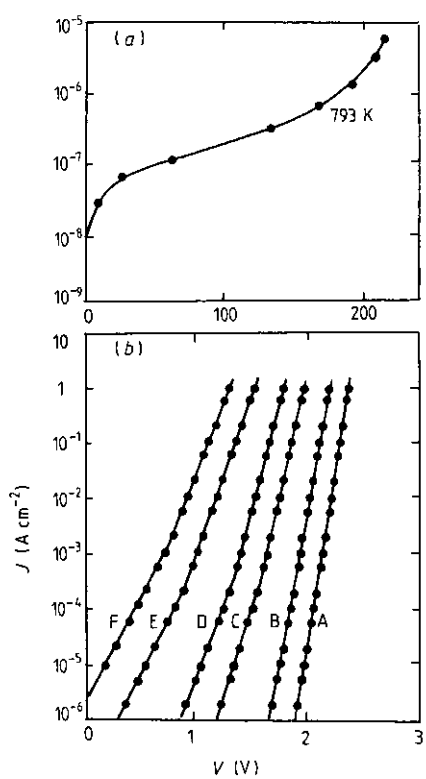

Figure 7. Reverse (*a*) and forward (*b*) current–voltage characteristics of a 6H α-SiC p^+–n diode: (A) 300 K, (B) 380 K, (C) 485 K, (D) 580 K, (E) 687 K, (F) 785 K [78].

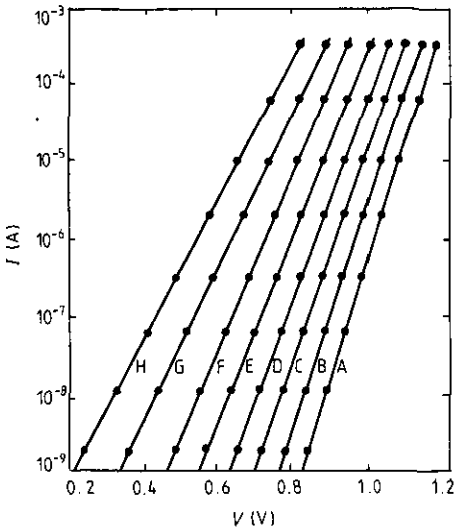

Figure 8. Forward current–voltage characteristics of a Au/6H α-SiC Schottky diode: (A) 293 K, (B) 317 K, (C) 340 K, (D) 373 K, (E) 395 K, (F) 423 K, (G) 473 K, (H) 523 K [84].

take over (see figure 7(*b*)). The pre-exponential factor J_0 had an activation-type dependence on temperature, with the activation energy (E_a) approximately equal to the bandgap value divided by n. Thermal injection currents with fractional values of n are ascribed to the carrier recombination in the space-charge region involving multivalent centres [101]. For these recombination centres, having several shallow (thermalized) levels and one deep level, $n = (m+1)/m$, where m is the total number of the levels. The energy E_a can be expressed as $E_a = [E_{g0} - (2-n)\,\Delta E]/n$, where E_{g0} is the bandgap value extrapolated to $T = 0$ K and ΔE is the average depth of the shallow levels. Note that for $m = 1$ (a single deep level) the above formula gives $n = 2$ and $E_a = E_{g0}/2$, which is consistent with the Saah–Noyce–Shockley recombination model. Measurement of the current–voltage characteristics of 6H α-SiC p^+–n junctions showed no currents due to diffusion or recombination in the quasi-neutral n-region, for which $n = 1$. In LPE-grown diodes the current component with $n = 6/5$ extends up to a current density of 10^2 A cm^{-2}, as implied by the measured dependence of the violet electroluminescence intensity on the current in a current range where the diode series resistance dominates. This observation is important for estimating the current gain that can be achieved in bipolar transistors.

Studies of Au/6H α-SiC Schottky diodes in the temperature range 300–600 K [84] show that they are close to those to be expected for an ideal SiC Schottky diode. The avalanche breakdown voltage of 170 V corresponds to an electric field strength of 2.3×10^6 V cm^{-1} (donor concentration 1×10^{17} cm^{-3}). In some structures, the current density prior to the breakdown was less than 10^{-10} A cm^{-2} (low dark currents are essential for obtaining high detectivity in Schottky photodiodes). The forward current–voltage characteristics of Schottky diodes could be described in terms of the model of thermal electron emission if account were taken of the effect of image forces on the potential barrier height (figure 8). The measured values of the ideality factor $n = 1.05 \pm 0.02$ were nearly identical to those calculated for structures with a donor concentration of 1×10^{17} cm^{-3} and a potential barrier height of 1.6 eV ($T = 300$ K).

Edmond *et al* [81] and Avila *et al* [80] fabricated p–n diodes in β-SiC using ion implantation. Although their n^+–p and p^+–n diodes retained rectifying properties up to 673 K, the devices possessed characteristics which could not be satisfactorily explained in terms of the above current mechanisms for 6H α-SiC diodes. In particular, semi-logarithmic plots of the forward current versus the voltage showed the ideality factor $n > 2$, which depended both on current and temperature [81]. The I–V characteristics plotted on a log–log scale consisted of several linear portions with slopes corresponding to the n values ranging from 1 to 2. The reverse current of the diodes revealed a power-law dependence on voltage, with a component resulting from thermal generation of carriers within the space-charge region ($J \sim V^{1/2}$) observable only at bias voltages less than 0.1 V. To explain the observed current–voltage characteristics, a model of space-charge limited currents was invoked and the presence of high concentrations of shallow and deep traps was assumed.

So far, a high density of defects in β-SiC has prevented fabrication of high quality Schottky diodes, i.e. without an intermediate layer at the metal/β-SiC interface. The barrier height, reverse current and ideality factor of Au/β-SiC [85] and Pt/β-SiC [86] Schottky diodes were dependent on the heat treatment conditions. So, the barrier height increased and the ideality factor decreased, though remaining definitely larger than unity.

Thus, at present 6H α-SiC rectifier diodes possess much better characteristics than β-SiC diodes. For 6H α-SiC p^+–n diodes, some outstanding results have been obtained: the reverse voltage up to 1.5 kV, the forward current density 10^3 A cm^{-2} at bias voltages of about 3 V and the operating temperature 500–600 °C.

4.2. Field-effect transistors

Interest in SiC field-effect transistors, as a type of device in which drift is important, is due to high values of the avalanche breakdown field and to high saturation values of the electron drift velocity in silicon carbide. All the classical types of field-effect transistor have already been demonstrated in SiC: depletion-mode MESFETs [102, 106], JFETs [104, 106, 107–111, 116] and MOSFETs [112–114]; normally-off MOSFETs (inversion-type) [106, 113–115, 119] and JFET [117]. The electrical parameters of FETs (transconductance, gate and drain leakage currents, breakdown voltage) are very sensitive to the presence of various structural defects, and therefore they are considered good indicators of the quality of SiC structures fabricated by different technologies.

In n-channel depletion-mode FETs, the drain current is controlled by varying the space-charge region width

within the n layer with a gate potential. The characteristics of SiC structures with a potential barrier for electrons can be described in terms of a full depletion model; therefore deep conductivity modulation of thin epitaxial silicon carbide layers is possible. The first MESFET in 6H α-SiC with an epitaxial n-channel was demonstrated by Muench [102]. At that time, the transistor had a fairly high transconductance (1.7 mS mm^{-1}), but the technology used was rather complicated. A channel thickness of less than 1 μm was obtained by mechanical polishing of the epitaxial layer, and the transistor insulation from the substrate was achieved with gas etching at 1300 °C.

Great expectations were associated with the technology for fabrication of heteroepitaxial β-SiC/Si structures that we described above. Research along these lines by Yoshida *et al* [103, 112], Kong *et al* [104, 105] and Furukawa *et al* [110] has shown that these hopes could not entirely come true: the electrical characteristics of the transistors produced were, on the average, inferior to those of Muench's transistor. The best device had a transconductance of 0.64 mS mm^{-1} and low drain–source voltage of 5–8 V [4]. The poor performance was attributed by the authors to a high density of defects in β-SiC/Si structures. The defects lowered the electron mobility, caused drain and source leakage and drastically reduced the breakdown voltage. The characteristics of β-SiC n-channel transistors were improved by Palmour *et al* [113] and Kelner *et al* [111] who used 6H α-SiC substrates for β-SiC growth. A transistor fabricated by Palmour *et al* [113] could operate satisfactorily up to 923 K, a maximum value for solid-state active devices of any type. To improve the characteristics of FETs, Ivanov *et al* [107, 109] concentrated their efforts on developing JFETs in 6H α-SiC because of the large avalanche breakdown field in 6H α-SiC p$^+$–n junctions.

For a depletion-mode FET, maximum transconductance (g_m) per unit channel width (Z) is given by the formula $g_m/Z = \varepsilon_s \mu E_b/L$ (ε_s is the dielectric constant, L is the channel length) [109]. It is worth noting that it has become common practice to assess a FET's quality by taking into consideration only two parameters, the electron mobility μ and the gate length L, because silicon and gallium arsenide have close values of the avalanche breakdown field ($E_b \simeq 4 \times 10^5$ V cm^{-1}). Yet, one can see from the above relationship that a low electron mobility in a properly designed SiC FET can be compensated by a high avalanche breakdown field. An important condition here is to maintain the optimum product of the donor concentration and the channel thickness $(Na)_{opt} = \varepsilon_s E_p^{opt}/q$, where $E_p^{opt} = E_b/\sqrt{3}$, so that at lower donor concentration N, the channel thickness could be appropriately reduced, and vice versa. Large thicknesses result in higher channel pinch-off voltages: $V_p = E_p a/2$. Large values of V_p are, in general, undesirable because they lead to higher input power; therefore, for SiC FETs it is reasonable to assume $V_p < 30$ V. Then, at $E_b = 5 \times 10^6$ V cm^{-1}, one obtains $a < 0.2$ μm and $N > 6 \times 10^{17}$ cm^{-3}. Further

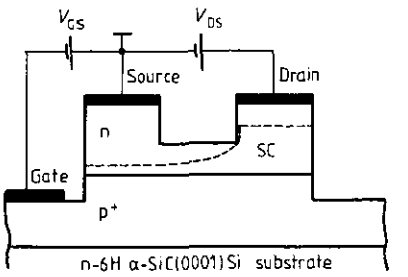

Figure 9. Schematic cross section of a 6H α-SiC JFET with buried p$^+$–n junction as a gate. The space charge (sc) region is shown in the saturated drain–current regime [108].

increase of the donor concentration with the aim of lowering the pinch-off voltage makes little sense, because in order to maintain the optimum gate length-to-channel thickness ratio defined as $L/a \simeq 3$, the gate length should be reduced below 0.5 μm, which is comparable with the resolution achievable in the commercial lithographic process. The above reasoning makes it clear that the SiC advantage of high avalanche breakdown field can be most fully exploited in power transistors operating at drain voltages of the order of 100 V.

6H α-SiC JFETs fabricated by Ivanov *et al* [108, 109] comprised p$^+$- and n-layers grown on 6H α-SiC (0001)Si Lely substrates. The channel was formed in the n-layer by etching to a required depth between the drain and source ohmic contacts (figure 9). A uniform electric field in the depletion region of the p$^+$–n junction was directed along the C crystal axis. This is important because the breakdown field in α-SiC is orientation-dependent and it is maximal just in this direction. The ohmic contacts to the source, the drain and the gate were made using metallization with Al/W. Insulation of the transistor channels from the substrate and thinning of the n-layer in the source–drain spacing were performed using low-temperature reactive ion etching with SF_6 plasma. The electrical characteristics of the transistors were as follows. The electrical breakdown of the p$^+$–n junction in the drain–gate region is a microplasma process caused by impact ionization in the semiconductor bulk. At breakdown, the electric field is close to the limiting value for 6H α-SiC (3×10^6 V cm^{-1}). The donor density per unit channel area $Na = 1 \times 10^{13}$ cm^{-2} ($N = 4 \times 10^{17}$ cm^{-3}, $a = 0.25$ μm) corresponds to $E_p = 1.6 \times 10^6$ V cm^{-1}. Because of a fairly high doping level in the channel, the pinch-off voltage of 17 V was obtained. The output characteristics prior to the drain–gate breakdown (figure 10) in a wide temperature range of 300–700 K agree with the Shockley model [118]: the drain current I_D shows complete saturation at the drain–source voltages $V_{DS} > |V_T| - |V_{GS}|$ (V_T is the gate threshold voltage) and the transconductance in the saturation region of the drain current is equal to the channel conductance G_{DS} observed at small V_{DS}. At room temperature, transistors with a channel length $L = 10$ μm and threshold voltage $V_T = -14.5$ V show the following electrical parameters: maximum drain current 50 mA mm^{-1}, maximum transconductance

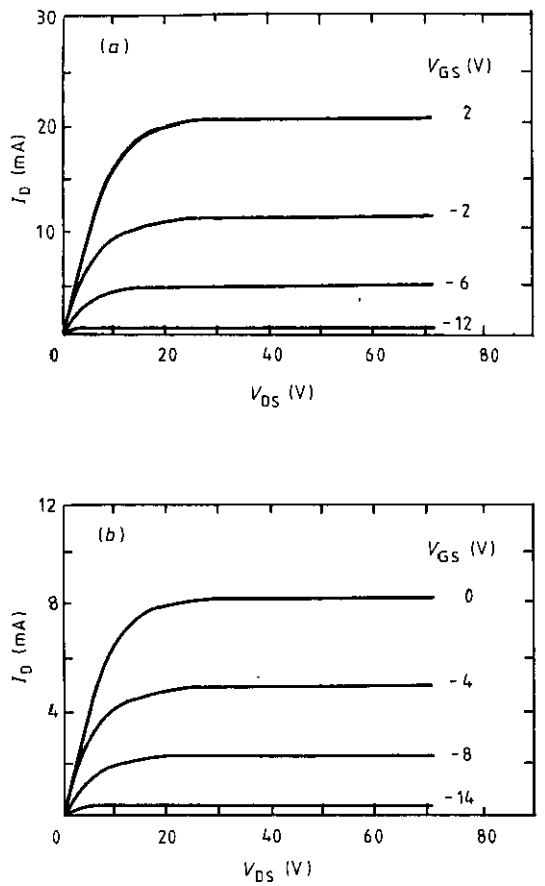

Figure 10. Drain current–voltage characteristics of a 6H α-SiC JFET at 300 K (*a*) and 700 K (*b*) [108, 109]. The gate length and width are 10 μm and 400 μm, respectively.

7.2 mS mm^{-1}, maximum drain–gate voltage 100 V, maximum switch power 2.5 W mm^{-1}. It was found in studies of the channel conductance in the temperature range 160–700 K that the electron drift mobility at room temperature equalled 180 cm^2 V^{-1}s^{-1} and varied with temperature as $\mu = 180(T/300)^{-2.4}$ cm^2 V^{-1}s^{-1}. The free electron concentration at $T = 300$ K amounted to 40% of the donor concentration and varied with temperature according to the statistics for a partially compensated non-degenerate semiconductor having the following parameters: the donor ionization energy $E_D = 100$ meV, the effective density of states in the conduction band $N_c = 6.8 \times 10^{18}(T/300)^{3/2}$ cm^{-3}, the degree of donor compensation 10%.

Good prospects for the proposed approach to designing SiC FETs are illustrated in figure 11, which shows a year-to-year progress in transconductance of depletion-mode transistors fabricated by different technologies. The parameter used for transistor estimation is the transconductance of a transistor with a gate 1 mm wide and 1 μm long. Analogous transistors made by Kelner *et al* [116] and by Palmour *et al* [106] had transconductance values three times larger in the above 6H α-SiC JFETs, due to a larger pinch-off voltage and shorter channel length.

Two types of normally-off FET are known: MOSFETs of the inversion-type and JFETs or MESFETs in which the depletion region traverses the entire channel thickness

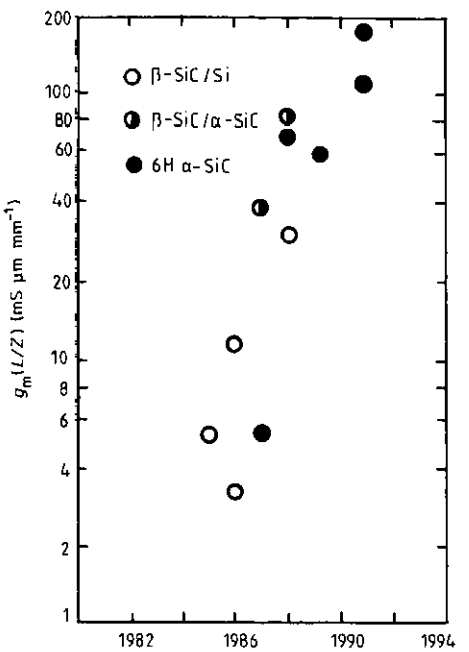

Figure 11. Progress in depletion-mode SiC FETs.

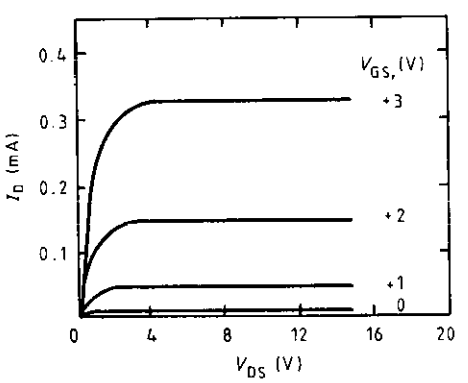

Figure 12. Drain current–voltage characteristics of a 6H α-SiC normally-off JFET at 300 K [117]. The gate length and width are 10 μm and 400 μm, respectively.

even at zero bias. SiC MOSFETs of the inversion type were fabricated in both β-SiC and 6H α-SiC. Their transconductance was less by about an order of magnitude than in normally-on transistors because of a lower electron mobility in the surface inversion layer compared with the bulk mobility and because of non-zero (positive) threshold gate voltage. The threshold voltage is influenced by various factors: (i) doping level in the p substrate and the oxide layer thickness [119]; (ii) the density of states at SiO_2/SiC interface [106]; (iii) gate length [113], and (iv) temperature [106, 113]. For example, an inversion-type n-channel MOSFET in 6H α-SiC [106] had a room-temperature threshold voltage of +3.6 V, dropping to less than +1 V at elevated temperatures.

Normally-off JFETs and MESFETs may have some advantages over MOSFETs, whose characteristics are related to the minority charge carriers in the surface inversion layer. Indeed, the performance of these devices

depends on the bulk mobility of the majority carriers, whereas the threshold voltage can be easily reduced to zero by adjusting the channel thickness. A prototype normally-off 6H α-SiC transistor fabricated by Ivanov *et al* [117] has a design similar to a normally-on transistor [107] except that the channel is totally traversed by the space-charge region at zero gate bias. The output characteristics of the transistor (figure 12) were well saturated up to the gate potential of +3 V. The threshold voltage was near to zero. At donor concentration $8 \times 10^{17}\,\mathrm{cm}^{-3}$ this corresponded to a channel width of about 60 nm. Maximum transconductance at room temperature was $0.5\,\mathrm{mS\,mm}^{-1}$. Note that this value is larger than in β-SiC MOSFETs at the same gate voltage.

4.3. Bipolar transistors and dinistor

As in other semiconductors with an indirect energy band structure, recombination of non-equilibrium charge carriers in silicon carbide occurs predominantly in a radiationless way. Recombination of electrons and holes involves centres which have energy levels within the bandgap and are thus capable of capturing charge carriers. The nature of the major radiationless recombination centres in silicon carbide still remains unclear. The concentration and capture cross sections for these centres are such that the lifetimes do not exceed 10^{-8} s even in the purest SiC samples. Small lifetimes set severe limitations on the performance of such injection devices as bipolar transistors and thyristors. Bipolar SiC devices were considered in detail by Chelnokov [122]. By way of example, let us estimate a possible base current gain of a 6H α-SiC bipolar transistor with hole injection into the n-base, taking into account the losses due to recombination in the base region and in the space-charge region (SCR) of the emitter p^+–n junction.

Recall that the recombination currents within the SCR in forward-biased p^+–n junctions with a long base ($W \gg L_p$) dominate up to the current densities $10^2\ \mathrm{A\,cm}^{-2}$: $J_r = J_{r0}\exp(qV/nkT)$, where $n > 1$ (see subsection 4.1). The currents due to diffusion and recombination in the quasi-neutral regions, $J_d \sim \exp(qV/kT)$, have not yet been detected. If recombination occurs in the SCR, the base current gain depends on the collector current density (J_C): $\beta_F^{-1} = (\beta_F')^{-1} + J_r/J_C$. In this expression β_F' is the gain in the absence of recombination within the SCR ($J_r = 0$). Because the hole diffusion length in the n-base (L_p) does not exceed 1.5 μm at room temperature [120], the base thickness (W) should be about 0.9 μm in order to obtain a gain $\beta_F' = 5$. The second term in the expression for β_F, which accounts for recombination in the SCR of the emitter junction, can be written in the form

$$J_r/J_C = (J_{r0}/J_{C0})\,(p(0)/p_n)^{1/n-1}.$$

Here

$$J_{r0} = (q\,D_p\,p_n/L_p)\sinh(W/L_p)$$
$$p(0) = p_n\exp(qV_{BE}/kT)$$

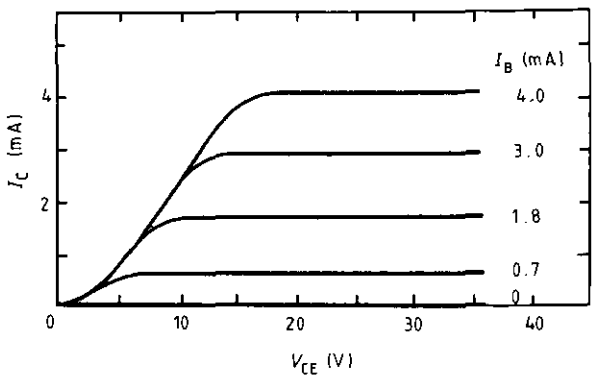

Figure 13. Collector current–voltage characteristics of a 6H α-SiC n^+–p–n bipolar transistor at 600 K [122].

where V_{BE} is a base–emitter voltage. Assuming that the density of injected holes $p(0)$ is equal to the base electron concentration n_n and recalling that $p_n = n_i^2/n_n$, one obtains an expression for the base current gain β_F

$$\beta_F^{-1} = \cosh(W/L_p) - 1 + (J_{r0}\,L_p\,n_n/q\,D_p\,n_i^2)(n_n/n_i)^{2/n-2}\sinh(W/L_p).$$

To our knowledge, the best 6H α-SiC p^+–n junctions have $J_{r0} = 10^{-37}\,\mathrm{A\,cm}^{-2}$ at room temperature, and $n = 6/5$ [100]. Taking the hole diffusion coefficient $D_p = 0.5\,\mathrm{cm}^2\,\mathrm{s}^{-1}$, the diffusion length $L_p = 1.5$ μm, the base electron concentration $n_n = 5 \times 10^{16}\,\mathrm{cm}^{-3}$ and the intrinsic carrier concentration $n_i = 10^{-6}\,\mathrm{cm}^{-3}$, one obtains a base thickness value of 0.6 μm from the above formula at $\beta_F = 5$.

An experimental 6H α-SiC n^+–p–n^+ bipolar transistor fabricated by Muench [121] showed a gain $\beta_F = 4$ with collector current 0.8 mA and base thickness 0.8 μm at room temperature. To fabricate a bipolar transistor and the first dinistor, Chelnokov [122] and Dmitriev *et al* [123] used multilayer p–n structures grown in a single LPE run. The bipolar transitor comprised an n-collector with the donor concentration $\sim 10^{17}\,\mathrm{cm}^{-3}$, a p-base with the acceptor concentration $\sim 10^{18}\,\mathrm{cm}^{-3}$, and an n^+-emitter with the donor concentration $> 10^{19}\,\mathrm{cm}^{-3}$. Studies of its electrical parameters at room temperature showed that the series resistance of the emitter–base junction (with the collector circuit open) was very large. This was due to high resistivity (about 20 Ω cm) of the p-layer. As a result, the emitter–base voltage required for attaining an intermediate injection level ($n(0) = p_p$) was less than the maximum collector–base voltage only at elevated temperatures, when the base resistivity decreased due to ionization of the acceptors. The collector current in a common-emitter circuit saturated at 15 V and was equal to 4 mA at 600 K; the differential base current gain in these conditions was $\beta_F = 1.2$ (figure 13). The influence of recombination current in the SCR of the emitter junction is illustrated in figure 14, where the dependence of the base current gain on the collector current is shown for different temperatures.

The dinistor consisted of a p^+-emitter with acceptor concentration $> 10^{19}\,\mathrm{cm}^{-3}$, an n-base (about 1 μm

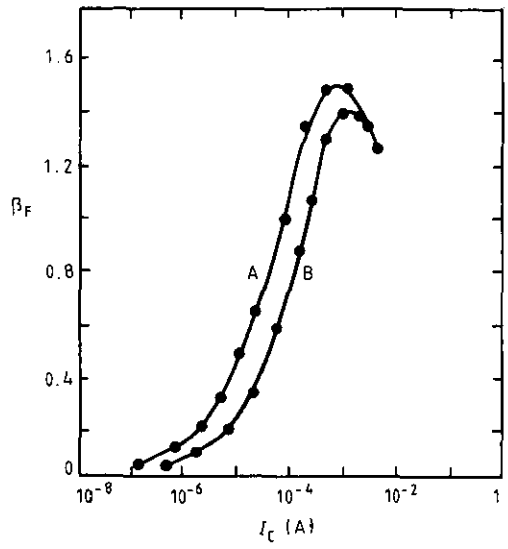

Figure 14. *Base current gain versus collector current:* (A) 500 K, (B) 600 K.

thick) with donor concentration $5 \times 10^{17}\,cm^{-3}$, a p-base about 3 μm thick with acceptor concentration $3 \times 10^{18}\,cm^{-3}$, and an n^+-emitter doped with donors to 10^{19}–$10^{20}\,cm^{-3}$. The voltage required to switch the dinistor into the on-state varied for different structures in the range 10–50 V; the switching current density was 3–10 $A\,cm^{-2}$ (figure 15). The reverse voltage was as high as 90–100 V. The current density required to hold the on-state and supported by a switched-on region of about 10 μm in diameter was estimated to be 10^2–10^3 $A\,cm^{-2}$. The respective holding voltage was close to the value of the built-in potential of the SiC p–n junction. The turn-on time of the dinistor (τ_{on}) after application of a dV/dt signal was 1–10 ns, depending on the amplitude of the voltage pulse applied to the structure. The current rise time determined by the propagation rate of the on-state was 10–40 ns. A diffusion model of the dinistor switching gives, for the turn-on time, an expression $\tau_{on} = (\theta_n \theta_p)^{1/2}$, where $\theta_p = W_n^2/2D_p$, $\theta_n = W_p^2/2D_n$ are diffusion times of minority carriers in the n- and p-regions, respectively. For $W_n = 1$ μm, $W_p = 3$ μm, $D_n = 2.5\,cm^2\,s^{-1}$ and $D_p = 0.25$ $cm^2\,s^{-1}$ the calculated turn-on time was 10^{-8} s, in agreement with experimental values. The switching time into the off-state (τ_{off}) varied between 150 and 200 ns, depending on the current prior to the turn-off. The hole lifetime in the lightly doped n-base calculated from τ_{off} was about 40 ns, which agrees with the hole diffusion length $L_p = 1$ μm and the hole diffusion coefficient $D_p = 0.25$ $cm^2\,s^{-1}$.

4.4. Short-wave light-emitting diodes

A large number of luminescence bands have been identified in silicon carbide; among them are the bands for (i) luminescence involving activating impurities and intrinsic structural defects, (ii) luminescence due to free and bound excitons, and (iii) pre-breakdown emission. Due to the above mechanisms of radiative recombination, the luminescence of various SiC polytypes covers

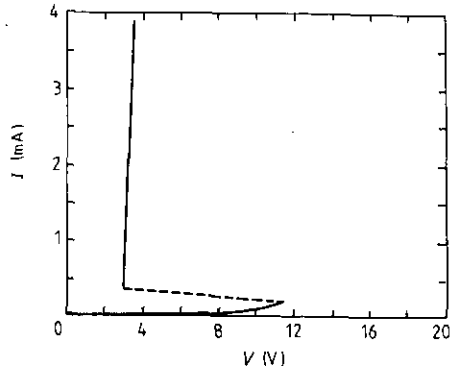

Figure 15. Switching current–voltage characteristic of a 6H α-SiC dinistor at room temperature [123].

nearly all of the visible spectrum as well as the near ultraviolet region [124]. In view of the fact that effective injection light-emitting diodes (LED) based on III–V semiconductors have been designed for the long-wave range of the visible spectrum (640–555 nm), our consideration will be restricted to the short-wave (540–420 nm) range, where injection SiC LEDs have no rivals.

Table 4 gives the characteristics of these LEDs for various luminescence bands: external quantum efficiency, emitted power, luminescence intensity, spectral range and monochromaticity, as well as operating parameters (currents and voltages). Purely green (520–530 nm) LEDs will have to be designed because the injection luminescence of III–V semiconductors does not extend to waves shorter than the yellow–green boundary of about 555 nm (GaP LEDs). Purely green 6H α-SiC LEDs with $\lambda_{max} = 530$ nm were fabricated by implantation of Al into n-type crystals [125] and by the LPE process [126]. The luminescence mechanism in LEDs of this group is considered to be related to the presence of intrinsic point defects of the vacancy type D1 in silicon carbide. These stable defects are thought to be due to deviations from the stoichiometry arising during the growth and/or under the bombardment with high energy particles. The green electroluminescence band is slightly affected by the current and the light intensity: the current characteristic tends to saturate with rising current density [126]. Apart from the luminescence related to the D1 centres in 6H α-SiC, green emission with $\lambda_{max} = 520$–530 nm was registered from 4H α-SiC p–n junctions due to the donor–acceptor recombination between boron–nitrogen pairs [127, 128].

Blue 6H α-SiC LEDs emitting in the spectral range 460–480 nm have been prepared by sublimation [128], liquid-phase epitaxy [129, 131] and chemical vapour deposition [130]. The injection electroluminescence mechanism in this group of LEDs is a donor–acceptor one involving aluminium–nitrogen and gallium–nitrogen pairs as well as the band-to-impurity recombination. The most efficient LEDs with purely blue emission at $\lambda = 470$ nm ($T = 300$ K) were obtained using LPE-grown 6H α-SiC p–n structures by introducing an acceptor impurity in the growth process to overcompensate the donors [131]. These blue LEDs have a fairly wide emission band ($\Delta\lambda = 60$–70 nm), its spectral shape

Table 4. SiC short-wave light-emitting diodes.

	Green		Blue		Violet
Peak wavelength (nm)	538	530	470	470	423
Spectral bandwidth (nm)	20	15	70	70	20
Quantum efficiency $\times 10^4$	—	—	1	—	0.5
Luminescence Intensity (mcd)	100	9	2	7-8	0.15
Power (μW)	100	2.6	—	—	—
Current (mA)	200	20	20	20	20
Voltage (V)	6–8	3.6	3.4	—	3.8
Beam angle (deg)	37	12	12	—	15
Reference	[125]	[126]	[129]	[131]	[133]

and peak position varying weakly with the current density. The emission intensity was practically linear in current [129]. The quantum efficiency of the LEDs increased with increasing number of donors and acceptors due to a faster rise of concentration of the close donor–acceptor pairs. Apart from 6H α-SiC (donor–acceptor band), blue emission with $\lambda_{max} = 480$ nm was obtained from 4H α-SiC p–n junctions (luminescence due to D1 centres [125, 128]).

Radiative annihilation of free excitons has been observed in various SiC polytypes. In LPE-grown 6H α-SiC p–n structures the free exciton electroluminescence is located in the violet ($\lambda_{max} = 425$ nm at $T = 300$ K [132]). The intensity of this luminescence band increases at lower concentrations of compensating impurities and with rising temperature. The highest room-temperature quantum efficiency of the violet electroluminescence is found in 4H α-SiC LEDs prepared by sublimation [128] or liquid-phase epitaxy [133, 134]. The donor–acceptor band of these LEDs has a peak in the violet ($\lambda_{max} = 423$ nm) because of the wider bandgap of 4H α-SiC. Note that the exciton luminescence spreads out into the near ultraviolet. It is seen from table 4 that the short-wave α-SiC LEDs have already reached the level of performance acceptable for commercial production and it might be considered that semiconductor LEDs have met the challenge of expanding throughout the entire visible spectrum.

4.5. Ultraviolet photodiodes

6H α-SiC is one of the most promising materials for semiconductor photodetectors sensitive to ultraviolet (UV) radiation. The large bandgap value makes 6H α-SiC UV photodetectors highly selective. Their sensitivity is sufficiently high over the wavelength range 200–400 nm, with the absorption depth of light varying in this range from 0.1 to 1000 μm. This photosensitivity range permits detection of UV signals against the background radiation from red-hot bodies. The peak position and shape of the photosensitivity spectrum can be controlled by changing the depletion region width where separation of non-equilibrium photogenerated carriers takes place. Owing to extremely small dark currents

Table 5. 6H α-SiC ultraviolet photodiodes.

Type	n^+–p		Au/n	n–p^+
Reference	[137]	[138]	[136]	[136]
Peak wavelength (nm)	280	270	215	225
Quantum efficiency	0.75	0.70	0.80	0.7
Current sensitivity (A W^{-1})	—	0.15	0.15	0.13

(less than 10^{-10} Acm^{-2}) and low noise in 6H α-SiC p–n junctions and Schottky barriers, their detectivity at room temperature can reach 10^{-14}–10^{-13} W $Hz^{-1/2}$ Furthermore, the high resistance of silicon carbide to irradiation makes possible operation at incident radiation power as high as 10^3–10^4 Wcm^{-2}.

In 6H α-SiC UV photodiodes demonstrated so far, use has been made of either semi-transparent Schottky barriers, Cr/SiC [135] and Au/SiC [136], or of shallow p–n junctions: implantation-doped [137] or epitaxial n^+–p junctions [138] and epitaxial n–p^+ junctions [136]. The photosensitivity spectra and other parameters of photodetectors fabricated by different techniques (see table 5) depend on the depth of the region where the photocarrier separation occurs. In the temperature range 295–673 K the long wavelength boundary of the photosensitivity band shifts between 400 and 450 nm in correspondence with the linear temperature variation of the bandgap [137].

5. Development prospects

5.1. Power microwave devices

Silicon carbide is often mentioned as a material possessing a unique combination of properties for power microwave applications. This opinion is based on the figures of merit (FM) of semiconductors proposed by Johnson (JFM) [139] and Keyes (KFM) [140], for microwave devices where drift is important. JFM gives an estimate of electrical limitations of the output power (P) at a cut-off frequency (f_T): $P f_T^2 X_C = E_b^2 v_s^2/4\pi^2$, $f_T = 1/2\pi\tau$. Here τ is the carrier transit time through the drift region of a device, X_C is the device impedance, E_b is the avalanche breakdown field and v_s the saturated drift velocity of carriers. KFM, on the other hand, defines thermal limitations of the output power at the cut-off frequency: $P f_T = \kappa(c v_s \varepsilon_0/4\pi\varepsilon_s)^{1/2}\Delta T$, where c is the velocity of light, κ is the semiconductor thermal conductivity, ΔT is an admissible temperature difference between the heat sink and the active region of the device, ε_0 is the dielectric constant in vacuum, ε_s is the dielectric constant of the semiconductor. It is readily seen that high values of E_b, v_s, κ and ΔT make silicon carbide much superior to silicon and gallium arsenide in terms of JFM and KFM. It should be remembered that these FMs refer to idealized two-terminal devices of circular cross section. The idealized device is most closely approached by a BARITT metal–semiconductor–metal diode. The device operates in a punch-through regime:

a forward-biased Schottky diode injects minority carriers directly into the high-field drift region produced by the space charge of the reverse-biased Schottky contact. The charge carriers in a BARITT diode drift at a saturation velocity practically over its entire length (L), so that the transit time is defined simply as $\tau = L/v_s$. In other drift devices for microwave generation and amplification, such as avalanche injection diodes, field-effect and bipolar transistors, the role of saturation drift velocity, though fairly important, is not exclusive. The fact is that in these drift devices there are low-field regions where the carrier velocity is determined by their low-field mobility. This may affect the upper frequency limit and output power of the device. This case has been treated by Tager [141] and Shenai *et al* [142], who have proposed a generalized FMS account for both electrical and thermal limitations on the output power of microwave devices at a specified frequency.

Consider in more detail the electrical limitations on the output power of a planar 6H α-SiC MESFET [143], which is likely to become one of the first microwave devices to be produced in silicon carbide. A characteristic feature of the field-effect transistor is the existence of a feedback between the distribution of the electric drift field under the gate and the electron current in the channel. According to a model by Pucel *et al* [144], part of the channel cross section under the gate is a low-field region where the electrons are accelerated up to a saturation velocity. With rising drain potential V_{DS}, the drain current I_D increases due to increasing dimensions of the part of the channel cross section where the electron velocity is saturated. At $V_{DS} = V_p$ (which is of practical interest for calculation of the drain current I_D), two extreme situations are possible: (i) the length and the thickness of the region where the electron velocity is saturated are very small, so that the maximum drain current can be calculated using the well known Shockley model [145]:

$$I_D = \tfrac{1}{3}qNa\mu(V_p/L)Z = \tfrac{1}{2}qNa\tilde{v}Z$$

where N is the donor concentration equal to the free electron density, $V_p = qNa^2/2\varepsilon_s$ is the channel pinch-off voltage, $\tilde{v} = \frac{1}{3}\mu E_p(a/L)$ is the electron drift velocity averaged over the gate length; (ii) the region of saturation velocity occupies practically the whole of the channel cross section under the gate, so that the drain current is at its maximum $I_D^{max} = qNav_sZ$.

According to [143], case (i) takes place if the relative channel length satisfies the inequality $L/a > \mu E_p/v_s$, where $E_p = 2V_p/a$. It is seen that the mean drift velocity is $\tilde{v} < v_s/3$. Case (ii), when $v = v_s$, occurs if $L/a < (2/\pi)\text{arcsinh}(\pi\mu E_p/4v_s)$. If the donor concentration N and the channel thickness a are chosen in such a way that the pinch-off voltage equals its optimal value $V_p = V_b/3$ (V_b is a breakdown voltage), then the transistor output power ($P = I_DV_p/16$) will be related to the cut-off frequency by $Pf_TX_C = (1/288\pi)\mu E_b^2V_p$ and $Pf_T^2X_C = (1/192\pi^2)E_b^2v_s^2$ for cases (i) and (ii) respectively.

For an optimally designed 6H α-SiC MESFET with $V_p = 20$ V, $N = 1 \times 10^{18}\,\text{cm}^{-3}$, $a = 0.1\,\mu$m and $\mu = 100\,\text{cm}^2\,\text{V}^{-1}\text{s}^{-1}$, the power calculated with the above relationships for the frequency range 10–100 GHz would be from 100 to 7 W. This is considerably lower than the power given by JFM for an idealized microwave device (figure 16(*a*)). It should be remarked that there are no reasons to expect that better power–frequency characteristics could be obtained for transistors in β-SiC, which feature higher electron mobility than 6H α-SiC. The point is that the major parameter of power FETs is not the electron mobility μ but the product μE_b which has the dimension of velocity. Experimental data on the magnitude of the field E_b required for inducing impact ionization in β-SiC are still lacking. It may only be surmised that this field is less than in 6H α-SiC because of a simpler energy band structure in the former. It follows from theoretical considerations of the parameters of 6H α-SiC power MESFETs at microwave frequencies that the state of complete velocity saturation in the transistor is reached at the gate lengths 0.3 μm or less (figure 16(*b*)) for pinch-off voltages less than 20 V.

There is still much to be done to produce SiC power microwave devices. In particular, one of the important problems is the preparation of high-temperature ohmic contacts. According to Shenai *et al* [142], the maximum conductivity of a microwave device in the on-state is given by $\sigma_{on} = \varepsilon_s\mu E_b^3/4V_b^2$. Hence, the resistivity of an ohmic contact should be as low as $\rho_c < 0.1\,\sigma_{on}^{-1}$. Let the minimum breakdown voltage be $V_b = 100$ V, then for $E_b = 4 \times 10^6$ V cm^{-1} and $\mu = 100$ cm^2 V^{-1} s^{-1} one obtains $\rho_c < 6 \times 10^{-6}\,\Omega\,\text{cm}^2$, whereas at present the lowest resistivity of ohmic contacts to both n- and p-SiC is $10^{-4}\,\Omega\,\text{cm}^2$.

5.2. Integrated circuits

Successful development of the technology of large-area SiC single crystals and discrete active devices has increased interest in producing high-temperature, radiation-resistant digital integrated circuits (IC) in SiC. Methods currently used for fabrication of silicon and gallium arsenide ICs can be also employed.

Silicon ICs started with injection logic (DTL, TTL). However, the existence of a thermal oxide facilitated the task of designing silicon ICs based on MOS transistors (n-channel MOS logic, complementary MOS logic). The absence of a suitable under-gate insulator was an obstacle to the development of gallium arsenide MIS structures. Nonetheless, owing to the availability of semi-insulating gallium arsenide and to the developments in ion implantation and planar technologies, it has become possible to produce MESFETs that are operated on the same wafer both in the enhancement and depletion modes. These transistors were used to design circuits in which the basic logic is functionally similar to the silicon n-MOS logic. For example, an ordinary inverter is a normally-off transistor loaded on a normally-on transistor with the gate and the source short-circuited. To compare the functional characteristics of normally-off SiC

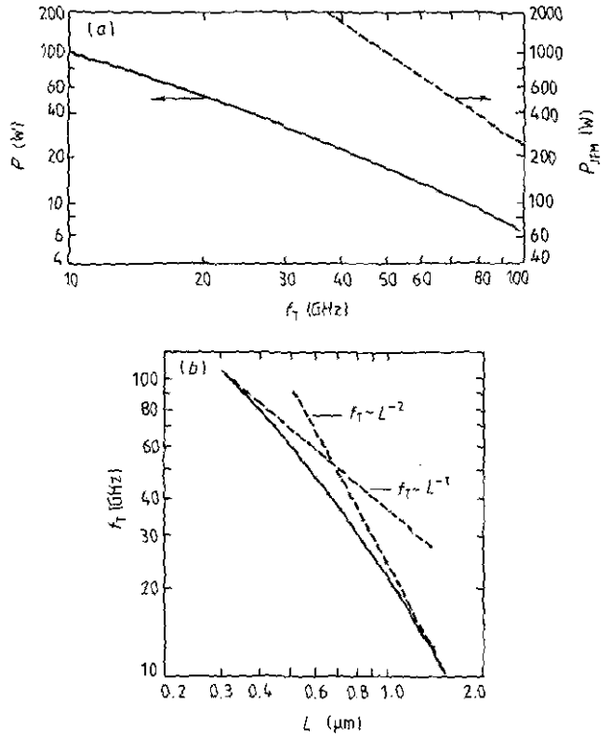

Figure 16. *Calculated high-frequency output power versus cut-off frequency (a) and cut-off frequency versus gate length (b) for a 6H α-SiC MESFET. $N = 1 \times 10^{18}$ cm^{-3} $V_p = 20$ V, $X_C = 50\ \Omega$.*

field-effect transistors, consider the transconductance of enhancement-mode FETs in its general form [145]: $dI_D^{sat}/dV_{GS} = \varepsilon_s \mu Z(V_{GS} - V_T)/dL$. Here d is the channel thickness of JFETs or MESFETs (thickness of the under-gate insulator of a MOS transistor) and V_T is the gate threshold voltage. Analysis of this relationship reveals the following advantages of JFETs or MESFETs. Firstly, the transistor operation depends on the bulk electron mobility, which is larger than in the inversion layer, where an additional scattering mechanism is effective at the oxide/semiconductor interface. Secondly, the threshold voltage of JFETs and MESFETs may be made zero by an appropriate choice of the channel thickness, whilst in MOSFETs of the inversion type the threshold voltage depends on the screening charge density, gate length and temperature. Finally, it should be taken into account that the channel thickness in JFETs or MESFETs may be close to the oxide layer thickness in MOSFETs because of the high avalanche breakdown field in silicon carbide comparable to the breakdown field strength of SiO_2. The above advantages of JFETs and MESFETs could be put to use only if the respective planar technology, so far unavailable, were developed. In this respect, MOSFETs are in a better position because their planar technology can easily borrow from the planar technology of silicon MOSFETs, e.g. the methods of forming field and under-gate oxide, the local ion-doping methods for producing source and drain regions. As shown in the present review, all techniques necessary for fabrication of the constituent elements of digital integrated circuits based on SiC MOS transistors have been fairly well developed.

6. Conclusion

Summarizing the present review, we express our conviction that silicon carbide has won an important position in semiconductor electronics: high temperature electrical devices and short-wave optoelectronic devices have no analogues among devices from other semiconductor materials. At the same time, silicon carbide has many potentialities still waiting to be used. This refers primarily to heterostructures. It should be recalled that devices with heterostructures based on III–V semiconductors opened up, at their time, a new era in semiconductor electronics. This included heterolasers, quantum-dimensional heterostructures, graded-gap structures and superlattices. With its variety of polytypes, silicon carbide presents a unique opportunity for producing hetero-polytype structures. Intensive research is already under way into β-SiC/Si heterostructures to be used as heteroemitters in bipolar transistors and as wide-gap optical windows in solar cells. Further, a continuous series of quasi-binary solid solutions of silicon carbide with aluminium nitride or gallium nitride has been found. The bandgap value of SiC–AlN solid solutions varies from 3 to 6 eV, and at an AlN content exceeding 70% there is a transition to the direct structure of the energy bands. So, there is a possibility of producing an ultraviolet semiconductor laser. Finally, one of the most exciting implications from the existence of various SiC polytypes is the occurrence of a natural superlattice in α-SiC polytypes, which means that negative differential conductance and microwave generation are possible along the C-axis.

References

[1] Lely J A 1955 *Ber. Deut. Keram. Ges.* **32** 229
[2] Tairov Yu M and Tsvetkov V F 1978 *J. Cryst. Growth* **43** 209
[3] Tairov Yu M and Tsvetkov V F 1981 *J. Cryst. Growth* **52** 146
[4] Ziegler G, Lanig P, Theis D and Weyrich C 1983 *IEEE Trans. Electr. Dev.* **ED-30** 227
[5] Nakata T, Koga K, Matsuchita Y, Ueda Y and Niina T 1989 *SPP Amorphous and Crystalline Silicon Carbide* ed M M Rahman, C-Y W Yang and G L Harris (Berlin: Springer) vol 43 p 26
[6] Barret D L, Seidensticker R G, Gaida W, Hopkins R H and Choyke W J 1991 *J. Cryst. Growth* **109** 17
[7] Vodakov Yu A, Mokhov E N, Ramm M G and Roenkov A D 1979 *Cryst. Res. Techn.* **14** 729
[8] Mokhov E N, Shulpina I L, Tregubova D S and Vodakov Yu A 1981 *Cryst. Res. Techn.* **16** 879
[9] Anikin M M, Guseva N B, Dmitriev V A and Syrkin A L 1984 *Sov. Inorg. Mat.* **20** 1768 (in Russian)
[10] Anikin M M, Dmitriev V A and Chelnokov V E 1989 *Extend. Abstr. of the 176th Meet. of the Electrochem. Soc. (Hollywood FL)* p 709

[11] Hoffman L, Ziegler G, Theis D and Weyrich C 1982 *J. Appl. Phys.* **53** 6962
[12] Suzuki A, Ikeda M, Nagao N, Matsunami H and Tanaka T 1976 *J. Appl. Phys.* **47** 4546
[13] Ikeda M, Hayakawa T, Yamagiva S, Matsunami H and Tanaka T 1979 *J. Appl. Phys.* **50** 8215
[14] Muench W and Kurzinger W 1978 *Solid State Electron.* **21** 1129
[15] Dmitriev V A, Ivanov P A, Korkin I V, Morozenko Ya V, Popov I V, Sidorova T A, Strelchuk A M and Chelnokov V E 1985 *Sov. Phys. Techn. Lett.* **11** 98 (in Russian)
[16] Dmitriev V A and Cherenkov A E 1991 *Sov. Phys. Techn. Lett.* **17** 43 (in Russian)
[17] Dmitriev V A, Kazakov S V, Tretjakov V V, Oding V G and Chernov M A 1989 *Extend. Abstr. of the 176 Meet. of the Electrochem. Soc. (Hollywood FL)* p 711
[18] Dmitriev V A, Popov I V and Chelnokov V E 1988 *Semiconductor Crystals and Film Growth Processes* ed F A Kuznetsov (Novosibirsk: Nauka) p 74 (in Russian)
[19] Nishino S, Powell J A and Will H A 1983 *Appl. Phys. Lett.* **42** 460
[20] Addamiano A and Klein P H 1984 *J. Cryst. Growth* **70** 291
[21] Liaw P and Davis R F 1985 *J. Electrochem. Soc.* **132** 642
[22] Kingon A I, Lutz L G, Liaw P and Davis R F 1983 *J. Am. Ceram. Soc.* **66** 558
[23] Fischman G S and Petuskey W T 1985 *J. Am. Ceram. Soc.* **68** 185
[24] Minagava S and Gatos H C 1971 *Japan. J. Appl. Phys.* **10** 844 and 1680
[25] Harris J M, Gatos H C and Witt A F 1971 *J. Electrochem. Soc.* **118** 335 and 338
[26] Kim H J and Davis R F 1986 *Appl. Phys. Lett.* **60** 2897
[27] Pirouz P and Chorey C M 1987 *Sov. Phys. Ser. of the Academy of Sciences* **51** 1616 (in Russian)
[28] Furumura Y, Doki M, Mieno F, Eshita T, Suzuki T and Maeda M 1988 *J. Electrochem. Soc.* **135** 1255
[29] Nishino S and Saraie J 1989 *SPP Amorphous and Crystalline Silicon Carbide* ed G L Harris and C Y-W Yang (Berlin: Springer) vol 34 p 45
Nishino S and Saraie J 1989 *SPP Amorphous and Crystalline Silicon Carbide* ed M M Rahman, C-Y W Yang and G L Harris (Berlin: Springer) vol 43 p 8
[30] Chorey C M, Pirouz P, Powell J A and Mitchel T E 1986 *Semiconductor-Based Heterojunctions: Interfacial Structure and Stability* ed M L Green *et al* (Warrendale PA: Metallurgical Soc.) p 115
[31] Nutt S R, Smith D J, Kim H J and Davis R F 1987 *Appl. Phys. Lett.* **50** 203
[32] Pirouz P, Chorey C M and Powell J A 1987 *Appl. Phys. Lett.* **50** 221
[33] Shibahara K, Nishino S and Matsunami H 1987 *Appl. Phys. Lett.* **50** 1888
[34] Powell J A, Matus L G, Kuczmarski M A, Chorey C M, Cheng T and Pirouz P 1987 *Appl. Phys. Lett.* **51** 823
[35] Pirouz P, Ernst F and Cheng T 1988 *Mat. Res. Soc. Symp. Proc.* **116** 57
[36] Shigeta M, Fujii Y, Furukawa K, Suzuki A and Nakajama S 1989 *Appl. Phys. Lett.* **55** 1522
[37] Kong H S, Glass J T and Davis R F 1986 *Appl. Phys. Lett.* **49** 1074; 1989 *J. Mat. Res. Soc.* **4** 204
[38] Powell J A, Larkin D J, Matus L G, Choyke W J, Bradshaw J L, Henderson L, Yoganathan M, Yang J and Pirouz P 1990 *Appl. Phys. Lett.* **56** 1353 and 1442
[39] Yang J and Pirouz P 1990 *Extend. Abstr. of the 176th Meet. of the Electrochem. Soc. (Hollywood FL)* p 713
[40] Kong H S, Glass J T and Davis R F 1988 *J. Appl. Phys.* **64** 2672
[41] Sugiura J, Lu W-Y, Cadien K C and Steckl A J 1986 *J. Vac. Sci. Techn.* **B4** 349
[42] Palmour J W, Davis R F, Astell-Burt P and Blackborow P 1987 *Mat. Res. Soc. Symp. Proc.* **76** 185
[43] Syrkin A L, Popov I V and Chelnokov V E 1986 *Sov. Phys. Techn. Lett.* **12** 240 (in Russian)
[44] Palmour J W, Davis R F, Wallett T M and Bhasin K B 1986 *J. Vac. Sci. Techn.* **A4** 590
[45] Dohmae S, Shibahara K, Nishino S and Matsunami H 1985 *Japan. J. Appl. Phys.* **24** L873
[46] Kelner G, Binari S C and Klein P H 1987 *J. Electrochem. Soc.* **134** 253
[47] Pan W-S and Steckl A J 1989 *SPP Amorphous and Crystalline Silicon Carbide* ed. M M Rahman, C Y-W Yang and G L Harris (Berlin: Springer) vol 43 p 217
Pan W-S and Steckl A J 1989 *SPP Amorphous and Crystalline Silicon Carbide* ed G L Harris and C Y-W Yang (Berlin: Springer) vol 34 p 192
[48] Suzuki A, Matsunami H and Tanaka T 1978 *J. Electrochem. Soc.* **125** 1896
[49] Lu W-J, Steckl A J, Chow T P and Katz W 1984 *J. Electrochem. Soc.* **131** 1907
[50] Fung C D and Kopanski J J 1984 *Appl. Phys. Lett.* **45** 757
[51] Suzuki A, Ashida H, Furui N, Mameno K and Matsunami H 1982 *Japan. J. Appl. Phys.* **21** 579
[52] Laukhe Yu, Tairov Yu M, Tsvetkov V F and Shchepanski F 1981 *Sov. Inorg. Mat.* **17** 177 (in Russian)
[53] Suzuki A, Mameno K, Furui N and Matsunami H 1981 *Appl. Phys. Lett.* **39** 89
[54] Muechlhoff L, Bozack M J, Choyke W J and Yates J T 1986 *J. Appl. Phys.* **60** 2558
[55] Deal B E and Grove A S 1965 *J. Appl. Phys.* **36** 3770
[56] Harris R C A and Call R L 1974 *Proc. Int. Conf. Silicon Carbide 73* ed J W Fast and C E Ryan (Columbia: University of South Carolina) p 329
[57] Petit J B, Powell J A and Matus L G 1991 *1st HiTEC Transactions* ed D B King and F V Thome (Albuquerque NM) p 198
[58] Zheng Z, Tressler R E, Spear K E and Costello J A 1990 *J. Electrochem. Soc.* **137** 854
[59] Hart R R, Dunlap H L and Marsh O J 1971 *Rad. Effects* **9** 261
[60] Spitznagel J A, Wood S and Choyke W J 1986 *Nucl. Instrum. Methods* **B16** 237
[61] Suzuki A, Furukawa K, Fujii Y. Shigeta M and Nakajama S 1990 *Proc. ICACSC* ed G L Harris, M G Spencer and C Y-W Yang (Washington DC) p 89
[62] Gudkov V A, Krysov G A and Makarov V N 1984 *Sov. Phys.-Semicond.* **18** 1098 (in Russian)
[63] Suvorov A V and Chechenin N G 1990 *Abstr. of the 7th Int. Conf. on Ion-Beam Modification of Materials (Nokswill CA)* p 310
[64] Burdell K K, Suvorov A V and Chechenin N G 1990 *Sov. Solid State Phys.* **32** 1672 (in Russian)
[65] Burdell K K, Varankin P V, Makarov V N, Suvorov A V and Chechenin N G 1988 *Sov. Solid State Phys.* **30** 629 (in Russian)
[66] Suvorov A V, Morozenko Ya V, Makarov V N and Ivanov P A 1986 *Abstr. of the 3rd Sov. Conf. on Phys. and Technol. of Wide-Bandgap Semiconductors* (Makhachkala USSR) p 28 (in Russian)
[67] Adachi S, Mohri M and Yamachina T 1985 *Surf. Sci.* **161** 479
[68] Kalinina E V, Suvorov A V and Kholuyanov G F 1980 *Sov. Phys.-Semicond.* **14** 652 (in Russian)
[69] Edmond J A, Withrow S P, Wadlin W and Davis R F 1987 *Interfaces Super-latties and Thin Films* ed

J D Dow and I K Schuller (Pittsburgh PA: Mat. Res. Soc.) p 193
[70] Bellina J J 1989 *SPP Amorphous and Crystalline Silicon Carbide* ed C-Y W Yang and G L Harris (Berlin: Springer) vol 43 p 162
[71] Naumov A V, Nikitin S V, Ostroumov A T and Vodakov Yu A 1987 *Sov. Phys.-Semicond.* **21** 377 (in Russian)
[72] Watt V H and Jackson K H 1989 *SPP Amorphous and Crystalline Silicon Carbide* ed G L Harris and C-Y W Yang (Berlin: Springer) vol 34 p 179
[73] Bellina J J and Zeller M V 1987 *Novel Refractory Semiconductors* ed D Emin, T L Aselage and C Wood (Pittsburgh PA: Mat. Res. Soc.) vol 297 p 265
[74] McMullin P G, Spitznagel J A, Szedon J R and Costello J A 1990 *Proc. ICACSC 90* ed G L Harris, M G Spencer and C-Y W Yang (Washington DC) p 294
[75] Geib K M, Mahan J E and Wilmsen C W 1989 *SPP Amorphous and Crystalline Silicon Carbide* ed M M Rahman, C-Y W Yang and G L Harris (Berlin: Springer) vol 43 p 224
[76] Anikin M M, Rastegaeva M G, Syrkin A L and Chuiko I V 1990 *Proc. ICACSC 90* ed M G Spencer and C-Y W Yang (Washington DC) p 191
[77] Anikin M M, Lebedev A A, Popov I V, Sevastjanov V N, Syrkin A L, Suvorov A V, Chelnokov V E and Schpynev G P 1984 *Sov. Phys. Techn. Lett.* **10** 1053 (in Russian)
[78] Anikin M M, Lebedev A A, Popov I V, Strelchuk A M, Syrkin A L, Suvorov A V and Chelnokov V E 1986 *Sov. Phys.-Semicond.* **20** 844 (in Russian)
[79] Anikin M M, Lebedev A A, Syrkin A L, Suvorov A V and Strelchuk A M 1989 *Extend. Abstr. of the 176th Meet. of the Electrochem. Soc. (Hollywood FL)* p 708
[80] Avila R E, Kopanski J J and Fung C D 1987 *J. Appl. Phys.* **62** 3469
[81] Edmond J A, Das K and Davis R F 1988 *J. Appl. Phys.* **63** 922
[82] Tang L A, Edmond J A, Palmour J W and Carter C H 1989 *Extend. Abstr. of the 176th Meet. of the Electrochem. Soc. (Hollywood FL)* p 705
[83] Edmond J A, Waltz D G, Brueckner S, Kong H S, Palmour J W and Carter C H 1991 *Ist HiTEC Transactions* ed D B King and F V Thome (Albuquerque NM) p 207
[84] Anikin M M, Andreev A N, Lebedev A A, Pyatko S N, Rastegaeva M G, Savkina N S, Strelchuk A M, Syrkin A L and Chelnokov V E 1991 *Sov. Phys.-Semicond.* **25** 328 (in Russian)
[85] Ioannou D E, Papanicolaou N A and Nordquist P E 1987 *IEEE Trans. Electr. Dev.* **ED-34** 1694
[86] Papanicolaou N A, Christou A and Gipe M L 1989 *J. Appl. Phys.* **65** 3526
[87] Yoshida S, Sasaki K, Sakuma E, Misawa S and Gonda S 1985 *Appl. Phys. Lett.* **46** 766
[88] Edmond J A, Ryu J, Glass J T and Davis R F 1988 *J. Electrochem. Soc.* **135** 359
[89] Dmitriev V A, Ivanov P A, Strelchuk A M, Syrkin A L, Popov I V and Chelnokov V E 1985 *Sov. Phys. Techn. Lett.* **11** 976 (in Russian)
[90] Anikin M M, Lebedev A A, Popov I V, Strelchuk A M, Suvorov A V, Syrkin A L and Chelnokov V E 1986 *Sov. Phys.-Semicond.* **20** 1654 (in Russian)
[91] Dmitriev V A, Ivanov P A, Popov I V, Strelchuk A M, Syrkin A L and Chelnokov V E 1986 *Sov. Phys. Techn. Lett.* **12** 773 (in Russian)
[92] Poltinnikov C A, Vodakov Yu A, Lomakina G A, Mokhov E N, Semenov V V and Roenkov A D 1986 *Sov. Phys. Techn. Lett.* **12** 261 (in Russian)
[93] Anikin M M, Lebedev A A, Popov I V, Pyatko S N, Rastegaev V P, Syrkin A L, Tsarenkov B V and Chelnokov V E 1988 *Sov. Phys.-Semicond.* **22** 133 (in Russian)
[94] Opdorp C and Wrakking J 1969 *J. Appl. Phys.* **40** 2320
[95] Dmitriev A P, Konstantinov A O, Litvin D P and Sankin V I 1983 *Sov. Phys.-Semicond.* **17** 686 (in Russian)
[96] Sze S M and Gibbons J 1966 *Appl. Phys. Lett.* **8** 111
[97] Konstantinov A O 1989 *Sov. Phys.-Semicond.* **23** 31 (in Russian)
[98] Konstantinov A O 1989 *Sov. Phys.-Semicond.* **23** 616 (in Russian)
[99] Konstantinov A O 1990 *Proc. ICACSC90* ed G L Harris, M G Spencer and C-Y W Yang (Washington DC) p 231
[100] Anikin M M, Evstropov V V, Popov I V, Rastegaev V P, Strelchuk A M and Syrkin A L 1989 *Sov. Phys.-Semicond.* **23** 647 and 1813 (in Russian)
[101] Evstropov V V, Kiselev K V, Petrovich I L and Tsarenkov B V 1984 *Sov. Phys.-Semicond.* **18** 1852 (in Russian)
[102] Muench W, Hoeck P and Pettenpaul E 1977 *Techn. Digest IEDM* (New York: IEEE) p 337
[103] Yoshida S, Daimon H, Yamanaka M, Sakuma E, Misawa S and Endo K 1986 *J. Appl. Phys.* **60** 2989
[104] Kelner G, Binari S, Sleger K and Kong H 1987 *IEEE Electr. Dev. Lett.* **EDL-8** 429
[105] Kong H S, Palmour J W, Glass J T and Davis R F 1987 *Appl. Phys. Lett.* **51** 442
[106] Palmour J W, Kong H S, Waltz D G, Edmond J A and Carter C H 1991 *1st HiTEC Transactions* ed D B King and F V Thome (Albuquerque NM) p 229
[107] Dmitriev V A, Ivanov P A, Il'inskaya N D, Syrkin A L, Tsarenkov B V, Chelnokov V E and Cherenkov A E 1988 *Sov. Phys. Techn. Lett.* **14** 289 (in Russian)
[108] Anikin M M, Ivanov P A, Syrkin A L, Tsarenkov B V and Chelnokov V E 1989 *Sov. Phys. Techn. Lett.* **15** 36 (in Russian)
[109] Anikin M M, Ivanov P A, Syrkin A L and Tsarenkov B V 1989 *Extend. Abstr. of the 176th Meet. of the Electrochem. Soc. (Hollywood FL)* p 779
[110] Furukawa K, Hatano A, Uemoto A, Fujii Y, Nakanishi K, Shigeta M, Suzuki A and Nakajima S 1987 *IEEE Electr. Dev. Lett.* **EDL-8** 48
[111] Kelner G, Shur M, Binari S, Sleger K and Kong H 1989 *IEEE Electr. Dev.* **ED-36** 1045
[112] Kondo Y, Takahashi T, Ishii K, Hayashi Y, Sakuma E, Misawa S, Daimon H, Yamanaka M and Yoshida S 1987 *Japan. J. Appl. Phys.* **26** 310
[113] Palmour J W, Kong H S and Davis R F 1988 *J. Appl. Phys.* **64** 168
[114] Fuma H, Miura A, Tadano H, Sugiyama S and Takigawa M 1989 *SPP Amorphous and Crystalline Silicon Carbide* ed C-Y W Yang and G L Harris (Berlin: Springer) vol 43 p 178
[115] Shibahara K, Takauchi T, Saito T, Nishino S and Matsunami H 1987 *Mat. Res. Soc. Symp Proc.* **97** 247
[116] Kelner G, Binari S, Sleger K and Palmour J 1990 *Proc. E-MRS90 Meet. (Strasbourg France)* (to be published)
[117] Dmitriev V A, Ivanov P A, Chelnokov V E and Cherenkov A E 1991 *Sov. Phys. Techn. Lett.* **17** 1 (in Russian)
[118] Shockley W 1952 *Proc. IRE* **40** 1356
[119] Suzuki A, Furukawa K, Fujii Y, Shigeta M and Nakajima S 1990 *Proc. ICACSC90* ed G L Harris, M G Spencer and C-Y W Yang (Washington DC) p 89
[120] Anikin M M, Lebedev A A, Pyatko S N, Soloviev V A and Strelchuk A M 1990 *Proc. ICACSC90* ed G L Harris, M G Spencer and C-Y W Yang (Washington DC) p 290

[121] Muench W 1978 *Solid State Electr.* **21** 479
[122] Dmitriev V A, Ivanov P A and Chelnokov V E 1991 *Sov. Electronic Industry* **5** 19 (in Russian)
[123] Dmitriev V A, Levinshtein M E, Vainshtein S N and Chelnokov V E 1988 *Electr. Lett.* **24** 1031
[124] Tairov Yu M and Vodakov Yu A 1977 *Topics in Appl. Phys.* ed I Pankove (Berlin: Springer) vol 17 p 31
[125] Gusev V M and Demakov K D 1981 *Sov. Phys.-Semicond.* **15** 2430 (in Russian)
[126] Vishnevskaya B I, Dmitriev V A, Kogan L M, Morozenko Ya V, Chelnokov V E and Cherenkov A E 1990 *Sov. Phys. Techn. Lett.* **16** 56 (in Russian)
[127] Barash A S, Vodakov Yu A, Koltsova E N, Maltsev A A, Mokhov E N and Roenkov A D 1988 *Sov. Phys. Techn. Lett.* **14** 2222 (in Russian)
[128] Vodakov Yu A, Mokhov E N, Roenkov A D, Semenov V I, Verenchikova R G, Konstantinov A O, Sokolov V I and Oding V G 1990 *Proc. ICACSC90* ed G L Harris, M G Spencer and C Y-W Yang (Washington DC) p 320
[129] Vishnevskaya B I, Dmitriev V A, Kovalenko I D, Kogan L M, Morozenko Ya V, Rodkin V S, Tsarenkov B V and Chelnokov V E 1988 *Sov. Phys.-Semicond.* **22** 664 (in Russian)
[130] Tang L A, Edmond J A, Palmour J W and Carter C H 1989 *Extend. Abstr. of the 176th Meet. of the Electrochem. Soc. (Hollywood FL)* p 705
[131] Nakata T, Koga K, Matsushita Y, Ueda Y and Niina T 1989 *SPP Amorphous and Crystalline Silicon Carbide* ed M M Rahman, C-Y W Yang and G L Harris (Berlin: Springer) vol 43 p 26
[132] Dmitriev V A, Ivanov P A, Morozenko Ya V, Popov I V and Chelnokov V E 1985 *Sov. Phys. Techn. Lett.* **11** 246 (in Russian)
[133] Dmitriev V A, Kogan L M, Morozenko Ya V, Tsarenkov B V, Chelnokov V E and Cherenkov A E 1989 *Sov. Phys.-Semicond.* **23** 39 (in Russian)
[134] Koga K, Nakata T, Ueda Y, Matsushita Y, Fujikawa Y, Uetani T and Niina T 1989 *Extend. Abstr. of the 176th Meet. of the Electrochem. Soc. (Hollywood FL)* p 689
[135] Verenchikova R G and Sankin V I 1988 *Sov. Phys. Techn. Lett.* **14** 1742 (in Russian)
[136] Anikin M M, Andreev A N, Pyatko S N, Rastegaeva M G, Syrkin L and Chelnokov V E 1991 *Proc. E-MRS90 Meet. (Strasbourg France)* to be published
[137] Glasov P A 1989 *SPP Amorphous and Crystalline Silicon Carbide* ed G L Harris and C Y-W Yang (Berlin: Springer) vol 34 p 13
[138] Brown D M, Downey E, Chezzo M, Kretchmer J and Liu Y S 1991 *1st HiTEC Transactions* ed D B King and F V Thome (Albuqerque NM) p 214
[139] Johnson E O 1965 *RCA Rev.* **26** 169
[140] Keyes R W 1972 *Proc. IEEE* 225
[141] Tager A S 1979 *Proc. 2nd Sov. Conf. on Physical and Technological Problems of Wide-Bandgap Semiconductors* (Leningrad USSR) p 211 (in Russian)
[142] Shenai K, Scott R S and Baliga B J 1989 *IEEE Trans. Electr. Dev.* **ED-36** 1811
[143] Ivanov P A and Tsarenkov B V 1991 *Sov. Phys.-Semicond.* to be published
[144] Pucel R, Haus H and Statz H 1975 *Advances in Electronics and Electr. Phys.* (New York: Academic) vol 38 p 195
[145] Sze S M 1981 *Physics of Semiconductors* 2nd edn (New York: Wiley)