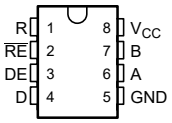
HIGH-SPEED DIFFERENTIAL LINE TRANSCEIVER

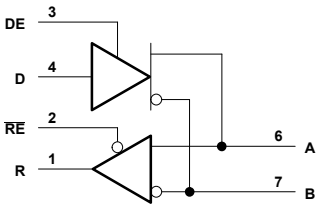
FEATURES

- **Low-Voltage Differential Driver and Receiver for Half-Duplex Operation**
- **Designed for Signaling Rates of 400 Mbit/s**
- **ESD Protection Exceeds 15 kV on Bus Pins**
- **Operates From a Single 3.3-V Supply**
- **Low-Voltage Differential Signaling With Typical Output Voltages of 350 mV and a 50-Ω Load**
- **Valid Output With as Little as 50 mV Input Voltage Difference**
- **Propagation Delay Times**
  - **Driver: 1.7 ns Typ**
  - **Receiver: 3.7 ns Typ**
- **Power Dissipation at 200 MHz**
  - **Driver: 50 mW Typical**
  - **Receiver: 60 mW Typical**
- **LVTTL Levels Are 5-V Tolerant**
- **Bus Pins Are High Impedance When Disabled or With V_{CC} Less Than 1.5 V**
- **Open-Circuit Fail-Safe Receiver**
- **Surface-Mount Packaging**
  - **D Package (SOIC)**
  - **DGK Package (MSOP)**

SN65LVDM176D (Marked as **DM176** or **LVM176)**
SN65LVDM176DGK (Marked as **M76**)
(TOP VIEW)



logic diagram (positive logic)



DESCRIPTION

The SN65LVDM176 is a differential line driver and receiver configured as a transceiver that uses low-voltage differential signaling (LVDS) to achieve signaling rates as high as 400 Mbit/s. These circuits are similar to TIA/EIA-644 standard compliant devices (SN65LVDS) counterparts except that the output current of the drivers is doubled. This modification provides a minimum differential output voltage magnitude of 247 mV into a 50-Ω load and allows double-terminated lines and half-duplex operation. The receivers detect a voltage difference of less than 50 mV with up to 1 V of ground potential difference between a transmitter and receiver.

The intended application of this device and signaling technique is for half-duplex or multiplex baseband data transmission over controlled impedance media of approximately 100-Ω characteristic impedance. The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics).

The SN65LVDM176 is characterized for operation from –40°C to 85°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T_A	PACKAGE	
	SMALL OUTLINE (D)[1]	MSOP (DGK)[1]
–40°C to 85°C	SN65LVDM176D	SN65LVDM176DGK

(1) The D package is available taped and reeled. Add the suffix R to the device type(e.g., SN65LVDM176DR).

FUNCTION TABLES

DRIVER[1]

INPUT D	ENABLE DE	OUTPUTS	
		A	B
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	Z	Z

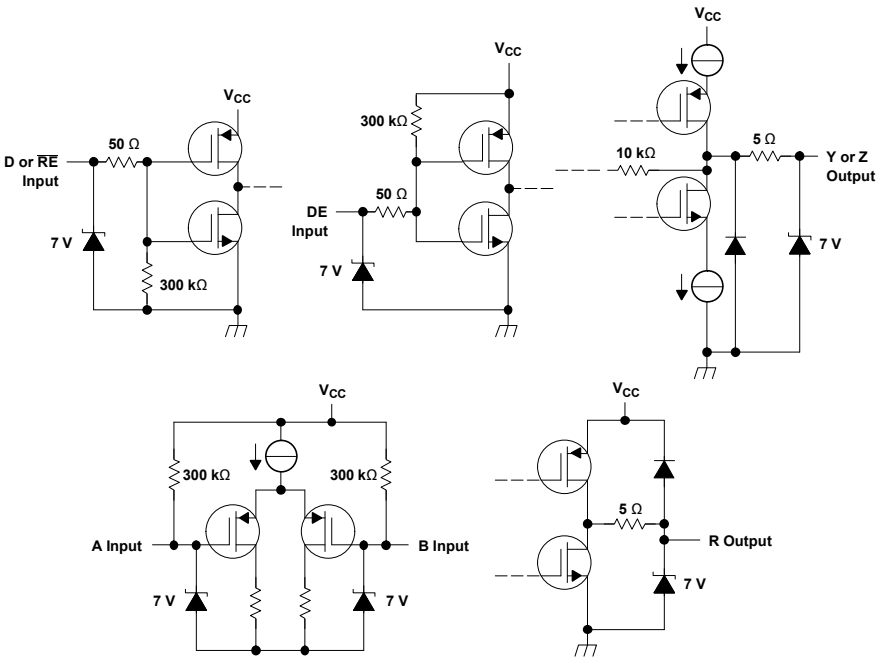
(1) H = high level, L = low level, X = irrelevant, Z = high impedance

RECEIVER[1]

DIFFERENTIAL INPUTS $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 50$ mV	L	H
50 mV < V_{ID} < 50 mV	L	?
$V_{ID} \leq -50$ mV	L	L
Open	L	H
X	H	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
V_{CC}	Supply voltage(2)		–0.5 V to 4 V
	Input voltage range	D, R, DE, $\overline{RE}$	–0.5 V to 6 V
		A or B	–0.5 V to 4 V
	Electrostatic discharge	A, B , and GND(3)	CLass 3, A:15 kV, B:600 V
		All terminals	Class 3, A:7 kV, B:500 V
	Continuous total power dissipation		See Dissipation Rating Table
T_A	Operating free-air temperature range		–40°C to 85°C
T_{stg}	Storage temperature range		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.
(3) Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
DGK	424 mW	3.4 mW/°C	220 mW

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
$\lvert V_{ID}\rvert$	Magnitude of differential input voltage	0.1		0.6	V
V_{IC}	Common-mode input voltage (see Figure 1)	$\frac{\lvert V_{ID}\rvert}{2}$		$2.4 - \frac{\lvert V_{ID}\rvert}{2}$	V
				$V_{CC}-0.8$	
T_A	Operating free-air temperature	–40		85	°C

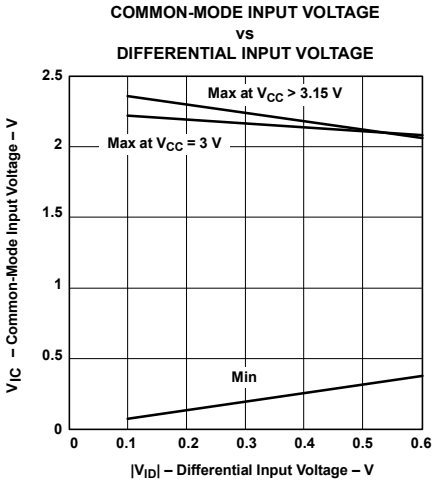


Figure 1.

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC} Supply current	Driver and receiver enabled, no receiver load, driver $R_L = 50\ \Omega$		10	15	mA
	Driver enabled, receiver disabled, $R_L = 50\ \Omega$		9	15	
	Driver disabled, receiver enabled, no load		1.8	5	
	Disabled		0.5	2	

(1) All typical values are at 25°C and with a 3.3-V supply.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude		R_L = 50 Ω, See Figure 2 and Figure 3	247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states			–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 4	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				50	150	mV
I_{IH}	High-level input current(1)	DE	V_{IH} = 5 V		0.5	10	µA
		D			2	20	
I_{IL}	Low-level input current(1)	DE	V_{IL} = 0.8 V		–0.5	–10	µA
		D			2	10	
I_{OS}	Short-circuit output current(1)		V_{OA} or V_{OB} = 0 V			–10	mA
			V_{OD} = 0 V			–10	
C_I	Input capacitance				3		pF

(1) The non-algebraic convention, where the more positive (least negative) limit is designated maximum, is used in this data sheet for this parameter.

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	See Figure 6			50	mV
V_{IT-}	Negative-going differential input voltage threshold		–50			
V_{OH}	High-level output voltage	I_{OH} = –8 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.4	V
I_I	Input current (A or B inputs)(2)	V_I = 0 V	–2		–20	µA
		V_I = 2.4 V	–1.2			
$I_{I(OFF)}$	Power-off input current (A or B inputs)	V_{CC} = 0 V or 1.8 V			20	µA
I_{IH}	High-level input current (enables)	V_{IH} = 5 V			10	µA
I_{IL}	Low-level input current (enables)	V_{IL} = 0.8 V			10	µA
I_{OZ}	High-impedance output current(2)	V_O = 0 V or 5 V			±1	µA

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) The non-algebraic convention, where the more positive (least negative) limit is designated maximum, is used in this data sheet for this parameter.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 50 Ω, C_L = 10 pF, See Figure 3	0.5	1.7	2.7	ns
t_{PHL}	Propagation delay time, high-to-low-level output		0.5	1.7	2.7	
$t_{sk(p)}$	Pulse skew ($\|t_{pHL} - t_{pLH}\|$)			0.2		ns
t_r	Differential output signal rise time			0.6	1	ns
t_f	Differential output signal fall time			0.6	1	
$t_{sk(pp)}$(2)	Part-to-part skew				1	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 5		8	12	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			7	10	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			3	10	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			4	10	

(1) All typical values are at 25°C and with a 3.3 V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 7	2.3	3.7	4.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2.3	3.7	4.5	
$t_{sk(p)}$	Pulse skew ($\|t_{pHL} - t_{pLH}\|$)			0.4		
t_r	Output signal rise time			0.8	1.5	ns
t_f	Output signal fall time			0.8	1.5	
$t_{sk(pp)}$(2)	Part-to-part skew				1	ns
t_{PZH}	Propagation delay time, high-level-to-high-impedance output	See Figure 8		3	10	ns
t_{PZL}	Propagation delay time, low-level-to-low-impedance output			3	10	
t_{PHZ}	Propagation delay time, high-impedance-to-high-level output			4	10	
t_{PLZ}	Propagation delay time, low-impedance-to-high-level output			6	10	

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

DRIVER

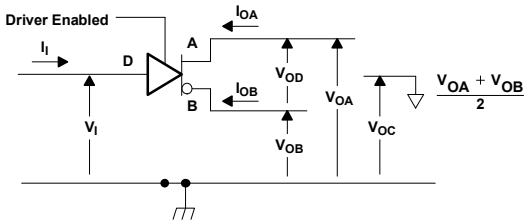
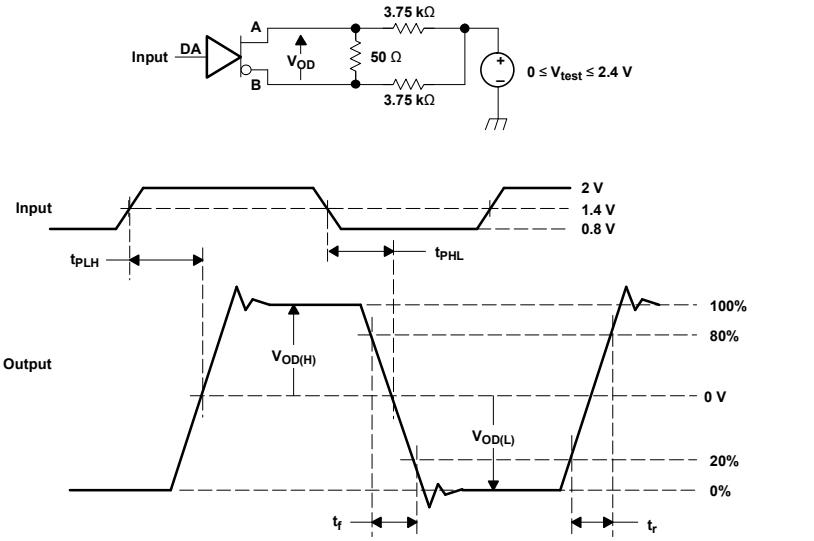


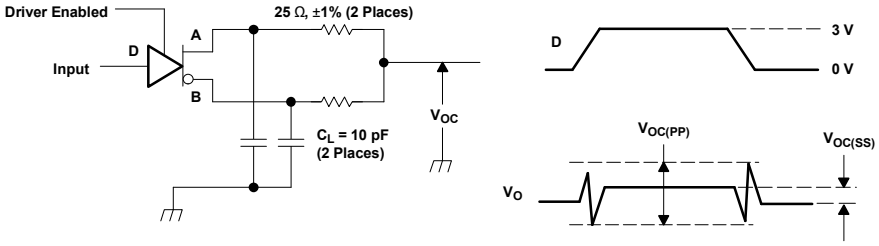
Figure 2. Driver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

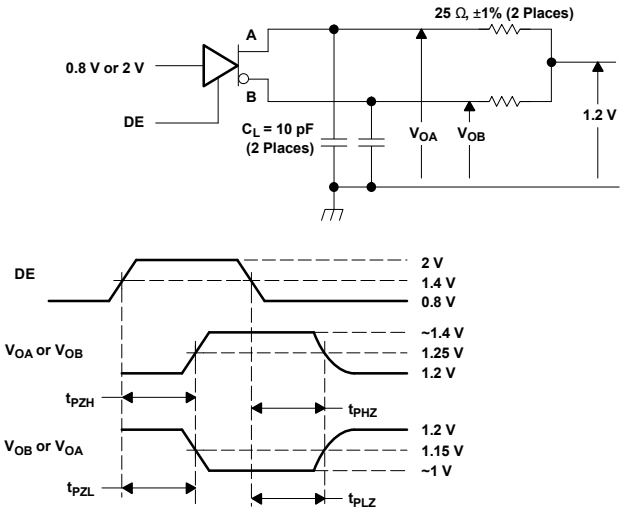
Figure 3. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION (continued)



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 5. Enable and Disable Time Circuit and Definitions

RECEIVER

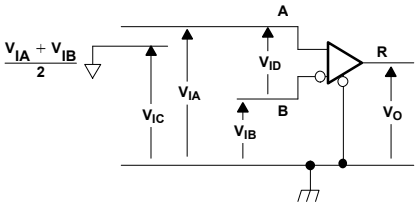
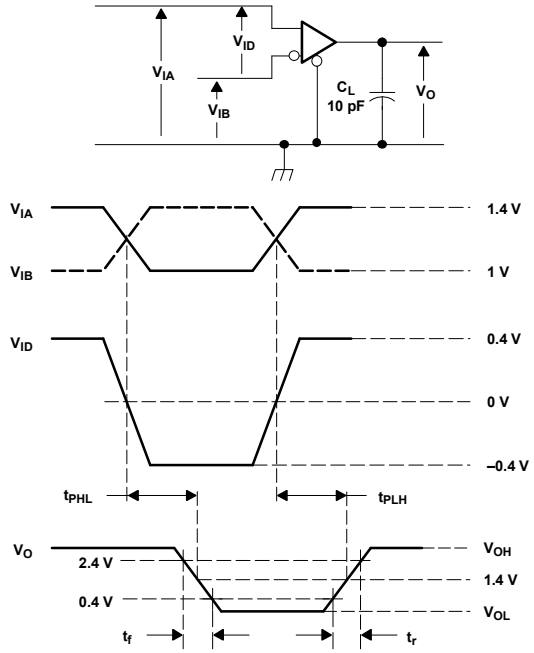


Figure 6. Receiver Voltage Definitions

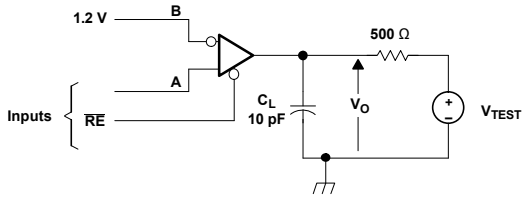
Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES (V)		RESULTING DIFFERENTIAL INPUT VOLTAGE (mV)	RESULTING COMMON-MODE INPUT VOLTAGE (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.225	1.175	50	1.2
1.175	1.225	–50	1.2
2.41	2.36	50	2.385
2.36	2.41	–50	2.385
0.05	0	50	0.025
0	0.05	–50	0.025
1.5	0.9	600	1.2
0.9	1.5	–600	1.2
2.4	1.8	600	2.1
1.8	2.4	–600	2.1
0.6	0	600	0.3
0	0.6	–600	0.3



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 7. Timing Test Circuit and Waveforms



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 5000 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

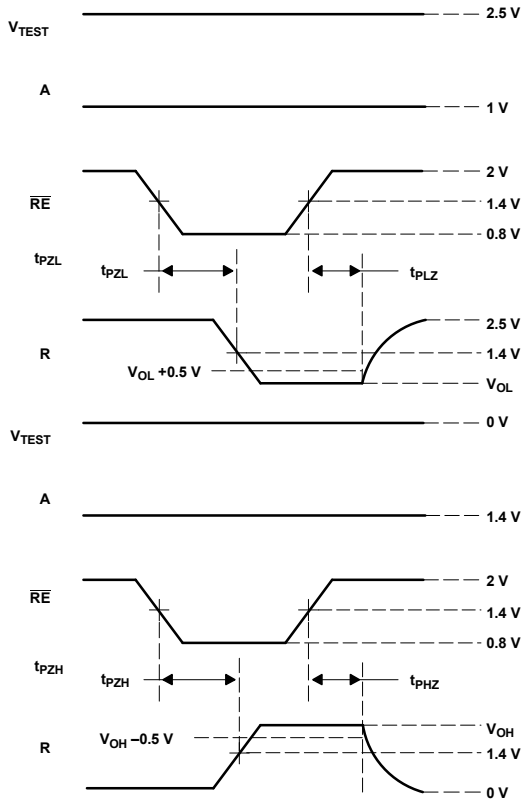


Figure 8. Enable/Disable Time Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

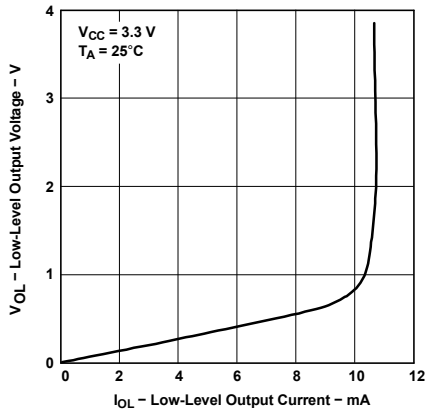


Figure 9.

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

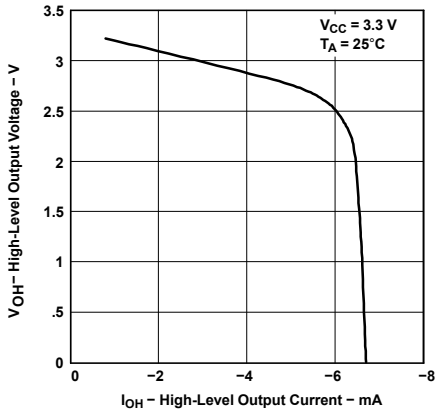


Figure 10.

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

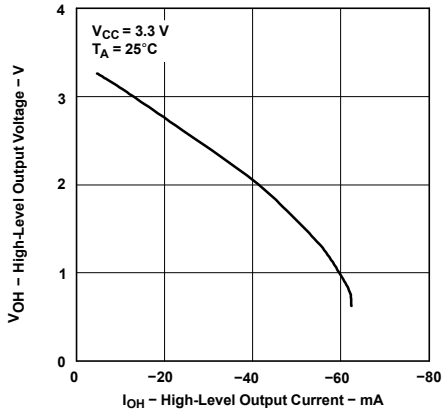


Figure 11.

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

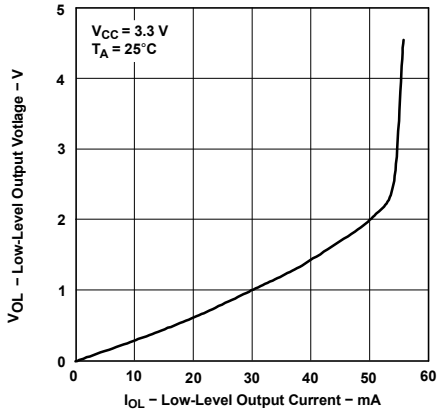


Figure 12.

TYPICAL CHARACTERISTICS (continued)

DRIVER
HIGH-TO-LOW LEVEL PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

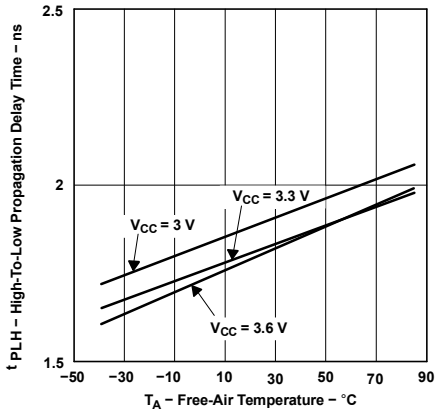


Figure 13.

DRIVER
LOW-TO-HIGH LEVEL PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

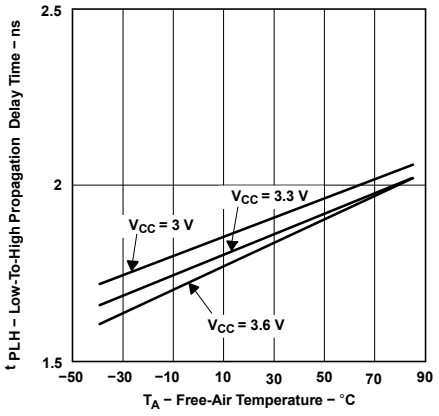


Figure 14.

RECEIVER
HIGH-TO-LOW LEVEL PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

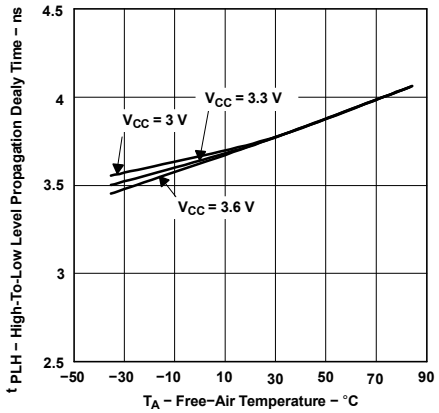


Figure 15.

RECEIVER
LOW-TO-HIGH LEVEL PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

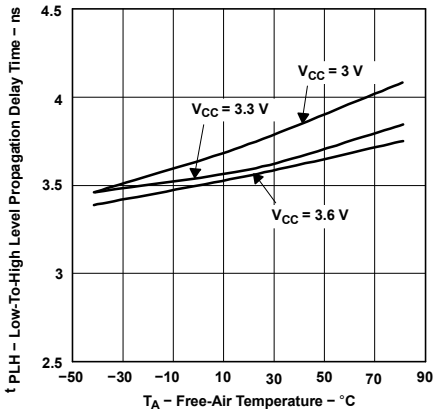


Figure 16.

APPLICATION INFORMATION

The devices are generally used as building blocks for high-speed point-to-point data transmission. Ground differences are less than 1 V with a low common-mode output and balanced interface for very low noise emissions. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/receivers maintain ECL speeds without the power and dual supply requirements.

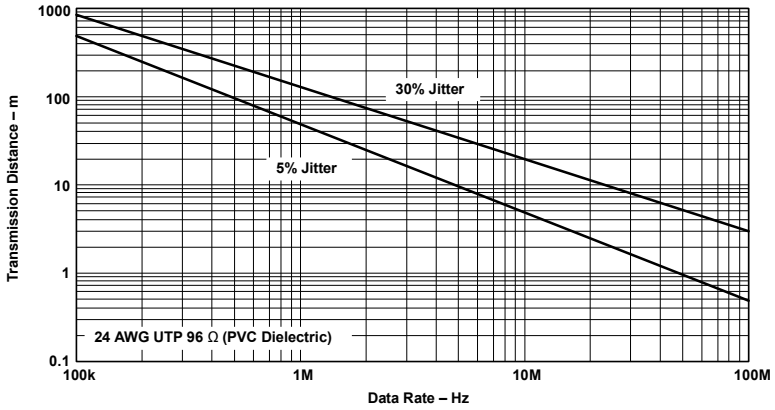


Figure 17. Data Transmission Distance Versus Rate

FAIL SAFE

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –50 mV and 50 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near V_{CC} through 300-kΩ resistors as shown in Figure 18. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level regardless of the differential input voltage.

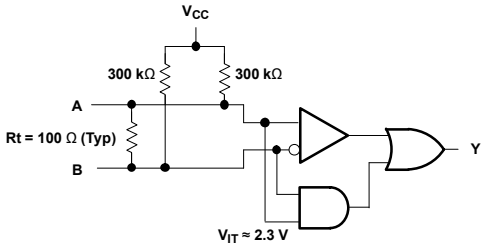
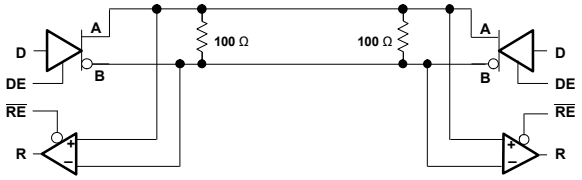


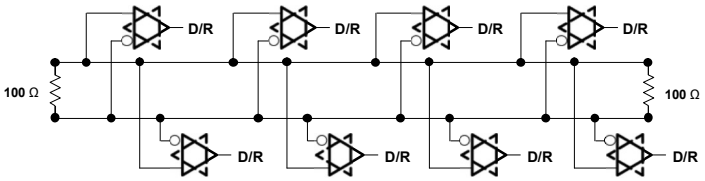
Figure 18. Open-Circuit Fail Safe of the LVDS Receiver

APPLICATION INFORMATION (continued)

It is only under these conditions that the output of the receiver will be valid with less than a 50-mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.



Bidirectional Half-Duplex Applications



Multipoint Bus Applications

Note A: Keep drivers and receivers as close to the LVDS bus side connector as possible.

Figure 19. Bidirectional Half-Duplex and Multipoint Bus Applications

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDM176D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DM176	Samples
SN65LVDM176DGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	M76	Samples
SN65LVDM176DGKG4	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M76	Samples
SN65LVDM176DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	M76	Samples
SN65LVDM176DGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	M76	Samples
SN65LVDM176DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DM176	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

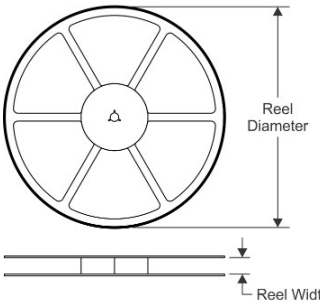
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

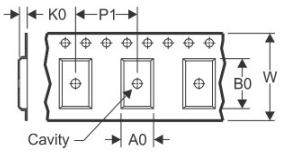
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

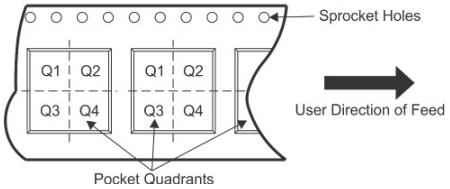


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

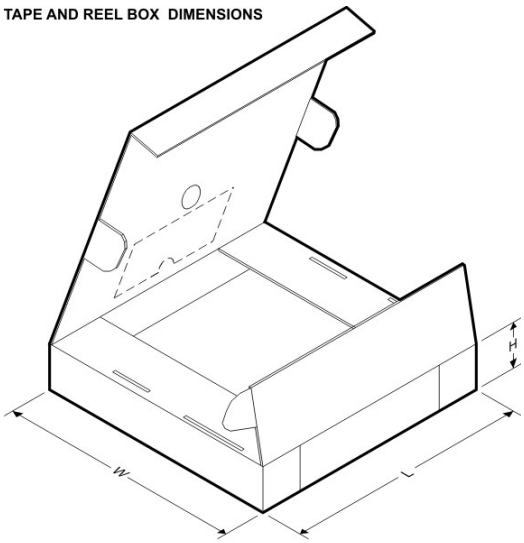
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDM176DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVDM176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

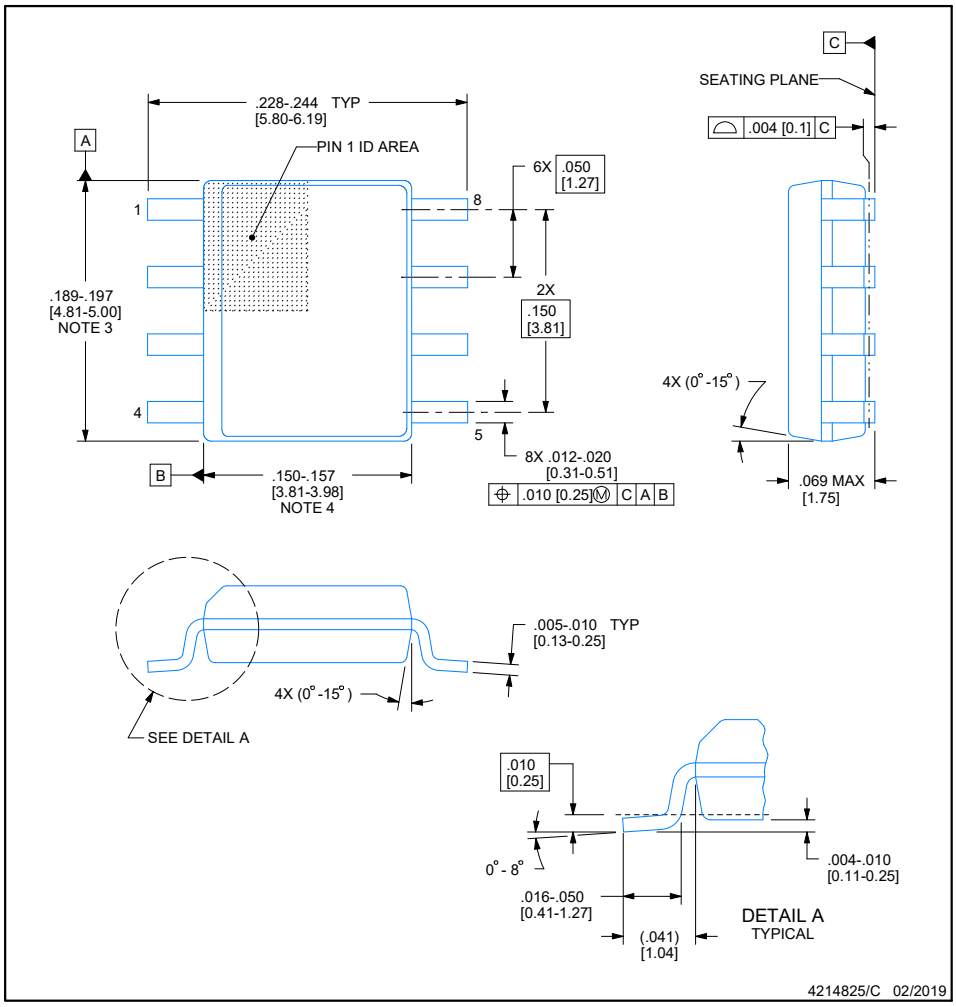
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDM176DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
SN65LVDM176DR	SOIC	D	8	2500	340.5	338.1	20.6

PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

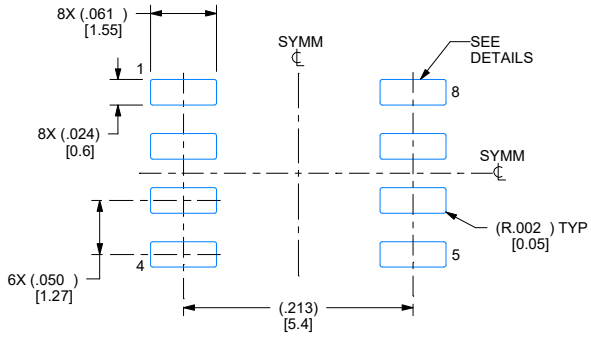
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

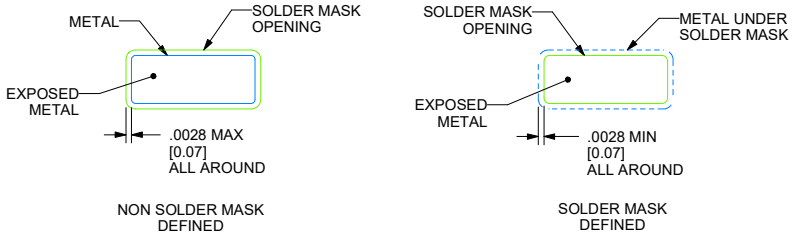
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

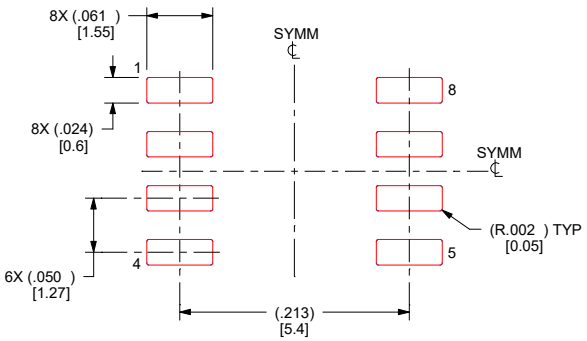


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



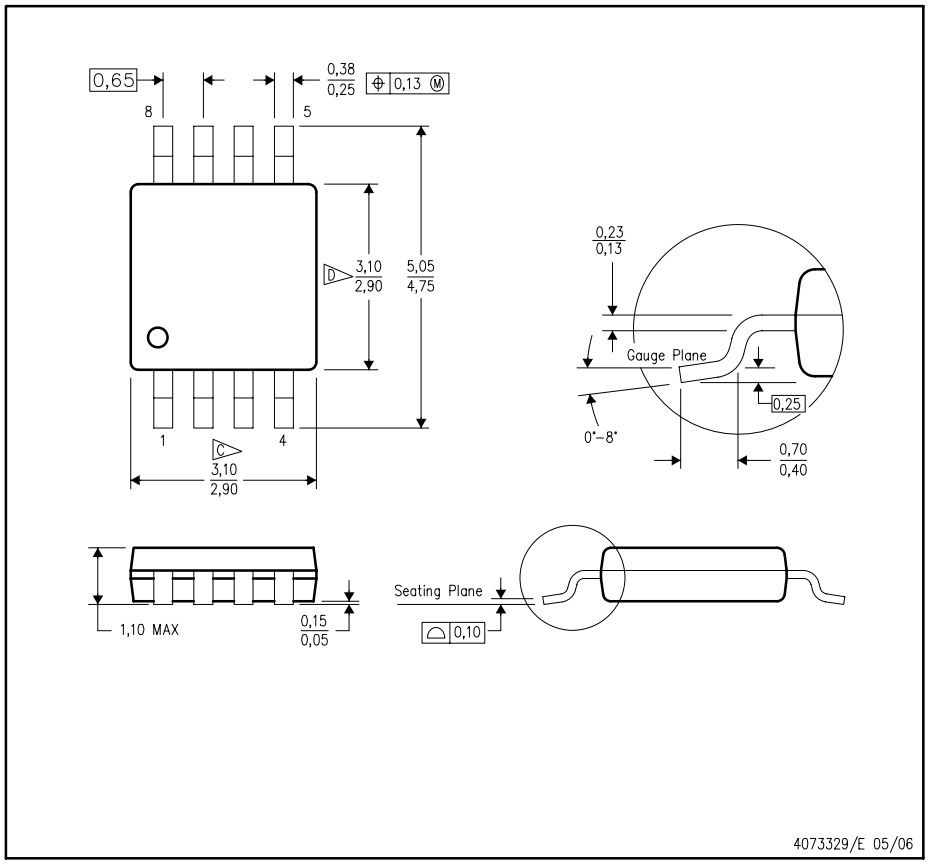
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

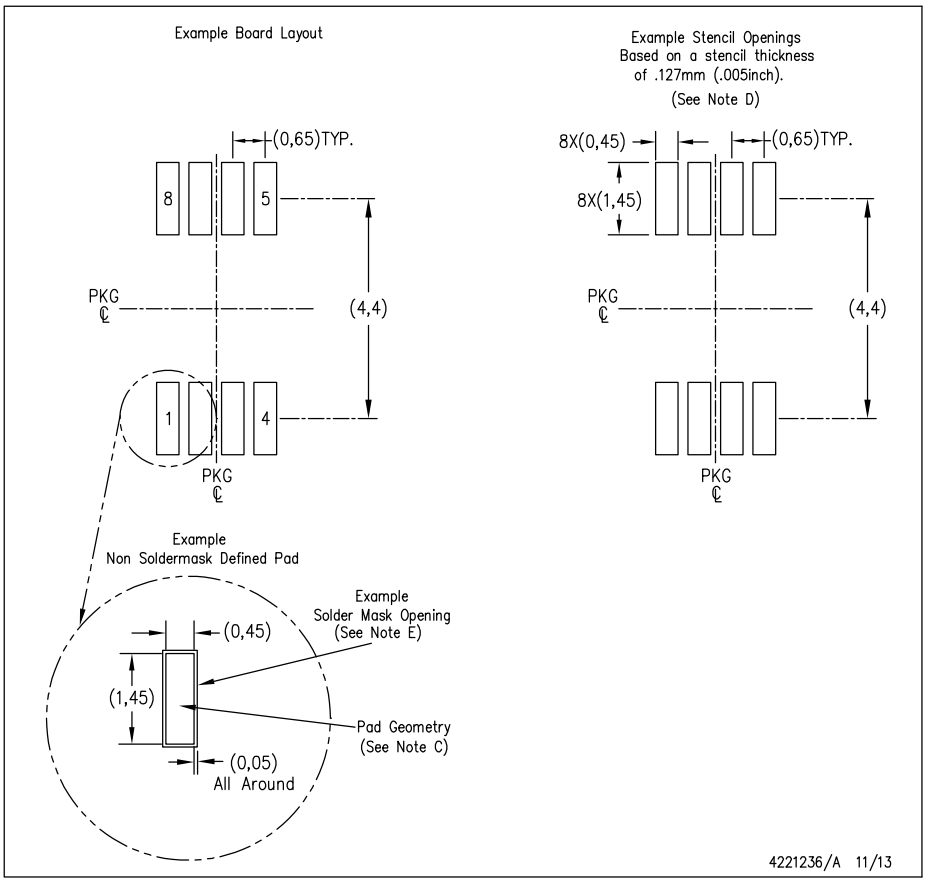
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265