CHAPTER 3

LIRD-4B OPERATION

3.1 GENERAL DESCRIPTION

LIRD-4B consists of two major sub-assemblies, the detector head and indicator unit..

The detector head (id. 69270) detects laser irradiation. It is mounted outside on the turret. The detector head consists of several windows with receivers of irradiation.

The detector head is electrically connected to the indicator unit (id. 69271) via two serially connected cables - Signal Cable 1 and the Signal Cable 2 . The direction of irradiation, and the kind of source (LR, LD, BR) of irradiation are displayed on the indicator unit. The power supply for the entire device is also led into the indicator unit. The on/off switch is on the indicator unit as well.

3.2 DETECTOR HEAD

The detector head is designed to detect laser irradiation from a laser illuminators-designators, from laser rangefinders or laser beam riders. The head is electrically connected with the indicator unit, witch provides the head with power supply. Information on detected laser irradiation is sent back via signals which are brought to connector K40 (See the block diagram bellow)

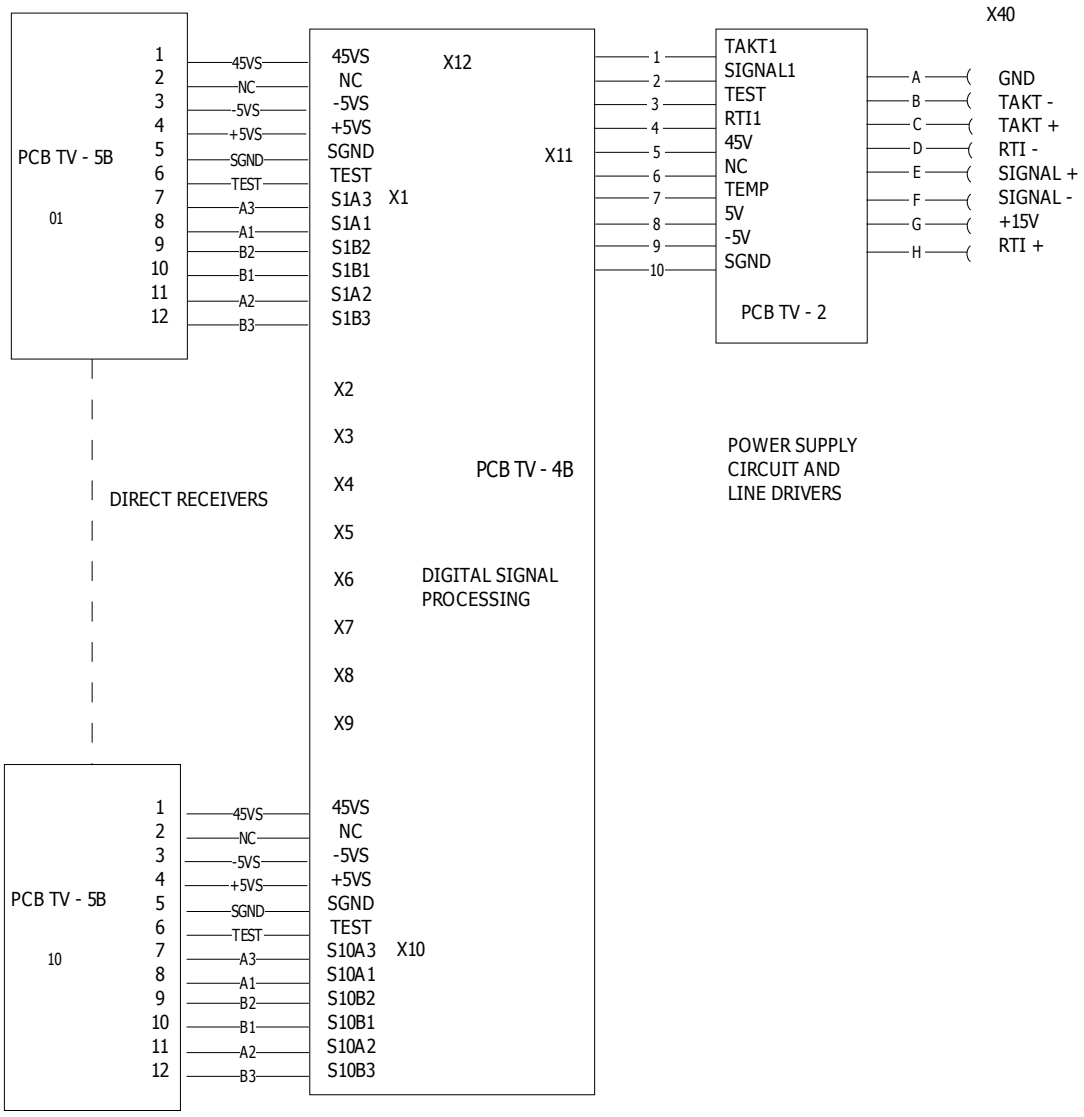

Figure 3.2
Detector Head Block Diagram

The Digital Signal Processing PC board (TV-4B) distributes the necessary power supply voltages to all the receiver PC board connected to it. Ten direct receiver PC boards are exactly alike (TV-5B) with exactly the same signal leads which connect them to the Digital Signal Processing PCB. This is a microprocessor based board which takes care of identifying from which receiver boards a laser threat signals are coming, processing their timing relations and preparing information to be sent to the indicator unit.

The data are output to the indicator unit via a synchronous RS-422 data transmission link (SIGNAL+, SIGNAL-, TAKT+, TAKT-) transmitting 16-bit data bursts and employing the RTI line (RTI+, RTI-) for precise (real time) indication of when exactly the laser threats were detected.

The detector head supply voltage: 12 - 15V, consumption 0.7A.

In terms of functions, the detection head can be divided into the following units:

- direct receivers optics
- direct receivers
- digital processing
- power supply
- serial lines controller
- mechanics

3.2.1 Direct Receivers Optics

The optical aperture in front of each direct receiver both allows admittance of the light pulses to be detected and protects the receiver electronics from undesired external mechanical and optical interference or damage. At the same time mechanical construction of the openings is such that the specified viewing angles both horizontally and vertically are assured (see Technical Data).

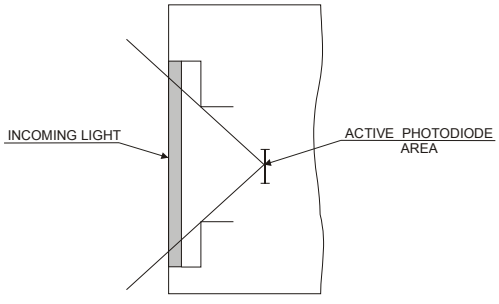

Figure 3.3
Cross section of one window in elevation

The viewing angles of the optical apertures of the direct receivers are designed such that proper overlapping of detection is assured. In this way the number of the receivers can be half the number of total angle sectors which can be actually designated and indicated by the device. The processing of the detector data is done in such a way that only one resulting sector indicator is triggered regardless of the actual number and distribution of the detected signals.

3.2.2 Direct Receiver (TV-5B), ID. 68088

The direct receiver comprises of: a Si and an InGaAs photodiode, two 3-level amplifiers and six threshold level circuits.

In order to accommodate the spectral sensitivity range 0.4 to 1.6 μm, two photodiodes are applied, a Si and an InGaAs photodiode. The Si photodiode has an active area diameter of 5 mm. It is reversely polarised by +35V. Its spectral sensitivity range is 0.4 to 1.1 μm.

The InGaAs diode has an active area diameter of 3 mm. It is reversely polarised by +5V. Its spectral sensitivity range is 1 to 1.6 μm. A change in the voltage drop over the photodiode working resistor, caused by the change of current through the photodiode, is amplified in 3 branches. Each branch ends with a threshold circuit. When the threshold circuit input signal exceeds a pre-set threshold level, a negative digital signal is output. All the threshold circuits are set by means of a single trimmer potentiometer and thus have the same level thresholds.

The direct receiver power supply consists of +5V, -5VS and +35V. Its input electrical signal is TEST, and its output signals are: A1, A2, A3, B1, B2 and B3.

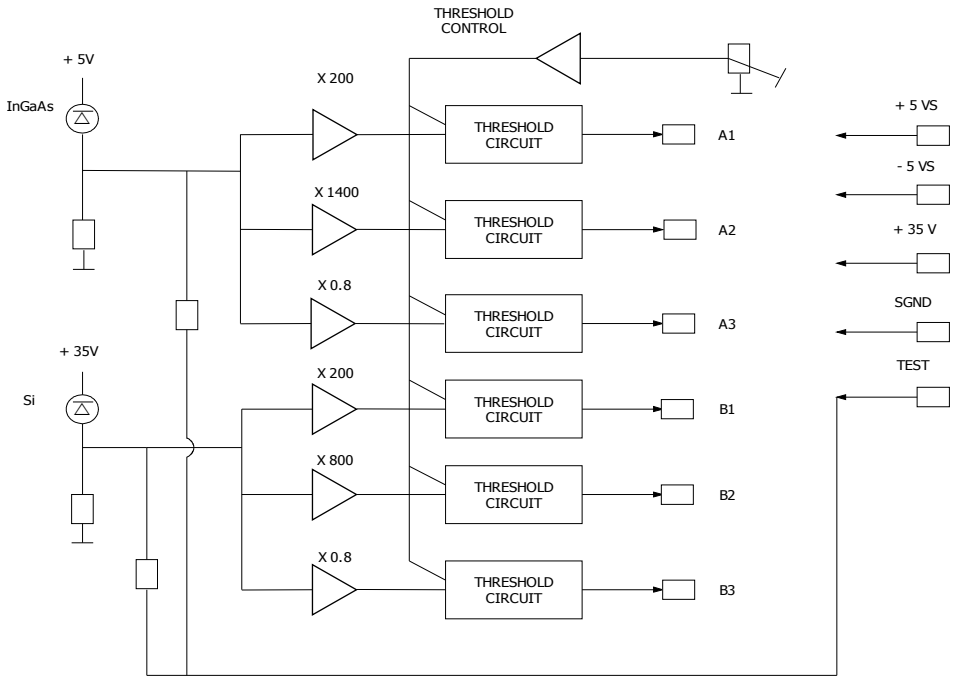

Figure 3.4

To a 5V input TEST impulse, the receiver responds with digital signals A2 and B2 as shown on the timing diagram. On the diagram the upper signal is TEST and the lower is A2.

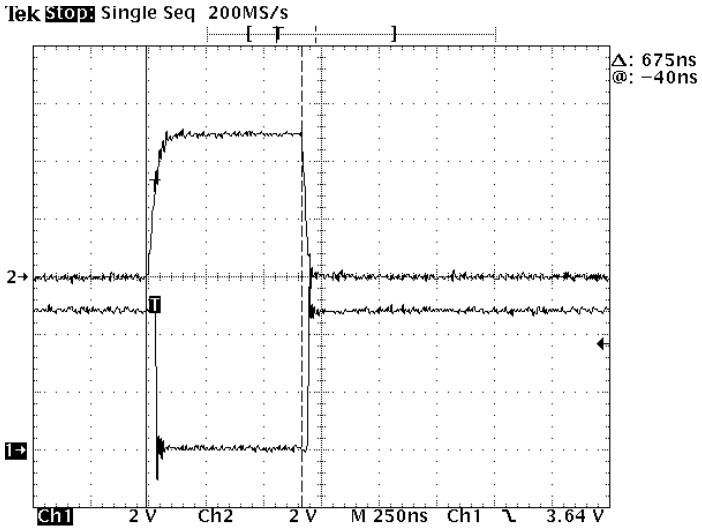

Figure 3.5
Test signal and A2 signal

3.2.3 Digital Signal Processing Board (TV-4B), ID. 68323

All the receivers are connected to the TV-4B. This printed circuit board comprises the digital electronic circuitry which processes the data from the receivers and transmits, in serial form, the information on irradiation to the indicator, generates the RTI output signal and generates the direct receivers' self-test signal. This board also provides power supply to the receivers.

Digital signals from the receivers are led to PLD (Programmable Logic Device) IC1. This fast circuit latches data for micro controller, disables belated signals caused by reflected laser pulse from nearby object and generates the RTI1 output signal. Power supply voltage for IC1 is 3.3V, generated from 5V by means of IC5. IC1 tolerates 5V amplitude of input signals. After detection IC1 triggers interrupt to the micro controller IC3. The micro controller then reads data from IC1, determines the direction of incoming laser irradiation and transmits the information, in the serial form to the indicator.

When detected signals from receivers are: A1, B1, A3 or/and B3, output data is generated after approximate 40us. In case when detected signals are: A2 or/and B2, output is generated only if in short time before 15 pulses are detected. In thic case RTI1 signal is not generated.

After 500 ms from the power-up, the microcontroller carries out the self-tests of the direct receivers, TV-4B logic and power supply voltages. Self-test of direct receivers is performed with assistance of IC4 and transistors V2 to V11. The outcome information of the self-test is transmitted to the indicator unit.

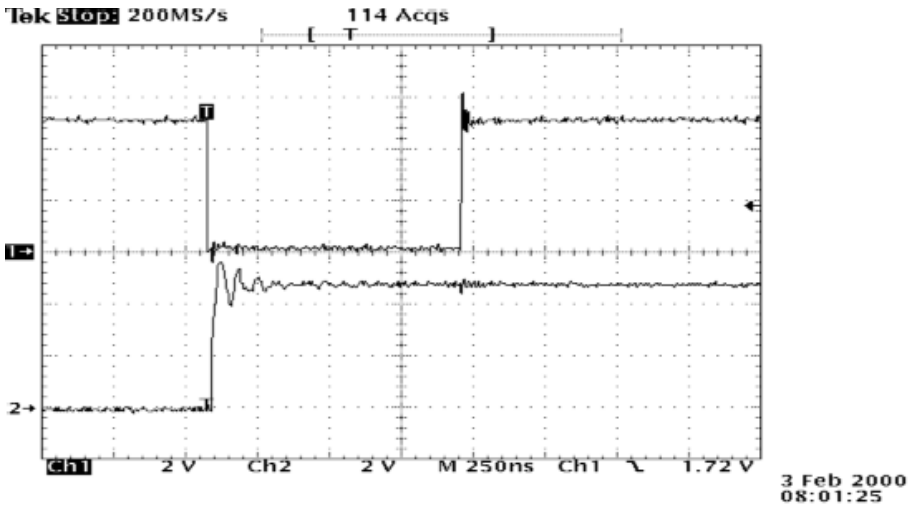

Figure 3.6
Signals: A1 and RTI+

The timing diagram on Fig. 3.6 shows the direct receiver signal 1A, which results from irradiation by a laser simulator. The length of the impulse may vary depending on the irradiation intensity and shape. It may happen that two impulses occur within a several hundred ns interval. In the subsequent processing, the relevant event is the first negative transition. All of the above applies also to the following signals: A3, B1, B3 . The lower trace on the figure shows the RTI+ signal, which is generated by the TV-4B as the result of the signal shown above.

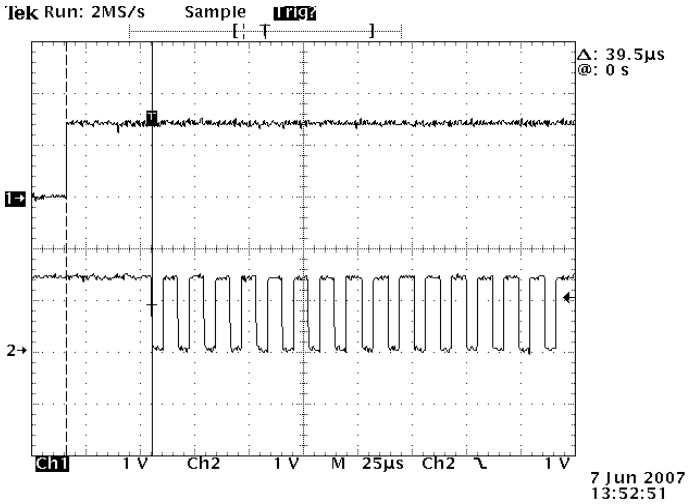

Figure 3.7
Signals: RTI1 and TAKT1

The figure shows the RTI1 signal (upper trace) and the TAKT1 (CLOCK) signal (lower trace) which serve in the synchronous transmission of the irradiation data from the detection module to the indicator module. In the above figure, the delay from the RTI1 signal and the transmission of irradiation data is 39,5 μs. Depending on the case of irradiation, the delay is different and may vary in the range of up to several tens of 10μs.

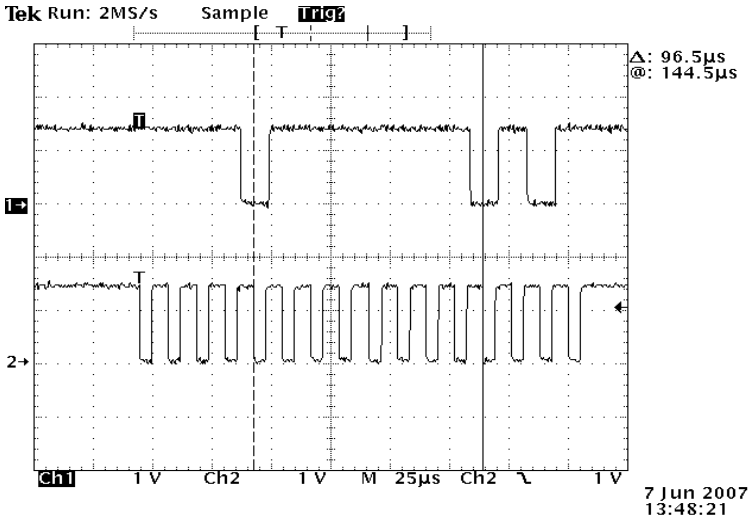

Figure 3.8
Signals: SIGNAL1 and TAKT1

The figure shows SIGNAL1 (upper trace), and the TAKT1 signal (lower trace). The amplitudes of these signals are cca 1,5V

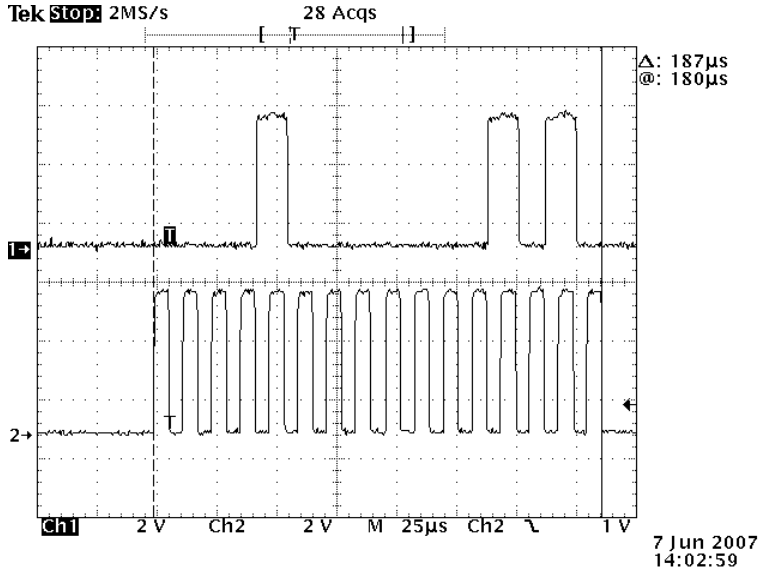

Figure 3.9
Signals: SIGNAL+ and TAKT+

In the subsequent processing, the relevant event is the value of the SIGNAL+ signal in the moment of the positive transition of the TAKT+ signal. Thus, the figure shows the value LLLLHLLL LLLLHLHL (15, 14, . . ., 0) of the SIGNAL signal. The first transmitted bit is bit 15, which is then followed by other bits in sequence to bit 0.

Bit 15 is L.

In the case of self-test data, the value of bit 14 is H.

Bit 13 is high only in the case of intensive irradiation by a rangefinder; otherwise it stays low.

Bit 12 is H in case of irradiation by a laser beam rider.

Bit 11 is H in case of irradiation by a laser rangefinder or laser designator.

Bit 10, 9 and 8 are low.

Bits 4, 3, 2, 1, 0 convey data on the direction of irradiation, bit 0 being the LSB. The direction 0 corresponds to irradiation from 180° and the value increases with the increasing angle. Direction 19 (HLLHH) corresponds to 162°. The figure above shows an example of irradiation from the direction 0°. (LHLHL – the tenth sector from the 180° direction).

In the case of transmitting a self-test result (bit 14 = H), the bits convey data on the result of the self-test. Positive result is indicated by bits 4,3,2,1 and 0 being H.

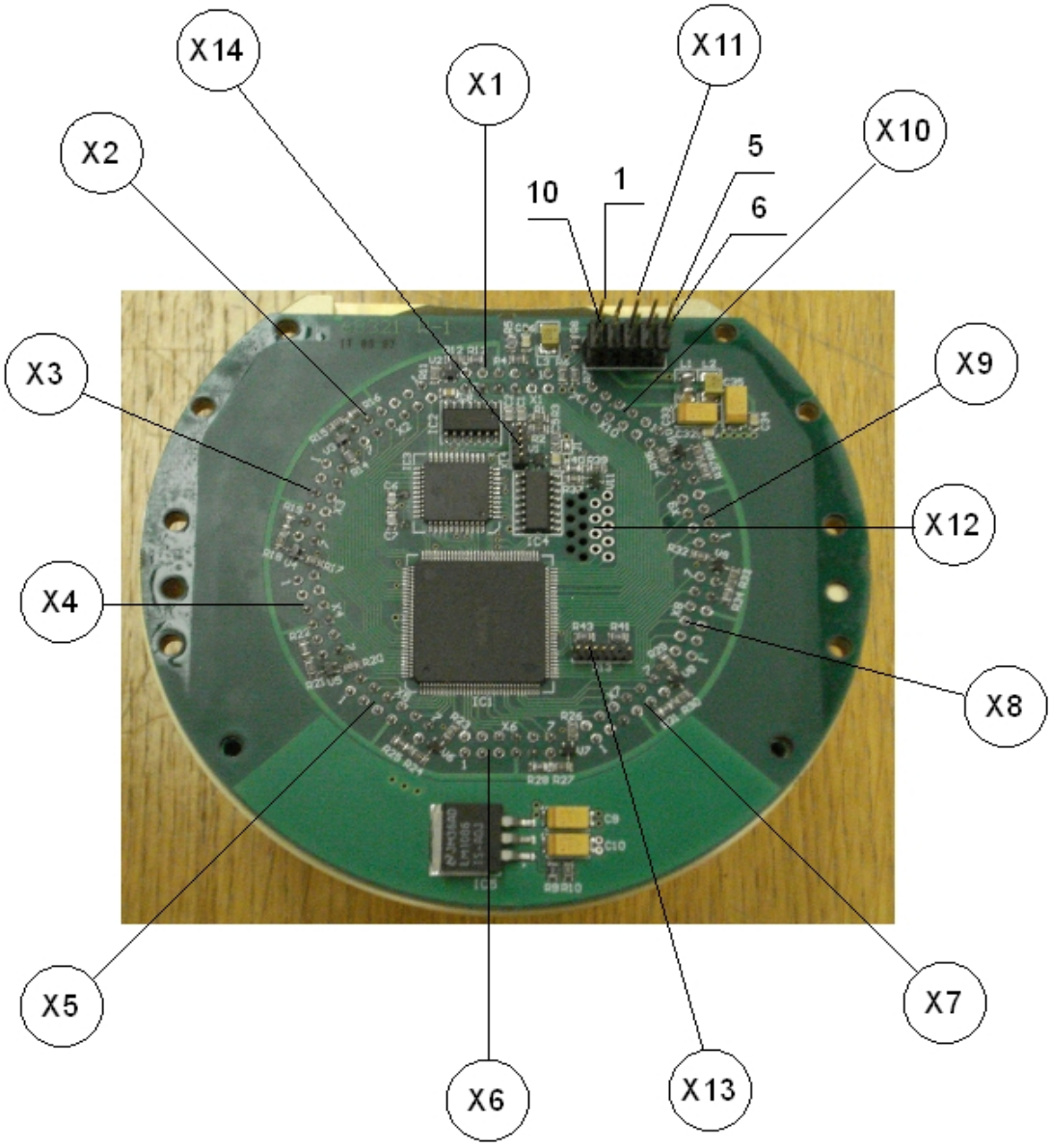

Figure 3.10
TV-4B – Bottom view (microcontroller side)

Fig. 3.10 shows the bottom view of the TV-4B. Except for the X11 all the connectors are located on the other side.

X1 – X10 connectors for connection to direct receivers
X11 connector to TV-2
1,2,5,6,10 arangement of pins (pin No.) on connectors

3.2.4 Power Supply & Line Drivers Circuit (TV-2), ID. 59160

Power supply circuitry is located on TV2. From the 12V input voltage, the circuitry generates +5VS, -5VS and +35VS supplying the receivers and the digital electronic circuitry and a separate +5VC for supplying the serial interface port. The DC resistance between the input power supply voltage ground, receiver ground and the serial port ground exceeds 1 Mohm. The receiver ground is connected to the detection head housing.

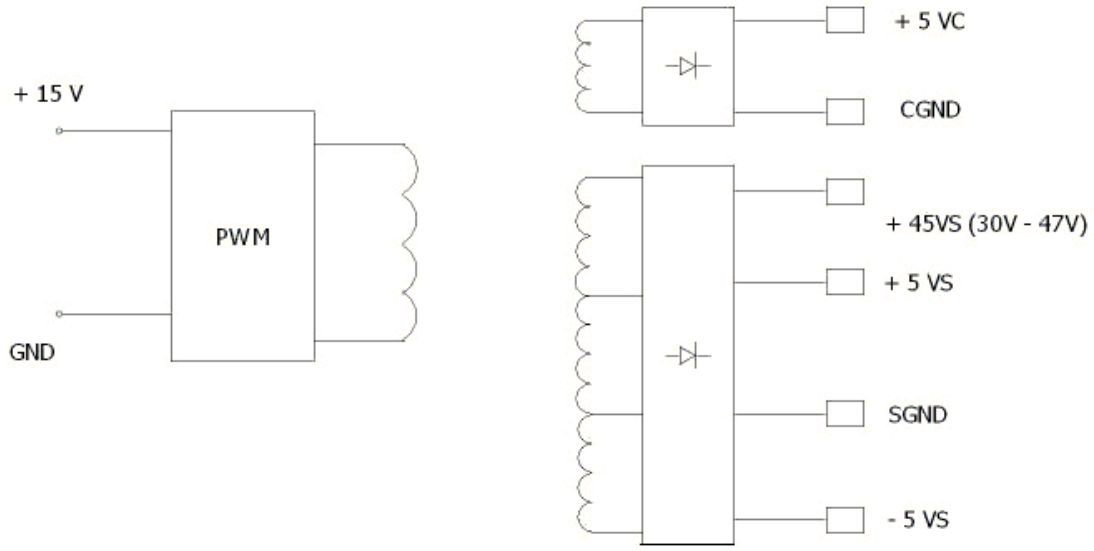

Figure 3.11
Power supply

Voltage + 5VS is 5 ± 0.1V
- 5VS is -5 ± 0.2V
+ 45VS is 30 to 47V
+ 5VC is 5 ± 0.4V

Serial Lines Controller (TV-2),

Serial Lines Controller is located on TV2. With the transmission of information to the indicator, the differential RS-422 transmission method is employed. From the digital processing output signals: RTI1, SIGNAL1 and TAKT1, the following signals are generated: RTI+, RTI-, SIGNAL+, SIGNAL-, TAKT+ and TAKT-. The differential transmission method enables reliable transmission of signals over distances exceeding 100 m.

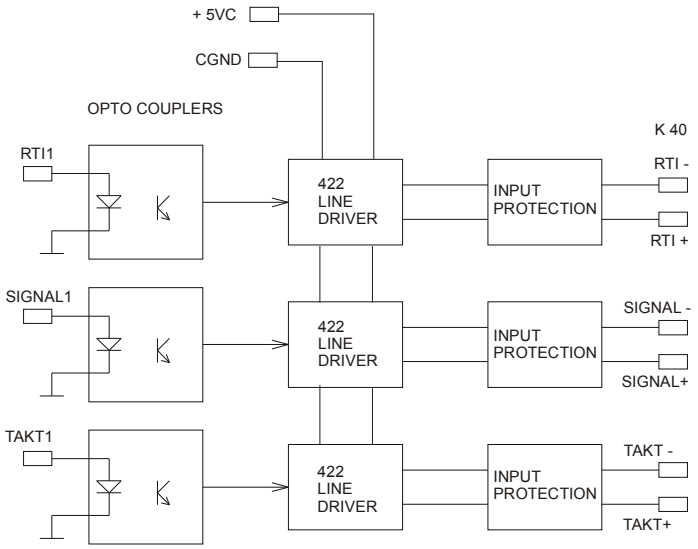

Figure 3.12
Serial lines controller

3.2.5 SIGNAL DESCRIPTIONS (in alphabetic order)

SIGNAL	PCB/CONNECTOR/PIN No.	SIGNAL DESCRIPTION
45V	TV-2/K1/5	35 V supply voltage generated on TV-2 assy.
	TV-4B/X11/5	
45VS	TV-4B/X1/1	35V supply voltage after filter on TV-4B assy.
	TV-4B/X2/1	
	TV-4B/X3/1	
	TV-4B/X4/1	
	TV-4B/X5/1	
	TV-4B/X6/1	
	TV-4B/X7/1	
	TV-4B/X8/1	
	TV-4B/X9/1	
	TV-4B/X10/1	
	TV-5B/X1/1	
+15V	K40/G	+15V input power supply voltage
5V	TV-2/K2/8	5 V supply voltage generated on TV-2 assy.
	TV-4B/X11/8	
+5VS	TV-4B/X1/4	5V supply voltage after the filter on TV-4 assy.
	TV-4B/X2/4	
	TV-4B/X3/4	
	TV-4B/X4/4	
	TV-4B/X5/4	
	TV-4B/X6/4	
	TV-4B/X7/4	
	TV-4B/X8/4	
	TV-4B/X9/4	
	TV-4B/X10/4	
	TV-4B/X12/3	
	TV-5B/X1/4	
-5V	TV-4B/X11/8	-5 V supply voltage generated on TV-2 assy.
	TV-2/K2/8	
-5VS	TV-4B/X1/3	-5V suplly voltage after filter on TV-4 assy.
	TV-4B/X2/3	
	TV-4B/X3/3	
	TV-4B/X4/3	

SIGNAL	PCB/CONNECTOR/PIN No.	SIGNAL DESCRIPTION
	TV-4B/X5/3	
	TV-4B/X6/3	
	TV-4B/X7/3	
	TV-4B/X8/3	
	TV-4B/X9/3	
	TV-4B/X10/3	
	TV-4B/X12/3	
	TV-5B/X1/3	
A1	TV-5B/X1/8	direct receiver output digital signal; 1st level, InGaAs photodiode; see fig. 3.5
A2	TV-5B/X1/11	direct receiver output digital signal; 2nd level, InGaAs photodiode; see fig. 3.5
A3	TV-5B/X1/7	direct receiver output digital signal; 3th level, InGaAs photodiode; see fig. 3.5
B1	TV-5B/X1/10	direct receiver output digital signal; 1st level, Si photodiode; see fig. 3.5
B2	TV-5B/X1/9	direct receiver output digital signals; 2nd level, Si photodiode; see fig. 3.5
B3	TV-5B/X1/12	direct receiver output digital signal; 3th level, InGaAs photodiode; see fig. 3.5
GND	K40/A	detector head input power supply ground
IND	TV-4B/X12/8	indirect receiver output digital signal
RTI1	TV-2/K2/4	real time signal generated on TV-4 assy.; see fig.3.5
	TV-4B/X11/4	
RTI+	K40/H	RS 422 + output real time signal, generated from RTI1 signal by line drivers on TV-2 assy.
RTI-	K40/D	RS 422 - output real time signal, generated from RTI1 signal by line drivers on TV-2 assy.
S1A1	TV-4B/K1/8	direct receiver output digital signal; 1st level, InGaAs photodiode; see fig. 3.5
S2A1	TV-4B/X2/8	
S3A1	TV-4B/X3/8	
S4A1	TV-4B/X4/8	
S5A1	TV-4B/X5/8	
S6A1	TV-4B/X6/8	
S7A1	TV-4B/X7/8	
S8A1	TV-4B/X8/8	
S9A1	TV-4B/X9/8	
S10A1	TV-4B/X10/8	
S1A2	TV-4B/X1/11	direct receiver output digital signal; 2nd level, InGaAs photodiode; see fig. 3.5
S2A2	TV-4B/X2/11	

SIGNAL	PCB/CONNECTOR/PIN No.	SIGNAL DESCRIPTION
S3A2	TV-4B/X3/11	
S4A2	TV-4B/X4/11	
S5A2	TV-4B/X5/11	
S6A2	TV-4B/X6/11	
S7A2	TV-4B/X7/11	
S8A2	TV-4B/X8/11	
S9A2	TV-4B/X9/11	
S10A2	TV-4B/X10/11	
S1A3	TV-4B/X1/7	direct receiver output digital signal; 3th level, InGaAs photodiode; see fig. 3.5
S2A3	TV-4B/X2/7	
S3A3	TV-4B/X3/7	
S4A3	TV-4B/X4/7	
S5A3	TV-4B/X5/7	
S6A3	TV-4B/X6/7	
S7A3	TV-4B/X7/7	
S8A3	TV-4B/X8/7	
S9A3	TV-4B/X9/7	
S10A3	TV-4B/X10/7	
S1B1	TV-4B/X1/10	direct receiver output digital signal; 1st level, Si photodiode; see fig. 3.5
S2B1	TV-4B/X2/10	
S3B1	TV-4B/X3/10	
S4B1	TV-4B/X4/10	
S5B1	TV-4B/X5/10	
S6B1	TV-4B/X6/10	
S7B1	TV-4B/X7/10	
S8B1	TV-4B/X8/10	
S9B1	TV-4B/X9/10	
S10B1	TV-4B/X10/10	
S1B2	TV-4B/X1/9	direct receiver output digital signals; 2nd level, Si photodiode; see fig. 3.5
S2B2	TV-4B/X2/9	
S3B2	TV-4B/X3/9	
S4B2	TV-4B/X4/9	
S5B2	TV-4B/X5/9	
S6B2	TV-4B/X6/9	
S7B2	TV-4B/X7/9	
S8B2	TV-4B/X8/9	
S9B2	TV-4B/X9/9	

SIGNAL	PCB/CONNECTOR/PIN No.	SIGNAL DESCRIPTION
S10B2	TV-4B/X10/9	
S1B3	TV-4B/X1/12	direct receiver output digital signal; 3th level, InGaAs photodiode; see fig. 3.5
S2B3	TV-4B/X2/12	
S3B3	TV-4B/X3/12	
S4B3	TV-4B/X4/12	
S5B3	TV-4B/X5/12	
S6B3	TV-4B/X6/12	
S7B3	TV-4B/X7/12	
S8B3	TV-4B/X8/12	
S9B3	TV-4B/X9/12	
S10B3	TV-4B/X10/12	
S1TEST	TV-4B/X1/6	
S2TEST	TV-4B/X2/6	
S3TEST	TV-4B/X3/6	
S4TEST	TV-4B/X4/6	
S5TEST	TV-4B/X5/6	
S6TEST	TV-4B/X6/6	
S7TEST	TV-4B/X7/6	
S8TEST	TV-4B/X8/6	
S9TEST	TV-4B/X9/6	
S10TEST	TV-4B/X10/6	
SGND	TV-2/K2/10	detector head common ground for receivers and digital signal processing
	TV-4B/X1/5	
	TV-4B/X2/5	
	TV-4B/X3/5	
	TV-4B/X4/5	
	TV-4B/X5/5	
	TV-4B/X6/5	
	TV-4B/X7/5	
	TV-4B/X8/5	
	TV-4B/X9/5	
	TV-4B/X10/5	
	TV-4B/X12/6	
	TV-4B/X12/7	
	TV-4B/X11/10	
	TV-5B/X1/5	
	TV-6/K1/E	
SIGNAL1	TV-2/K2/2	a digital signal 8 bits in length - serial data

SIGNAL	PCB/CONNECTOR/PIN No.	SIGNAL DESCRIPTION
		transmission from detector head to the indicator unit;
SIGNAL+	K40/E	RS 422 + output signal, generated from SIGNAL1 by line drivers on TV-2 assy.
SIGNAL-	K40/F	RS 422 - output signal, generated from SIGNAL1 by line drivers on TV-2 assy.
TAKT1	TV-2/K2/1	a series of 8 digital pulses - synhronisation pulses for data transmission from detector head to indicator unit; see fig.3.8
	TV-4B/X11/1	
TAKT+	K40/C	RS 422 + output signal, generated from TAKT1 by line drivers on TV-2 assy.; see fig. 3.9
TAKT-	K40/B	RS 422 - output signal, generated from TAKT1 by line drivers on TV-2 assy.;
TEMP	TV-2/K2/7	not used in this version
	TV-4B/X11/7	
TEST	TV-5B/X1/6	during the self-test procedure, direct receivers are tested by means of this signal; see fig.3.5

3.3 INDICATOR UNIT

3.3.1 General description

The indicator unit is located in a solid box, consisting of two parts:

- upper housing assembly (ID. 76799)
- lower housing assembly (ID. 76846)

The upper housing assembly includes components for man/machine interfacing. through which a 4 x 7 segment display and LED indicators may indicate information on irradiation. There are 20 direction sectors altogether. Beside direction indicators there is also an ON/OFF indicator. The type of irradiation is represented by the LD (laser target designator), LR (laser rangefinder) indicators and BR (laser beam rider).

Bellow the disc there is TV-10 -assy. printed circuit board (ID. 59393), on which LED displays and indicators are located in such a way that they are positioned exactly as defined by the mask on the disc. Cable 6-assy. (ID. 59901) is connected to this PCB, connecting the following switches:
- ON/OFF switch,
- TEST/REPET. double return switch.

A silica gel is mounted on the exterior of the upper housing. The upper housing assembly and lower housing assembly are connected electrically with Cable 5 - assy. (ID. 51630).

The lower housing assembly is carrying connectors K10, K20 and K30. All the connector pins are soldered directly to TV-15A - assy. printed circuit (ID. 72895) which also includes power supply unit and input protection unit.

TV-7A - assy. printed circuit board (ID 76595) connects all the printed circuits in the lower assembly housing.

TV-8A - assy. (ID. 76705) is the control part of the indicator unit.

INDICATOR UNIT

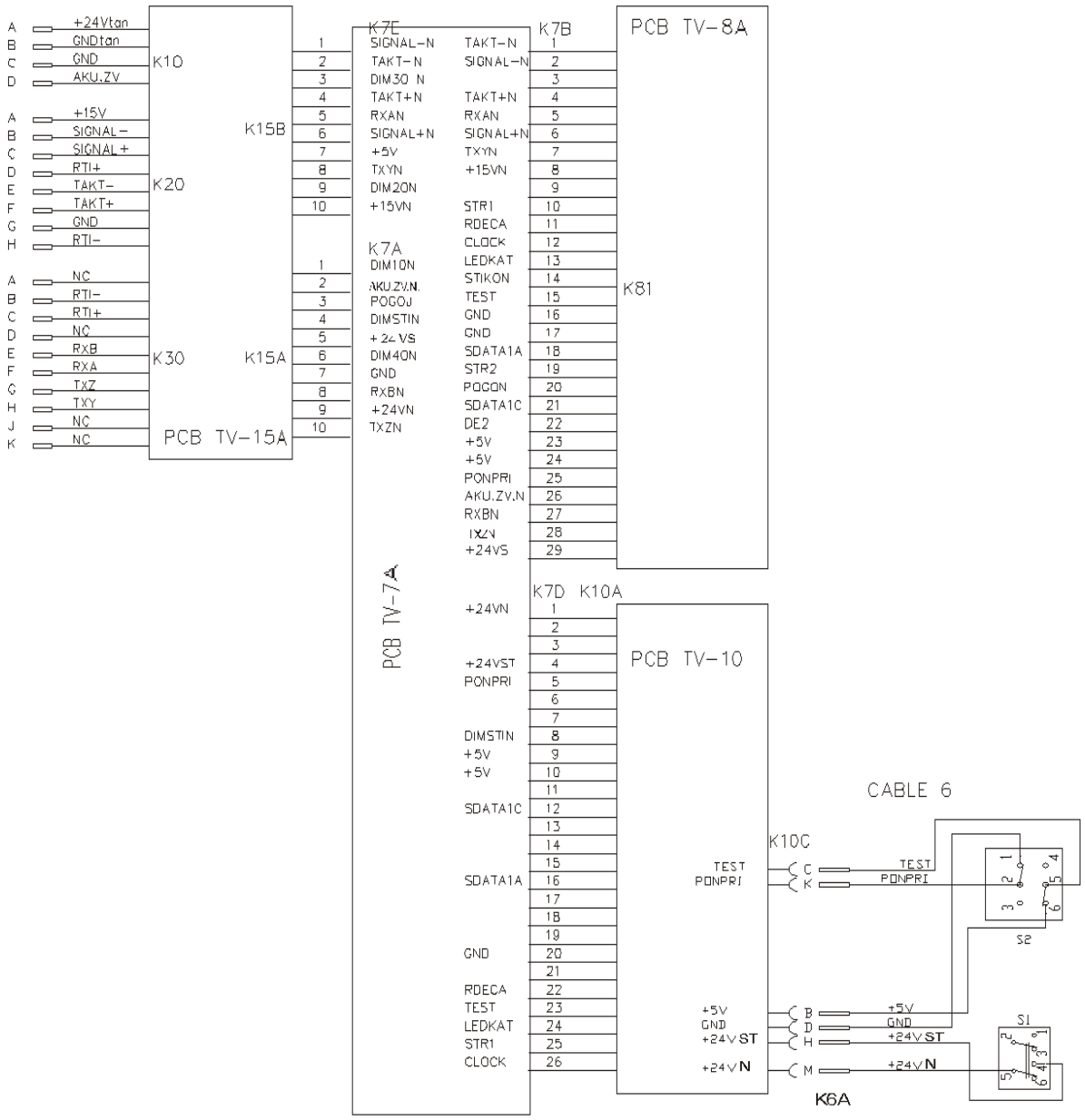

Figure 3.13
Indicator unit- block diagram

3.3.2 TV-7A-assembly

TV-7A-assy. (ID. 76595) connects the TV-8A-assy., TV-15A-assy. and via cable TV-10-assy.

3.3.3 TV-8A -assembly

TV-8A-assy. (ID. 76705) comprises the following functional entities:

- processor circuitry
- circuitry for communication with the detector head
- circuitry for communication with external units
- circuitry for control of light indicators
- circuitry for loudspeaker control

3.3.3.1 Processor

The oscillator Q1 (11059 MHz) and the capacitors C21 and C22 assure the necessary ocilattions needed for the clock signal generation within the processor chip. The processor is an Intel 87C51 type micro controller (IC12). Two eight bit processor parts are organized such that one of them (pins P00-P07) acts as a data bus on which two shift registers of the synchronous serial communication circuitry are connected. Another part (pins P20-P27) which is driven directly by the upper address bus lines (A8-A15) is brought to 3 to 8 decoder (IC7). Six decoded addres lines are formed to address six peripheral units as follows:

0800HSHIFTL signal:	addresses the shift register IC11 (the lower data byte of the communication channel to the detector head
000HSHIFTH signal:	addresses the shift register IC10 (the upper data byte of the communication channel to the detector head
1800HWD signal:	used in watch-dog timer circuitry (IC5)
2000HSTR1 signal:	used to strobe serial data to the LED indicator controllers
2800HSTR2 signal:	used to strobe serial data to an auxilliary output controller (smoke discharge interface with LIRD-1A, not used with LIRD-4B)
3000HSHFTR signal:	a reset signal to the shift registers IC10 to IC11

The signals located on other two processor ports P1 (P10... P17) and P3 (P30... P37) are used for communication with other parts of the circuitry. These signals are as follows:

P10	SDATA1	serial data line to the drivers of LED diodes and output trigger signals (smoke discharges)
P11	CLOCK	clock for shifting the upper data
P12	SER.DATA.T1	serial data control signal to the processor
P13	OUTEN2	not in use with LIRD-4B
P14	STIKON	not in use with LIRD-4B
P15	TXE	not in use – logically high
P16	PO	goes logically low when the input voltage is lower than 18 V
P17	ZV	generation for driving the loudspeaker (via T1 and T2 transistors)
P30	RXD	receive line of the serial channel to external units
P31	TXD	transmit line of the serial channel to external units
P32	TAKT	synchronization signal of the serial communication to the detector head (interrupt triggering)
P33	ponpri	signal from the REPET. return switch
P34	TAKT	synchronization signal (counting the number of clock passages)
P35	TEST	signal from the TEST return switch
P36	WR	write signal (logically low when the processor is entering data)
P37	RD	read signal (logically low when the processor is reading data)

The IC5 (MAX693) watch-dog circuit ensures correct processor operation. This circuit resets the processor when the processor does not change the status of the 1800HWD signal within every 1.6 sec. In addition to that this circuit monitors the 24V supply voltage and in case of voltage drop below 18V the pin P16 on the microcontroller is brought low. The processor in such a case stops all activities as long as this pin is low. The state is indicated by blinking the ON LED on the indicator panel.

3.3.3.2 Circuitry for communication with the detector head

Communication with the detector head is carried out via four signals. The TAKT+ and the TAKT- signals are the clock for entering the data into the IC10 and IC11 shift registers (54HC299). The data, being entered into the registers, are coming via SIGNAL+ and SIGNAL- signals. Before these signals enter the registers, they are translated into normal CMOS signals by means of the IC2 differential receiver (DS 78C120)

Each time the detector head senses a laser beam, a data package arrives via the above mentioned signals. In this package the TAKT signal performs sixteen positive passages, which enter the data (SIGNAL) into the eight memory cells of the shift registers. The TAKT signal is also led into the processor to two other inputs - the input for interrupt 0 and the input for timer 0 T0. On the first passage of the TAKT signal the interrupt is triggered, to the CPU triggering the program subroutine for reading the contents of the shift registers. In this subroutine the processor waits for a while and then checks whether the contents in the shift registers are correct and whether there have been 16 passages carried out (16 clock transitions). It also checks with what frequency the data packages are reaching the registers and, if everything is all right, the subroutine enables the output to the light indicators and the output to the serial port.

The data coming from the detector head are arranged in eight-bit words as described with the detector unit.

3.3.3.3 Communication with external devices

Data transmission for communication with external devices is of a RS422 or RS 232 type with the transmission speed of 9600Bd, 1 stop bit, no parity.

The data exchange is basically organized in one way, transmit only type, with the LIRD-4B transmitting data packages autonomously at

- startup (startup & self test message),
- after every detected laser threat event,
- each time the REPET. return switch is activated (information from memory).
- when the detector head is disconnected or ripped off (error message).

In addition to that the external device may send requests at any time to trigger re-transmission of certain information. This transmit/receive data line allows further improvement or sophistication of the data protocol explained below. For the same reason the data message contains more bytes of information than presently needed as well as the possibility to extend the length of the messages. Not used bytes or bits are designated with NU.

The structure of the data messages currently used is as follows:

Transmit:
(seven data byte message)
XX_h block begin
07_h No. of bytes
XX_h data control byte
AH address H
AL address L
D0 data byte
D1 data byte
D2 data byte
D3 data byte
XX_h checksum

Receive:
(one data byte request message)
XX_h block begin
01_h No. of bytes
XX_h data control byte
XX_h checksum

BLOCK BEGIN:

This is a constant value byte designating all LIRD data messages from any other messages in case a multi node data transmission line is implemented. In addition to that the block begin byte tells the receiving end what type of LIRD-4B is connected regarding the angle unit for the threat direction (sector) angle:

$3A_h$ - block begin character for messages with angle values in degrees (360º);
$3B_h$ - block begin character for messages with angle values in mils (6300 mil).

As each particular LIRD-4B device works with the angle unit that is used on engravings on the control panel of the indicator unit, the block begin character implicitly tells the receiving end which type of LIRD-4B is connected. When receiving a request message the device will not respond to messages not containing the same block begin character as transmitted in it's data messages.

No. of BYTES:

The second byte in the message contains the number of bytes that follow before the last byte in the message - the checksum byte. The total length of the data message is therefore the value of **No. of bytes** plus 3. As shown above the total length of the messages transmitted by the LIRD-4B is always10 and the total length of the messages expected at the LIRD-4B's receiving input is always 4.

CHECKSUM:

The checksum byte, the last byte in the message, contains a binary value that is to be added to the sum of all other bytes in the message including the block begin character. The sum obtained in that way, truncated to the least significant byte, should give zero result. Any non-zero result would mean that the data message has not been received correctly.

3.3.3.3.1Data messages transmitted to external devices

DATA CONTROL BYTE:

In this byte various flags and codes are given as follows:

1) In data messages (bit D7 = 0):

D7	D6	D5	D4	D3	D2	D1	D0
0	NU (0)	NU (0)	NU (0)	NU (0)	1 - BR (0)	**0** - DIR **1** - IND	**0** - LR **1** - LD

examples: 01_h - **D**irect hit**,** **L**aser **D**esignator
02_h - **I**ndirect hit, **L**aser **R**angefinder
04_h - BR

2) In the startup (self test) message (bit D7 = 1):

D7 D7	D6 D6	D5 D5	D4 D4	D3 D3	D2 D2	D1 D1	D0 D0
1	X	X	X	X	X	X	X

Error Code Bits

Error code Bits:
0000000 - no errors, self test is OK
0000001 - ERROR 1: PCB TV-4 is in malfunction,
0000010 - ERROR 2: Direct receivers in improper state
0000100 - ERROR 4: No supply voltage on photo-diodes
0001000 - ERROR 8: Direct receivers not responding properly on 2A
0010000 - ERROR16:Direct receivers not responding properly on 2B

The tests producing these codes are independent of each other and may all return an error condition. Therefore all the error codes from ERROR1 (0000001) to ERROR31 (0011111) are possible. The codes not listed above mean a combination of two or more error states. The two MS bits are reserved for further improvements.

A special error code:

1000000 - ERROR64 (equivalent to ERROR0 shown on the panel) is used to alarm the state when the detector head is disconnected (or ripped off).

Except for the detector head alarm test, which is performed continually (ON-LINE), all other tests are done only at startup. The results of the tests are contained in the self test message. See the troubleshooting section of the manual for details about error codes.

ADDRESS H,L bytes:

When the data message is containing the **currently detected** laser threat event, then the address value is zero:
Address H = 00_h
Address L = 00_h.

Address H,L value other than zero is a BCD address of the laser threat data stored and kept in a memory location after power-on of the device as follows:

Address H,L = 00_h 01_h - the most recent laser threat event stored in the memory,
Address H,L = 02_h 00_h - the oldest possible (20^{th}) stored laser threat event.

Until all the 20 locations are filled up, the oldest laser threat address is less than 20. After filling up all 20 location the device maintains the last 20 events, omitting the oldest threat event each time a new event is detected and stored in the memory (FIFO principle).

DATA BYTES:
The four data bytes give in BCD form the direction (sector) from which the laser threat is coming and is sensed by the detector head.

Example: 00_h 03_h 06_h 00_h = 360.

The angular unit in which the value is given is designated by the unique block begin character.

EXAMPLES for DATA MESSAGES:

3A 07 00 00 00 00 00 00 00 BF = direct LR threat in sector 0 (º)
3B 07 00 00 00 00 00 00 00 BE = direct LR threat in sector 0 (mils)
3A 07 00 00 00 00 01 08 00 B6 = direct LR threat in sector 180 (º)
3B 07 00 00 00 03 01 05 00 B5 = direct LR threat in sector 3150 (mils)
3A 07 03 00 00 XX XX XX XX CS = indirect LD threat (º)
3B 07 00 00 02 03 01 05 00 B3 = direct LR, sector 3150, mem. 2 (mils)
3A 07 C0 00 00 XX XX XX XX CS = Selftest: detecor head alarm (º)
3B 07 80 00 00 XX XX XX XX CS = Selftest: OK (mils)

Bytes with XX have no meaning in the message and are to be disregarded.

3.3.3.3.2 Data messages received from external devices

Although it is possible to get along with one way data communication only, the LIRD-4B can receive and answer to some request messages, which can be very useful in certain situations. A typical situation in which such a request for data is needed from the external device is when the latter is switched on later than the LIRD-4B and needs to be updated with the state of affairs regarding the LIRD-4B and possible laser threats detected prior to that moment.

The LIRD-4B understands the following request messages received at its input, provided that the block begin character corresponds to the same block begin character that this particular LIRD-4B device is using in its own data messages:

1) Request for re-transmission of the last data message

3A 01 00 C5: Upon receiving this message the LIRD-4B will repeat the last data message sent at any earlier time after power on. In case of no laser threat events the repeated message will be the startup/self test message as it was emitted at power on.

2) Request for laser threat locations memory dump

3A 01 01 C4: Upon receiving this message the LIRD-4B will transmit, one after another, all the messages about events accumulated since startup. The last valid self-test message will be followed by a data message for each laser threat event stored in the memory, starting with the location containing the oldest event detected. In this way the first message after self-test report will also tell the receiving end how many stored threat events are altogether (the address L,H value of the oldest event detected).

In case there is no laser threat events stored in the memory, the self-test message will be the only message sent upon receiving this request.

3.3.3.3.3 Real Time Interface Signal

The main purpose of this signal is to provide a pulse which is preceding the data message as early as possible with regard to the moment of actual detection of the laser threat.

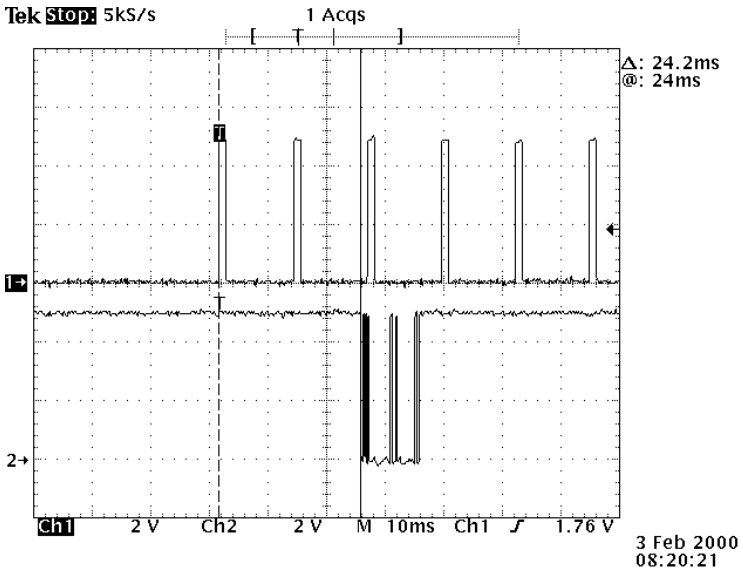

Figure 3.14
Signals: RTI+ and TXZ

The figure 3.14 presents, at the top, the RTI+ signal, and at the bottom, the TXZ signal, in the case of illumination by a handheld IR simulator in the LD mode of operation. With respect to the detection of the first illumination, the TXZ signal is delayed by 24 ms.

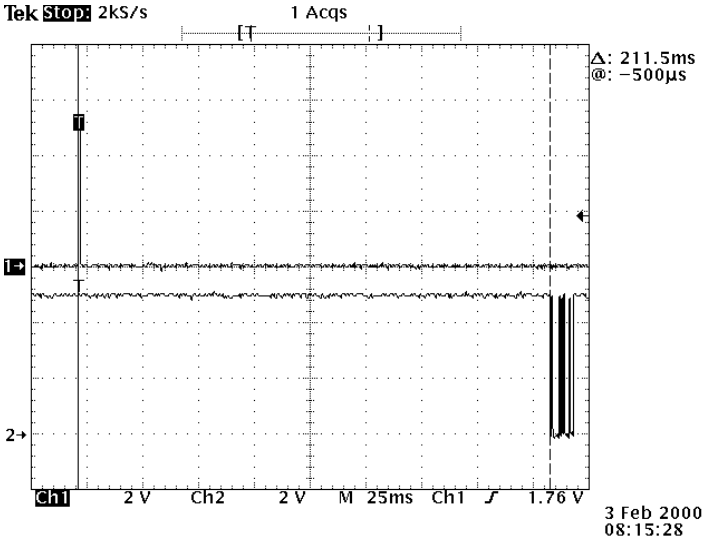

Figure 3.15
Signals: RTI+ and TXZ

The figure 3.15 presents, at the top, the RTI+ signal, and at the bottom, the TXZ signal, in the case of illumination by a handheld IR simulator in the LR mode of operation. The TXZ signal is delayed by 210 ms.

It can be noticed that the delay of the data message is varying a lot and therefore can not be used effective for exact determination of the laser threat appearance. On the other hand the RTI pulse is delayed for a few nanoseconds only and therefore much more conveniement for use in active counter measures.

3.3.3.4 Light Indicator Control Circuitry

A MIC5822 power driver with latch (IC1 on TV-8) and two MAX7219 serial display drivers (IC1, IC2 on TV-10) are used for this purpose. The serial data line SDATA1 from the processor first enters IC1 on TV-10 (SDATA1C signal) on the Data input pin DIN. The DOUT pin of the same IC is then connected to DIN of IC2 and from the DOUT pin brought back to the IC1 on TV-8 (signal SDATA1A). The serial data line is then looped back to the processor (signal SER. DATA.T1). The three serially interfaced chips are clocked with the same CLOCK signal and strobe signal STR1 strobe signals. The trains of information bits are serially shifted through this cascade-like connection and then strobed with STR1 signal for parallel transfer to the corresponding output control registers.

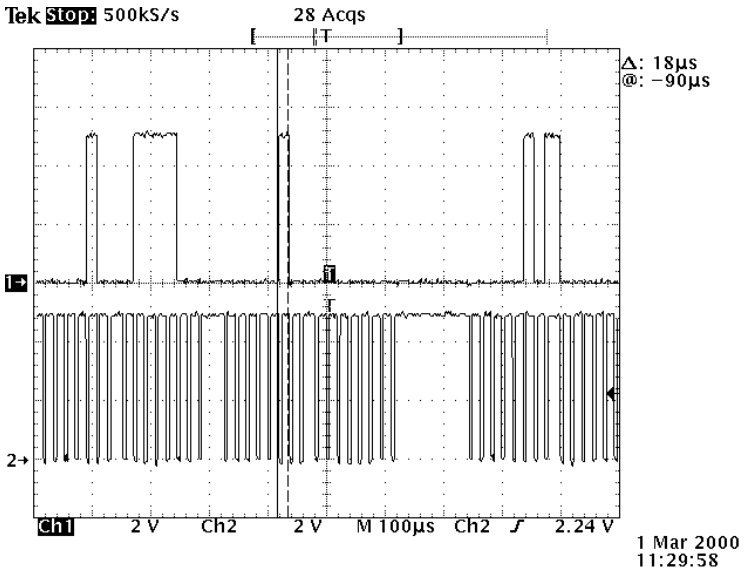

Figure 3.16
Signals: SDATA1A and CLOCK

The above figure presents a typical section of the SDATA1A (ch1) and CLOCK (ch2) signals. These signals serve for the transmission of data from TV-8A to TV-10. These signals are normally checked on the oscilloscope only for their shape rather than for their actual timing relations.

On the output of the IC1 and IC2 (TV-10) the necessarry time multiplexing for proper control of the seven segment LED display digits as well as the necessary current for driving the LED segments are all taken care of by these two powerful driver chips.

3.3.3.5 Test Loudspeaker Control Circuitry

The processor generates a tone signal via the ZV pin. The signal is amplified by the T1 and T2 transistors (BC109) located on the same PCB (TV8). The audio signal generated in such a way (AKU.ZV.N) is brought directly to K10.

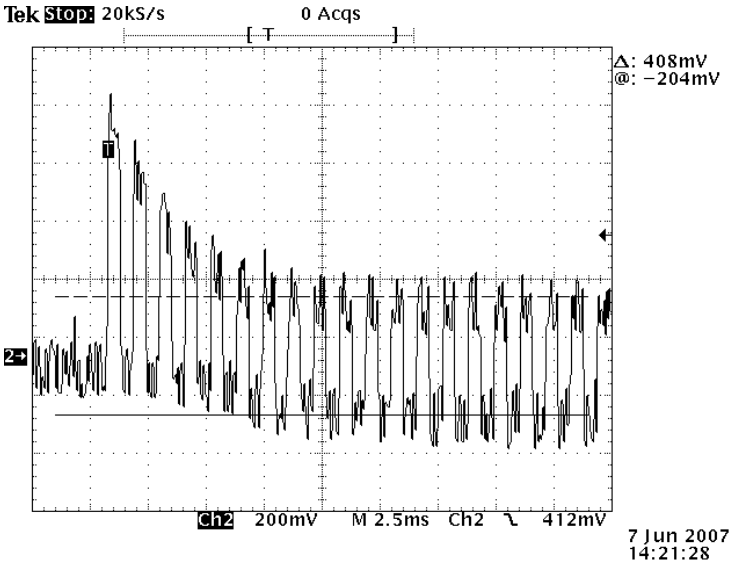

Figure 3.17
Signal: AKU.ZV on 150 OHMS RESISTOR

3.3.4 TV-10, ID. 59393

This printed board is connected, via Cable 5, to TV-7A. The board accommodates a 4 digit x 7-segment display, several LED diodes and the controller of all the display segments. The controller comprises of IC1 and IC2 (MAX7219). The controller receives data in serial form from the TV-8A processor. The LED diode current is set by R1 and R2.

The TV-10 board does not only accommodate the display elements on the indicator panel, but is also used as a relay board for Cable 6, the S1 on/off switch and the S2 TEST/REPET switch also located on the indicator unit.

3.3.5 TV-15A, ID. 72895

The TV-15A has all the three indicator module external connectors soldered to it. The printed board also includes +15V and +5V voltage regulators. It further accommodates the protection of the external connectors against incorrect voltage.

The input supply voltage +24Vtan to GNDtan is led through varistor protection against voltage peaks.

Via the K15A connector, the 24V power supply voltage is led to the TV-7A, from which it reaches the ON/OFF switch located on Cable 6 (via TV-10). It returns from the switch to TV-15A, where on the input is: voltage suppressor V3 against voltage polarity and pre-regulator against voltage surges over +40V.

Switching voltage regulator IC1 convert power supply voltage to +15VN (14 to 15 V). IC2 regulates this voltage to +5V (5 ± 0.1V).

The data signals present on the indicator module output connectors are protected by means of a varistor and a transient voltage supressor.

3.3.6 Cable 6, ID. 59901

Cable 6 is connected to TV-10-assy. printed circuit and connects switches with other electronics of the indicator.

A switch for switching the S1 of the indicator unit on/off (ON/OFF) is considered as part of this cable.

3.3.7 SIGNAL DESCRIPTION

SIGNAL	CONNECT/ CONTACT	SIGNAL DESCRIPTION
+15V	K20/A	15 V stabilized output voltage for the detector head power supply
+15VN	K15B/10	15 V stabilized voltage inside indicator unit
	K7E/10	
	K7B/8	
	K81/8	
+24VN	K15A/9	24 V supply voltage after the input protection and input filter
	K7A/9	
	K7D/1	
	K10A/1	
	K10C/M	
+24VS	K7B/29	24 V supply voltage after the filter on TV-7
	K81/29	
	K7A/5	
	K15A/5	
+24VST	K19C/H	24 V supply voltage after the ON/OFF switch
+24Vtan	K10/A	power supply input for the instrument
+5V	K15B/7	5 V supply voltage generated on TV-15
	K7E/7	
	K7B/23	
	K7B/24	
	K81/23	
	K81/24	
	K7D/9	

SIGNAL	CONNECT/ CONTACT	SIGNAL DESCRIPTION
	K7D/10	
	K10A/9	
	K10A/10	
	K10C/B	
AKU.ZV	K10/D	output signal for test loudspeaker
AKU.ZV.N	K15A/2	AKU.ZV signal before the input protection

SIGNAL	CONNECT/ CONTACT	SIGNAL DESCRIPTION
	K7B/26	
	K81/26	
CLOCK	K81/12	signal generated by the TV-8-assy. used for serial data transmission
	K7B/12	
	K7D/26	
	K10A/26	
DE2	K81/22	not used in LIRD-4B
	K7B/22	
DIM10N	K7A/1	not used in LIRD-4B
	K15A/1	
DIM20N	K7E/9	not used in LIRD-4B
	K15B/9	
DIM30N	K7E/3	not used in LIRD-4B
	K15B/3	
DIM40N	K7A/6	not used in LIRD-4B
	K15A/6	
DIMSTIN	K7A/4	not used in LIRD-4B
	K15A/4	
GND	K10/C	common indicator ground
	K15A/7	
	K7A/7	
	K7B/16	
	K7B/17	
	K81/16	
	K81/17	
	K7D/20	
	K10A/20	
	K10C/D	
GNDtan	K10/C	instrument input power supply ground
LEDKAT	K81/13	not used in LIRD-4B
	K7B/13	
	K7D/24	
	K10A/24	
POGOJ	K15A/3	not used in LIRD-4B
	K7A/3	
POGON	K7B/20	not used in LIRD-4B
	K81/20	
PONPRI	K81/25	signal from the TEST/REPET. switch
	K7B/25	
	K7D/5	
	K10A/5	

SIGNAL	CONNECT/ CONTACT	SIGNAL DESCRIPTION
	K10C/K	
RDECA	K81/11	not used in LIRD-4B
	K7B/11	
	K7D/22	
	K10A/22	
RTI+	K20/D	real time interface signal
	K30/B	
RTI-	K20/D	inverted RTI+
	K30/H	

SIGNAL	CONNECT/ CONTACT	SIGNAL DESCRIPTION
RXA	K30/B	signal for serial communication with external units
RXAN	K15B/5	signal RXA after the input protection
	K7E/5	
	K7B/5	
	K81/5	
RXB	K30/E	signal for serial communication with external units
RXBN	K15A/8	signal RXB after the input protection
	K7E/8	
	K7B/27	
	K81/27	
SDATA1A	K81/18	signal from TV-8 assy. to TV-10-assy.
	K7B/18	
	K7D/16	
	K10A/16	
SDATA1C	K81/21	signal for the indicator unit serial transmission of control signals from TV-8 assy. to TV-10-assy.
	K7B/21	
	K7D/12	
	K10A/12	
SIGNAL+	K20/B	digital signal 8 bit in length - serial data transmision from the detector head to the indicator unit
SIGNAL+N	K15B/6	SIGNAL+ after the input protection
	K7E/6	
	K7B/6	
	K81/6	
SIGNAL-	K20/C	inverted SIGNAL+
SIGNAL-N	K7E/1	SIGNAL- after the input protection
	K15B/1	
	K7B/2	
	K81/2	
STIKON	K81/14	not used in LIRD-4B

SIGNAL	CONNECT/ CONTACT	SIGNAL DESCRIPTION
	K7B/14	
STR1	K81/10	strobe signal used to transfer serially entered data bits to the corresponding output registers with the display segment control
	K7B/10	
	K7D/25	
	K10A/25	
STR2	K81/19	not used in LIRD-4B
	K7B/19	
TAKT+	K20/F	synhronization pulses for data transmision from detector to indicator unit a series of 8 digital pulses
TAKT+N	K15B/4	TAKT+ signal after the input protection
	K7E/4	
	K7B/4	
	K81/4	
TAKT-	K20/E	inverted TAKT+
TAKT-N	K15B/2	TAKT- signal after the input protection
	K7E/2	
	K7B/1	
	K81/1	
TEST	K81/15	signal arriving from the TEST/REPET. switch
	K7B/15	
	K7D/23	
	K10A/23	
	K10C/C	
TXY	K30/H	output RS 422 signal, communication with the environment
TXYN	K15B/8	TXY before the input protection
	K7E/8	
	K7B/7	
	K81/7	
TXZ	K30/G	RS 422 output signal, communication with external units
TXZN	K15A/10	TXZ before the input protection
	K7A/10	
	K7B/28	
	K81/28	

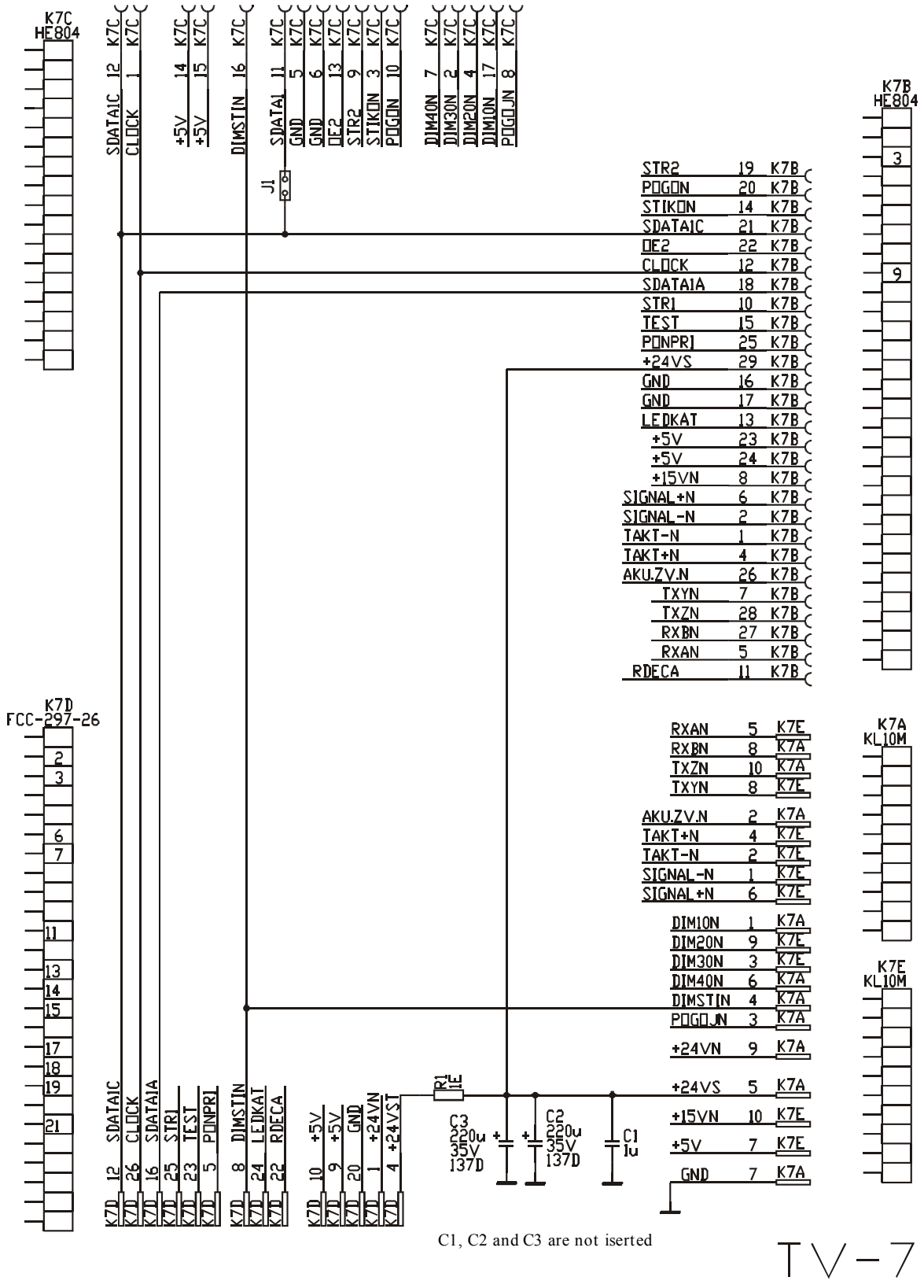

Figure 3.18
TV-7A block diagram

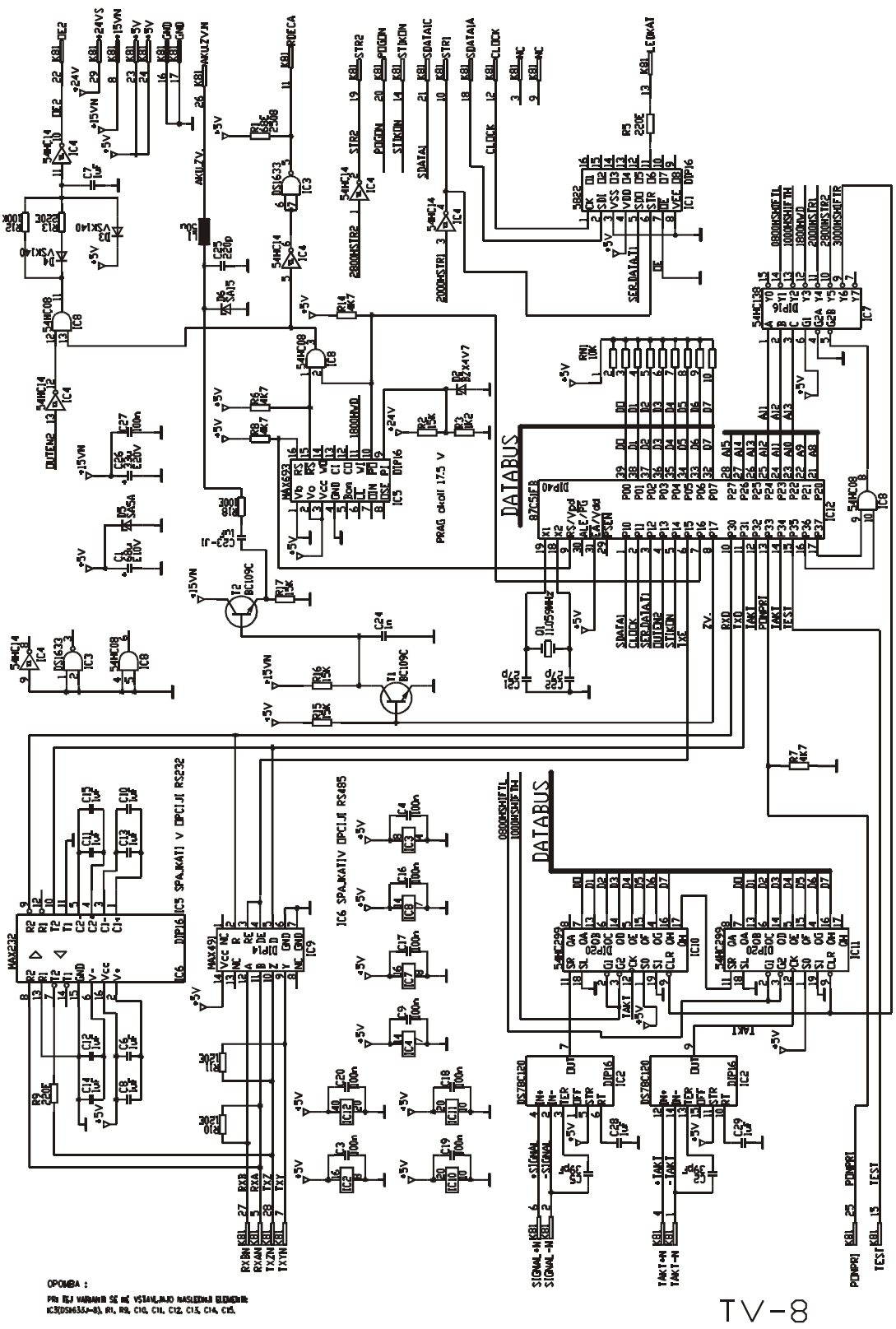

Figure 3.19
TV-8 block diagram

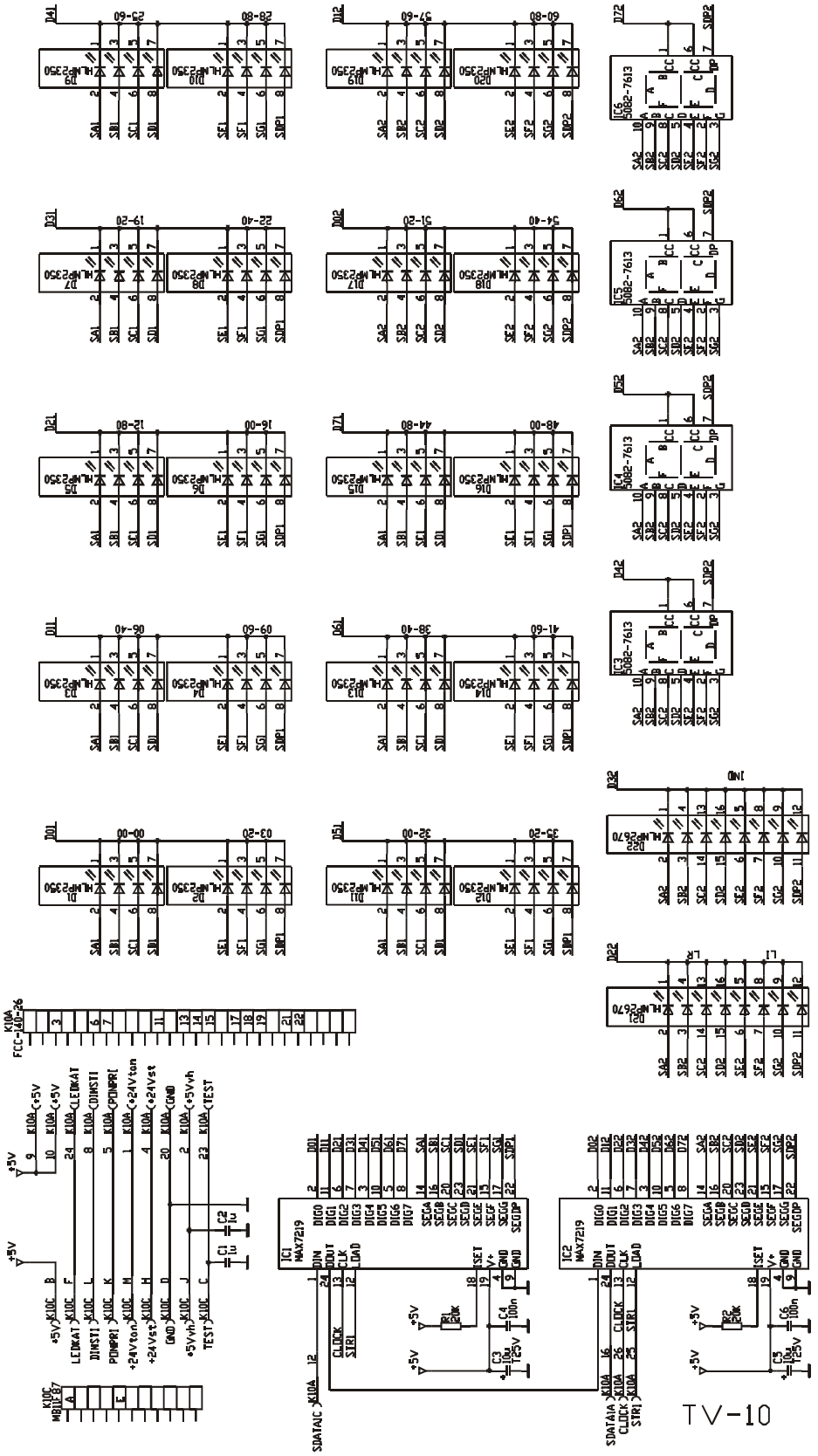

Figure 3.20
TV-10 block diagram

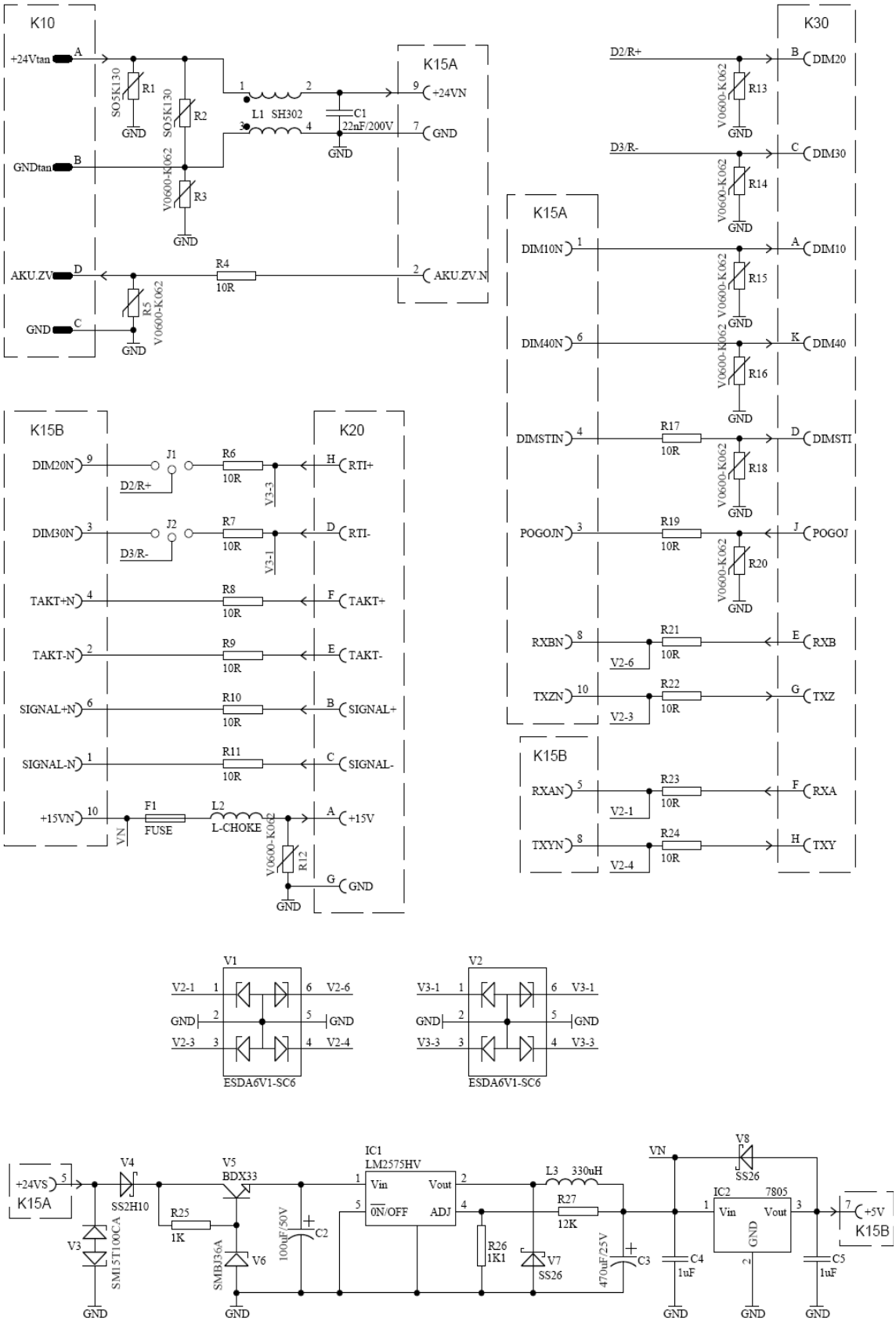

Figure 3.21
TV-15A block diagram