UAq EMC Laboratory

Corso di Integrità del Segnale

Class Project

Embedded capacitance e misure per Power Integrity

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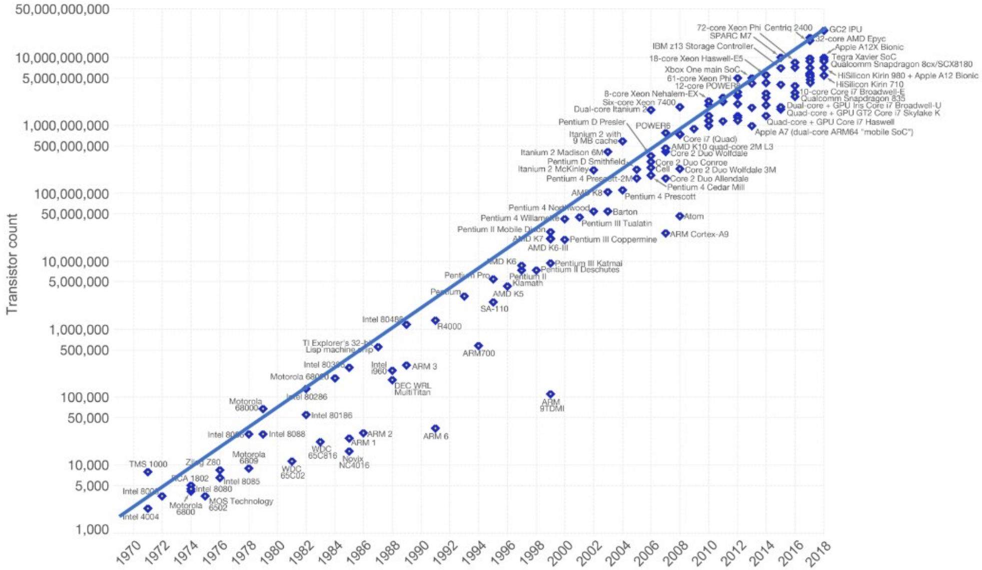
Introduzione



Legge di Moore (1971-2018)

Sfide per la Power Integrity (PI):

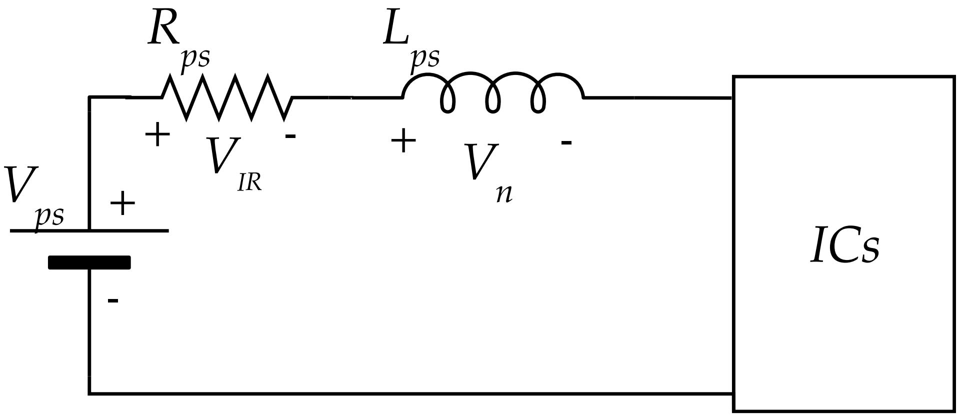
- Incremento densità di gates
- Incremento della densità di IC sulle schede
- Sistemi a velocità crescente
- Dispositivi low voltage

Richieste sempre più spinte per le reti di alimentazione

Rumore sull’alimentazione

- ***IR*-drop**: rumore proporzionale alla corrente I causato da R parassita
- ***ΔI* noise** : dipende dalla velocità di switching dei gate

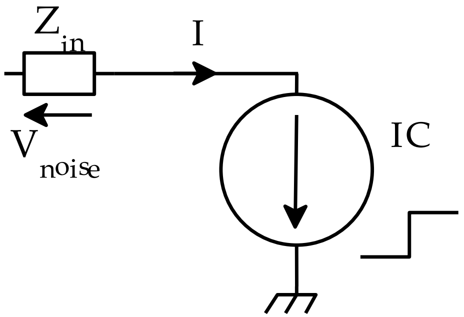
$$V_N = -L_{ps}\frac{di(t)}{dt}$$



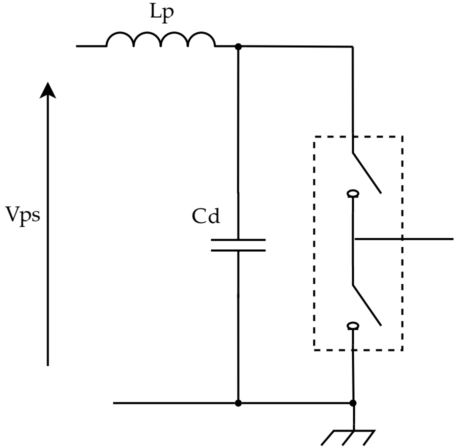
Necessità di ottenere PDN a bassa R_{ps} e bassa L_{ps} ⟶ ***minimizzare*** $\boldsymbol{Z_{in}}$

Power Decoupling

Nel dominio della frequenza: $V_{noise} = Z_{in}\, I$

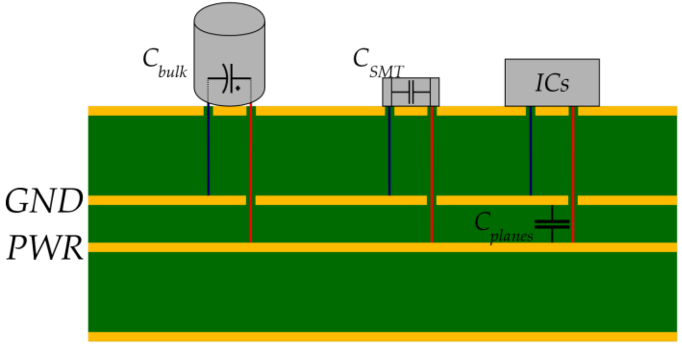


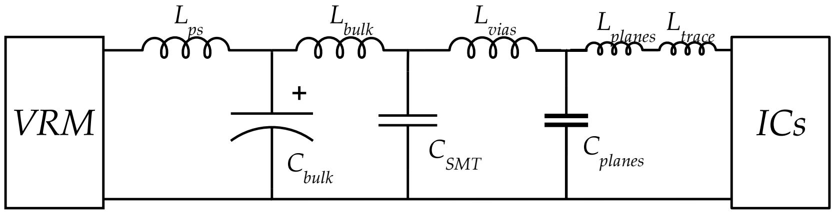
- $Z_{Lp} = j\omega L_p$ impedenza induttiva aumenta con f
- $Z_{Cd} = {}^{1}\!/_{j\omega C_d}$ impedenza capacitiva decresce con f

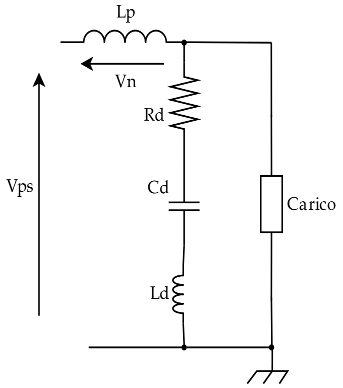


La capacità di disaccoppiamento C_d in parallelo introduce un percorso a bassa impedenza

Problemi di Decoupling

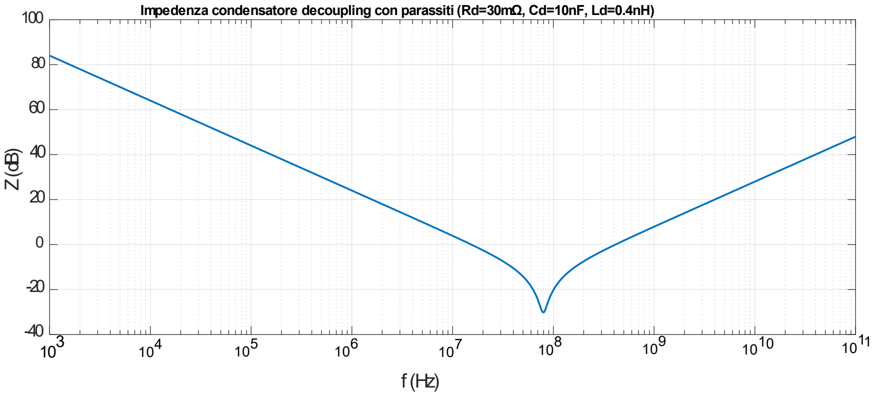






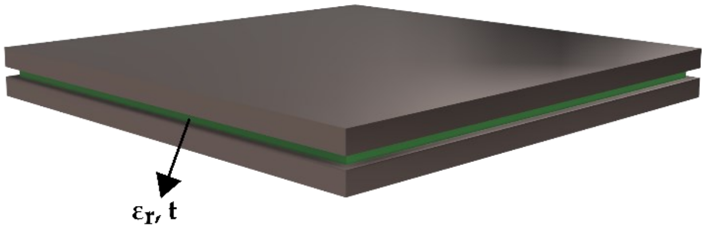
- I condensatori hanno ESL ed ESR non nulle
- Il montaggio introduce parassiti

Incremento indesiderato di Z_{in}

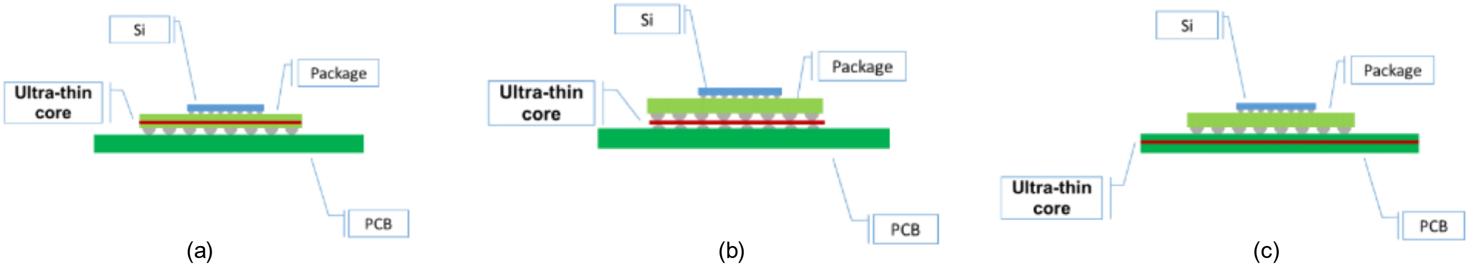


Embedded Capacitance

$$C = \varepsilon_o \varepsilon_r \frac{S}{t}$$

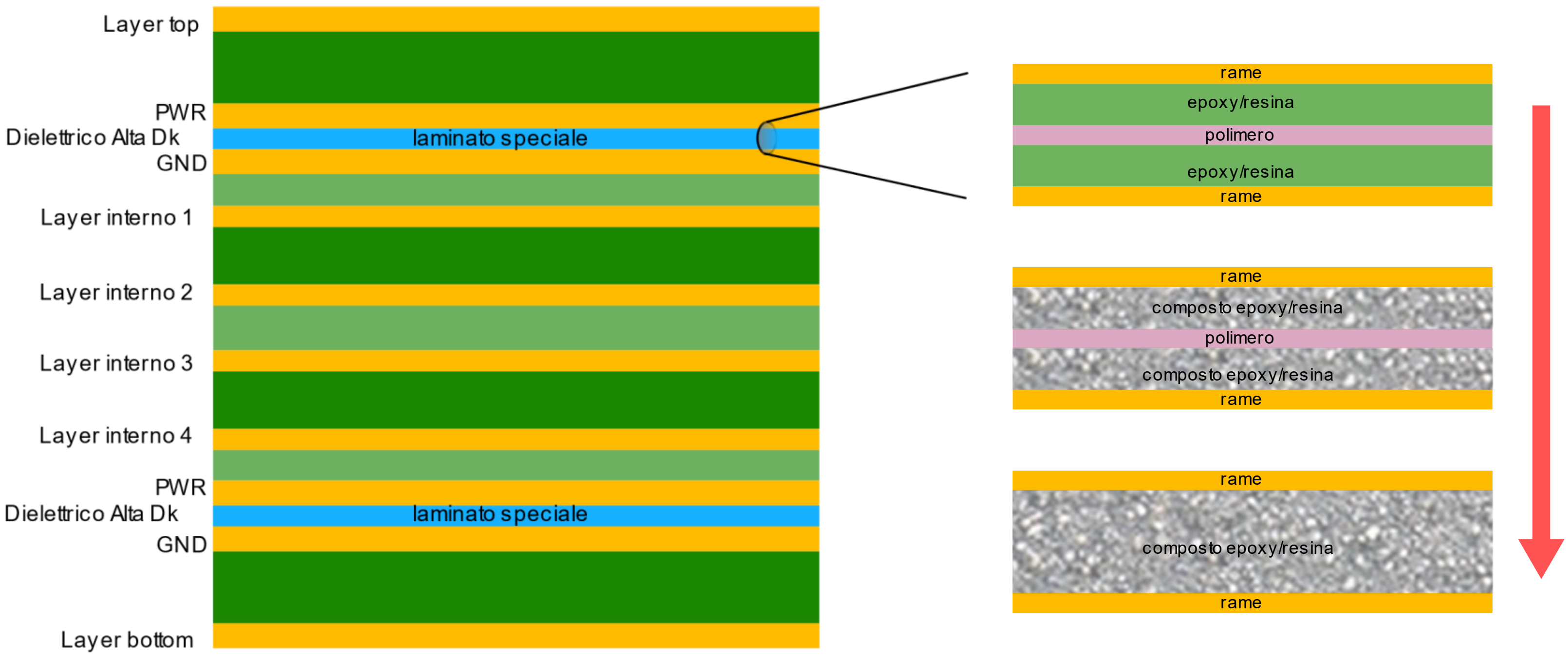


Livelli di implementazione dell'embedded capacitance



Minore L_{par}

Tipologie realizzative

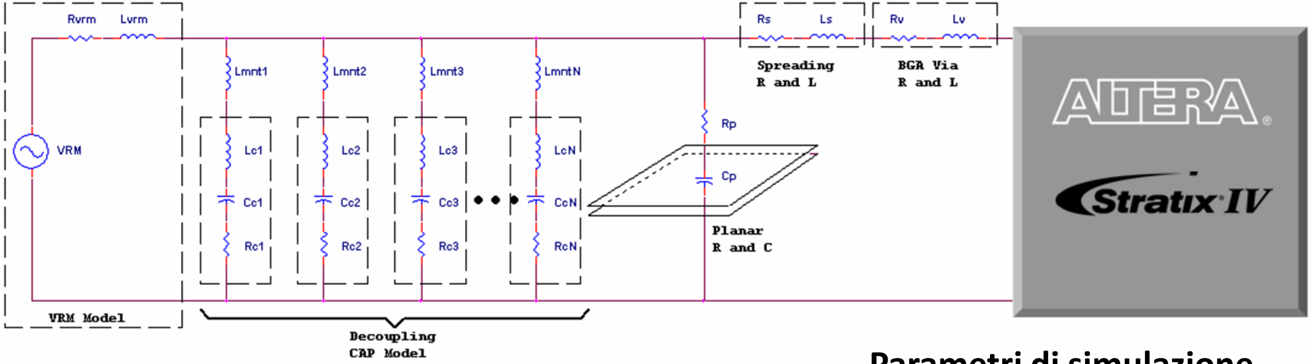


$€ \nearrow$

$\varepsilon_r \nearrow$

$V_{max} \searrow$

Simulazione PDN



$$I_{max} = 1.3A \qquad W = 10500\,mils$$

$$F_{effective} = 70MHz \qquad L = 5600\,mils$$

$$Z_{in} \leq Z_{target} = 68m\Omega$$

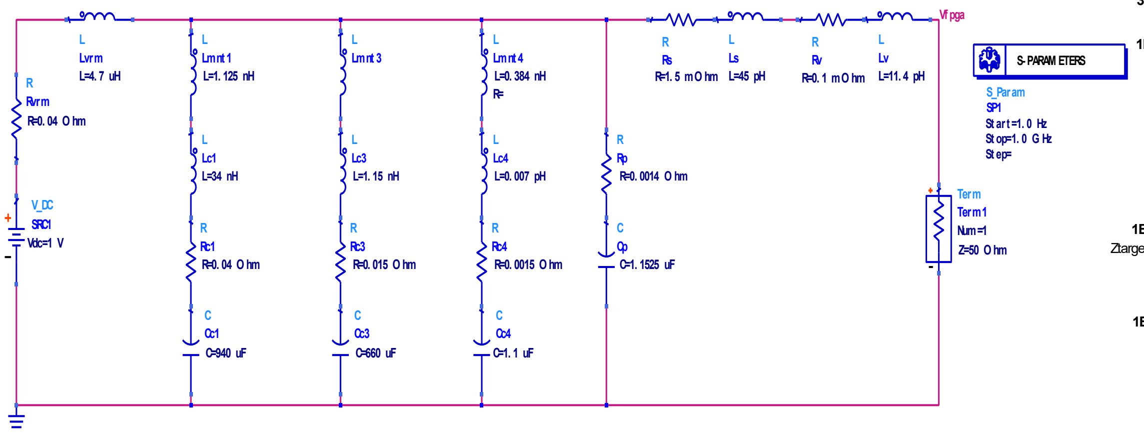
Parametri di simulazione

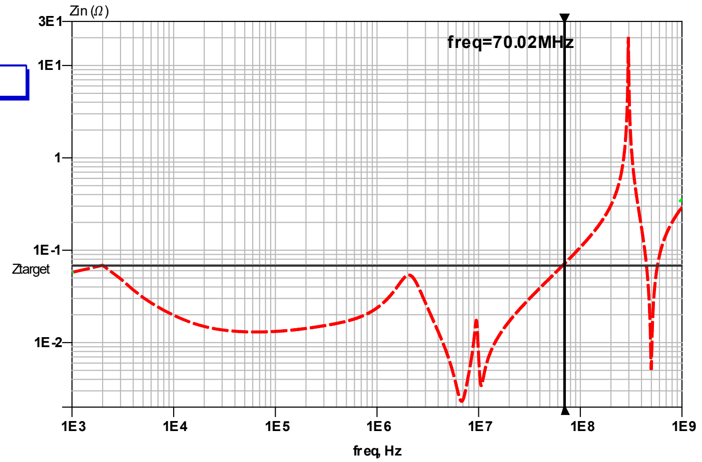
Bulk Cap (µF)	Bulk Custom ESR (Ω)	ESL (nH)	Lmnt (nH)
10	0,030	2,300	1,700
22	0,030	2,300	1,700
47	0,030	2,300	1,700
100	0,030	2,300	1,700
220	0,030	2,300	1,700
330	0,030	2,300	1,700
470	0,080	68,000	2,250

Summary	Options	R (Ω)	L (nH)	C (µF)
VRM	Custom	4,0E-02	4,7E+03	N/A
Spreading	High	0,0015	0,0450	N/A
BGA Via	Calculate	0,0001	0,0114	N/A
Plane Ca	Calculate	0,0014	N/A	0,0027

Decoupling Cap (µF)	Custom ESR (Ω)	ESL (nH)	Lmnt (nH)
0,001	0,001	0,300	1,000
0,0022	0,001	0,300	1,000
0,0047	0,001	0,300	1,000
0,01	0,001	0,300	1,000
0,022	0,001	0,300	1,000
0,047	0,001	0,300	1,000
0,1	0,008	0,035	1,920
0,22	0,008	0,035	1,920
0,47	0,080	28,000	2,300
1	0,080	28,000	2,300
2,2	0,001	0,300	1,000
4,7	0,080	28,000	2,300
User1	0,080	28,000	2,300
User2	0,080	23,000	2,450
User3	0,001	0,300	1,000
User4	0,001	0,300	1,000

Simulazione PDN: risultati FR4





Footprint	Valore (μF)	Quantità
SMT	0.1	10
SMT	0.22	8
bulk	330	2
bulk	470	2

$\varepsilon_r = 4.0\ {}^{F}/_{m}$ $\quad t = 20\ mils$

Condensatori totali: 22

Simulazione PDN: embedded capacitance

Properties	Test Method	Standard Dk			High Dk		Low Df
		MC24M	MC12M	MC8M	MC12TM	MC8TM	MC25L
Dielectric Thickness, µm	Nominal	22	12	8	12	8	25
Cp @ 1 MHz, nF/in² (pF/cm²)	Nominal	1.2 (180)	2.0 (320)	3.1 (480)	4.2 (650)	6.5 (1010)	1.0 (130)
Dk (Dielectric Constant) @ 1 MHz/1 GHz	Mitsui Method	4.4/3.5	4.4/3.5	4.4/3.5	10.0/9.5	10.5/10.0	3.9/3.8
Df (Loss Tangent) @1 MHz/1 GHz	Mitsui Method	0.015/0.016	0.015/0.020	0.016/0.021	0.015/0.020	0.020/0.021	0.004/0.005
Peel Strength, kN/m 1 oz Cu	IPC TM-650 2.4.8C*	1.5	1.5	1.5	0.9	0.9	1.0
Breakdown Voltage, V	IPC TM-650 2.5.6.2A*	≤5000	4000	3000	2500	1500	≤5000
Tensile Strength, MPa (kpsi)	ASTM D-882	219 (31.8)	194 (28.2)	126 (18.3)	153 (22.2)	127 (18.4)	227 (32.9)
Elongation, %	ASTM D-882A	36.0	13.5	8.5	31.4	14	47.0
CTE, ppm/°C, x-y, TMA	IPC TM-650 2.4.24.5*	24	23	32	28	22	30
Tg, °C, DMA	IPC TM-650 2.4.24.4*	183	187	188	189	191	170
Hi-Pot test (each panel)	IPC TM-650 2.5.7.2*	PASS (500V)	PASS (500V)	PASS (500V)	PASS (500V)	PASS (250V)	PASS (500V)
Thermal Stress (10 Sec Float @288°C), Times	Mitsui Method	>10	>10	>10	>10	>10	>10
Moisture Absorption %	TM-650 2.6.2.1*	1.3	1.3	0.5	0.8	0.5	0.3
THB, 85°C/85% RH/dc bias	Mitsui Method	PASS (50V)	PASS (50V)	PASS (35V)	PASS (50V)	PASS (35V)	PASS (50V)
HAST, 130°C/85% RH/dc bias	Mitsui Method w/GEA-700G	PASS (50V)	PASS (50V)	PASS (50V)	PASS (50V)	PASS (50V)	PASS (50V)
Flammability/Temp Rating	UL 94	V0 130°C	V0 130°C	V0 130°C	V0 130°C	V0 130°C	V0 130°C
PWB Processing	–	Both sides	Both sides	Both sides	Both sides	Both sides	Both sides

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Properties	Test Method	High Dk/Low Df		High Dk			
		MC12LD	MC12ST	MC8TM	MC8T	MC3TA	MC3TB
Dielectric Thickness, µm	Nominal	12	12	8	8	3	3
Cp @ 1 kHz/1 MHz, nF/in²	Nominal	- /4.3	10.9/10.5	7.0/6.5	24.2/21.9	40.0/36.7	40.0/38.5
Dk (Dielectric Constant) @ 1 kHz/1 MHz	Mitsui Method	7.3@1MHz 7.9@1GHz	23.1/22.8	10/10.5	30.0/24.0	23.0/21.0	22.4/21.7
Df (Loss Tangent) @1 kHz/1 MHz	Mitsui Method	0.002@1MHz 0.0017@1GHz	0.006/0.005	0.020/0.020	0.020/0.025	0.020/0.023	0.010/0.008
Peel Strength, kN/m 0.5 oz Cu	IPC TM-650 2.4.8C*	0.70	0.70	0.77	0.70	0.45	0.70
Breakdown Voltage, V	IPC TM-650 2.5.6.2A*	300	150	1500	200	50	50
Tensile Strength, MPa (kpsi)	ASTM D-882	N/A	NA	127 (18.4)	NA	NA	NA
Elongation, %	ASTM D-882A	N/A	NA	14	NA	NA	NA
CTE, ppm/°C, x-y, TMA	IPC TM-650 2.4.24.5*	55	32 (@1) 97 (@2)	22	17 (@1) 42(@2)	47 (@1) 153 (@2)	32 (@1) 121 (@2)
Tg, °C, DMA	IPC TM-650 2.4.24.4*	215	160	191	191	189	136
Hi-Pot test (Sampling/Lot)	IPC TM-650 2.5.7.2*	N/A	PASS (50V)	PASS (100V)	PASS (50V)	PASS (20V)	PASS (20V)
Thermal Stress (10 Sec Float), Times	Mitsui Method	>10 (288°C)	>10 (288°C)	>10 (288°C)	>10 (288°C)	>10 (300°C)	>10 (300°C)
Moisture Absorption %	TM-650 2.6.2.1*	0.37	0.14	0.5	0.4	0.2	0.2
THB, 85°C/85% RH/dc bias	Mitsui Method	PASS (10V)	PASS (3.7V)	PASS (35V)	PASS (3.7V)	PASS (3.7V)	PASS (3.7V)
HAST, 130°C/85% RH/dc bias	Mitsui Method w/GEA-700G	N/A	PASS (2.8V)	PASS (50V)	PASS (2.8V)	PASS (2.8V)	PASS (2.8V)
Flammability/Temp Rating	UL 94	N/A	NA	V0 130°C	V0 130°C	NA	NA
PWB Processing	–	Sequential	Sequential	Both sides	Sequential	Sequential	Sequential

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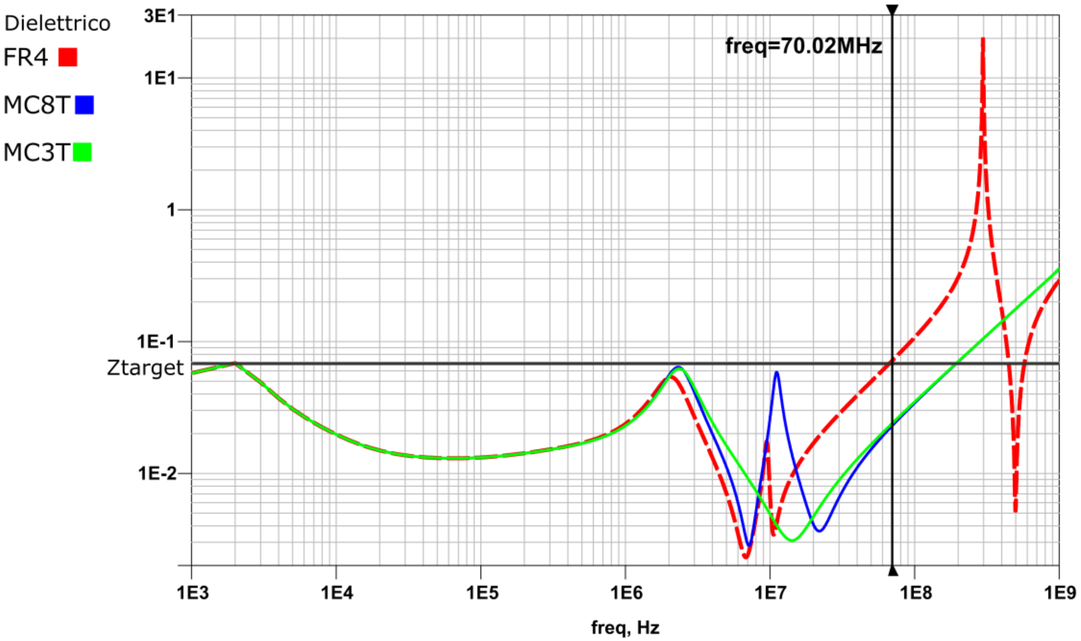
Simulazione PDN: risultati embedded capacitance



Laminato MC8T

Footprint	Valore (μF)	Quantità
SMT	0.22	5
bulk	330	2
bulk	470	2

Condensatori totali: 9

Laminato MC3T

Footprint	Valore (μF)	Quantità
bulk	330	2
bulk	470	2

Condensatori totali: 4

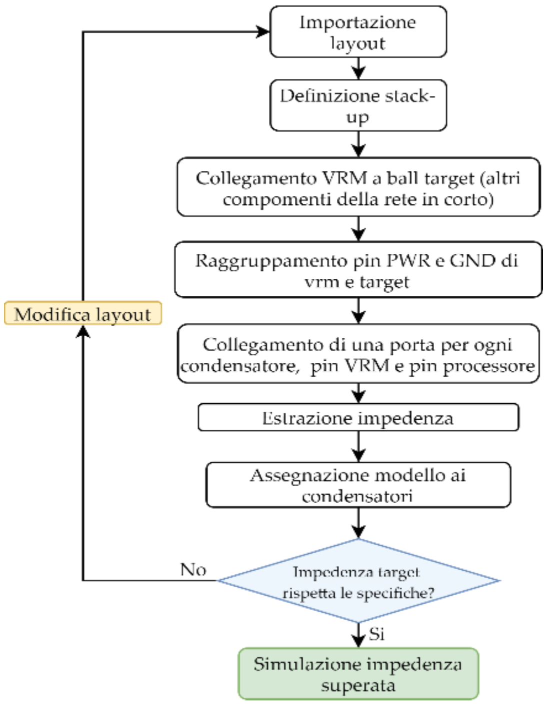
Dal circuito alla board

Simulazione circuitale

Simulazione EM → *Software dedicati*

Realizzazione

Misure board → *Frequency domain (VNA)*; *Time domain (oscilloscopio)*

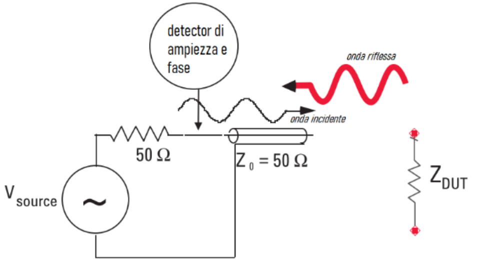


Workflow simulazione EM
Mentor Nimbic

Misure Frequency Domain (VNA)

Misura 1-port:

- $Z_{DUT} \leq 0.1 m\Omega$ → riflessione quasi totale → misura poco accurata

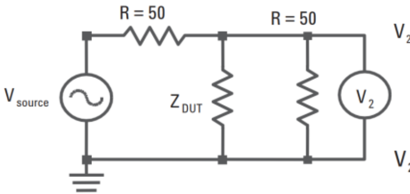


S11 coefficente di riflessione

$$S_{11} = \frac{Z_{DUT} - Z_1}{Z_{DUT} + Z_1} = \frac{Z_{DUT} - 50}{Z_{DUT} + 50}$$

Misura 2-port:

- S_{21} accurata → misura accurata



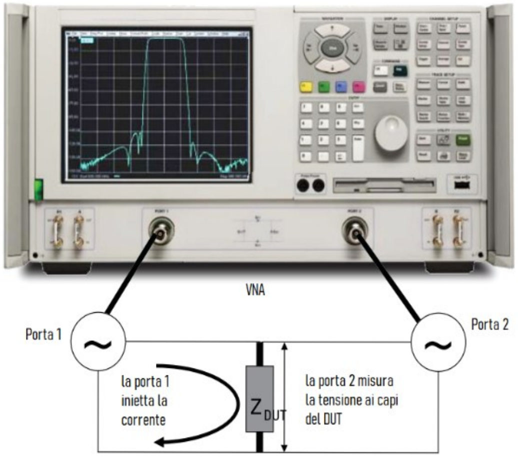
$$V_2 = V_{source} \frac{\frac{50 Z_{DUT}}{50 + Z_{DUT}}}{50 + \frac{50 Z_{DUT}}{50 + Z_{DUT}}}$$

$$V_2 = V_{source} \frac{Z_{DUT}}{50 + 2Z_{DUT}}$$

$V_1 = 1/2\, V_{source}$

$S_{21} = \frac{V_2}{V_1}$

$$Z_{DUT} = 25 \frac{S_{21}}{1 - S_{21}}$$



Misure Time Domain (oscilloscopio)

Necessità per una buona misura:

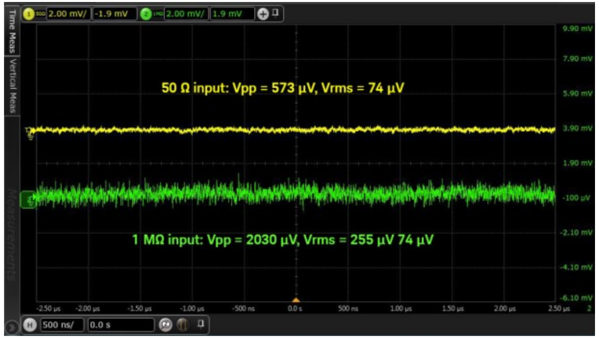
- banda sufficientemente ampia

Null measurement

Bandwidth	Vpp	Vrms
2 GHz	1,040 µV	110 µV
1 GHz	860 µV	90 µV
500 MHz	800 µV	80 µV
20 MHz	460 µV	60 µV

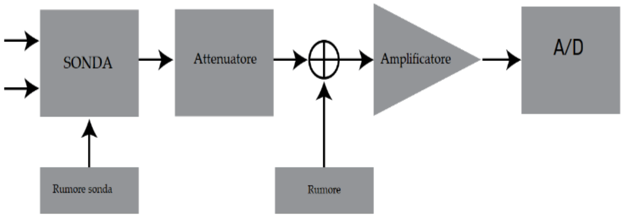
Misure Time Domain (oscilloscopio)

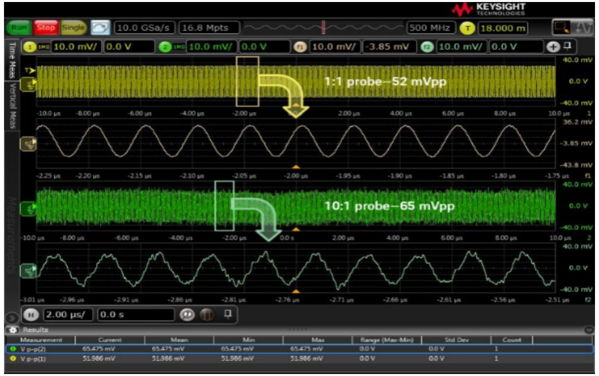
- basso rumore



- evitare attenuazione

  → Preferire sonde 1:1

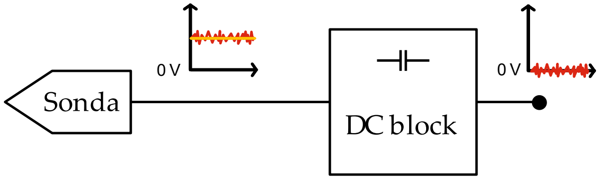


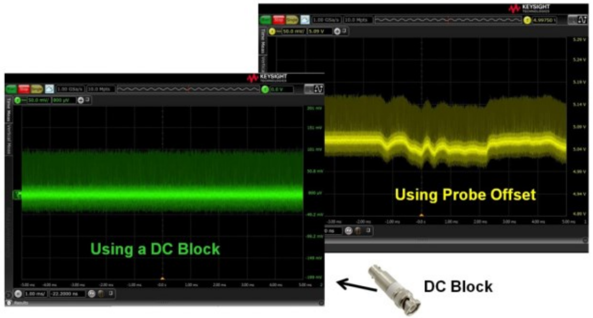


Misure Time Domain (oscilloscopio)

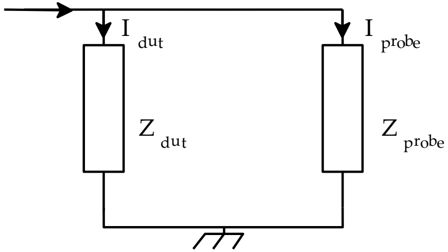
- utilizzo di offset

  → (evitare DC block)

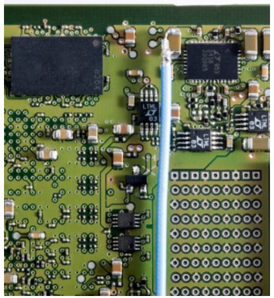




- limitare effetto di carico della sonda



Sonda Coax 50 Ω



Sonda Keysight N7020A

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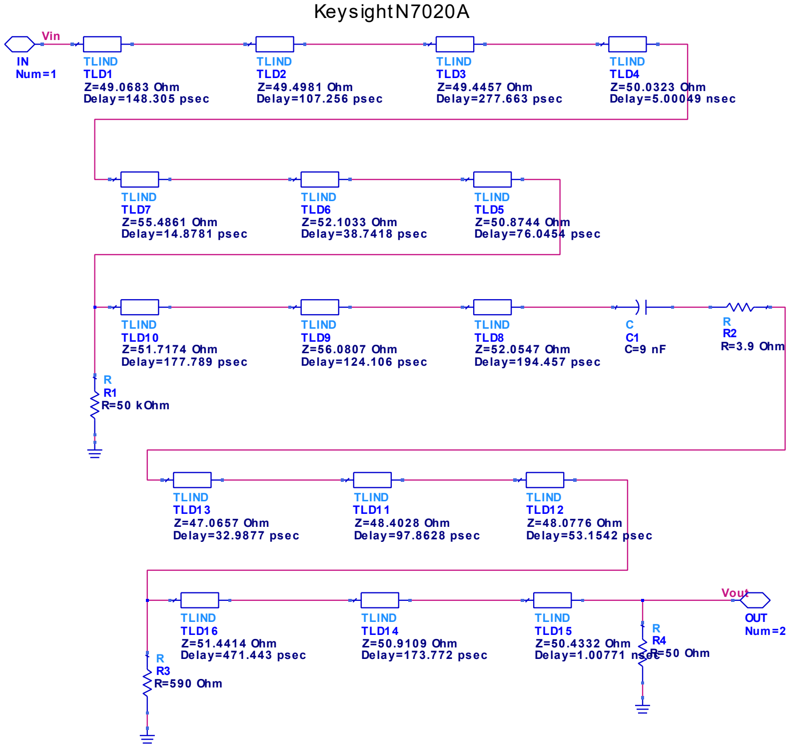
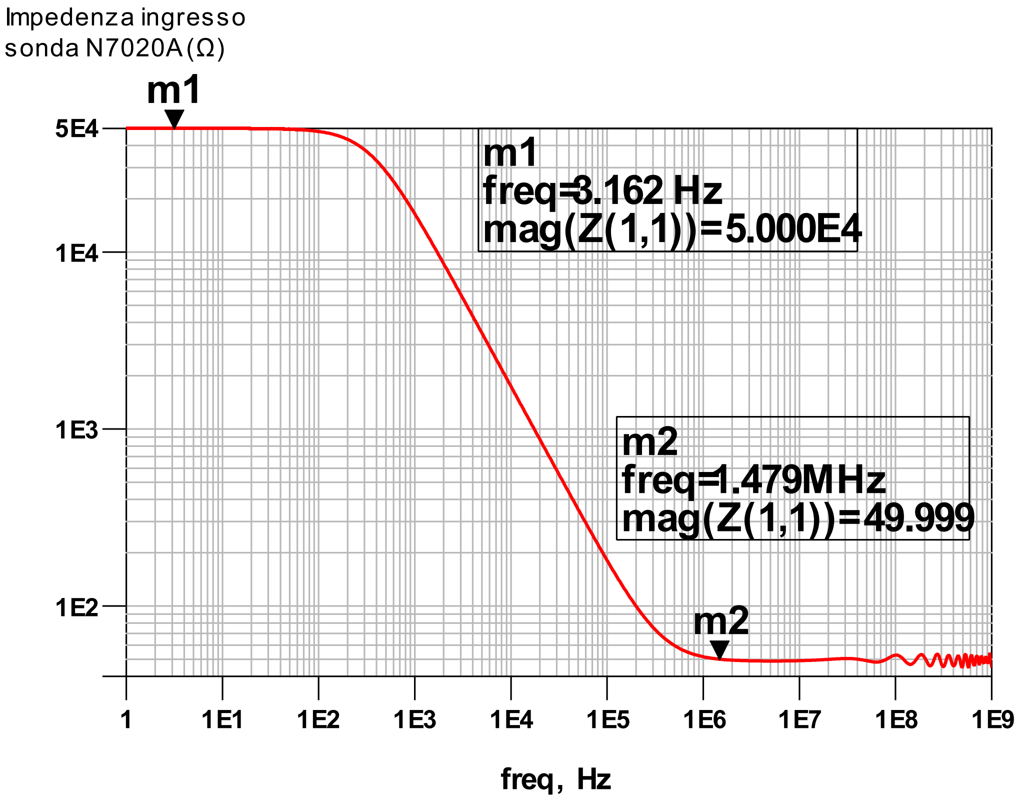


Table 6 N7020A Electrical Characteristics and Specifications

Attribute	Characteristics (based on probe's connection configuration)				
	With N7022A Main Cable	With N7021A Pigtail Cable & N7022A Main Cable	With N7023A Browser	With N7032A Browser & N7022A Main Cable	With N7033A Browser & N7022A Main Cable
Probe Bandwidth (-3 dB)	2 GHz	2 GHz	350 MHz (using the included ground spring)	2 GHz	2 GHz
Maximum Input Voltage (non-destructive)	±30V peak input (mains isolated)				
Attenuation Ratio	1.1:1				
Offset Range	± 24V				
Input Impedance at DC *	50 kΩ ±2%				
Active Signal Range	± 850 mV (about offset voltage)				
Probe Noise (at 2 GHz)	10% increase in the noise of the connected oscilloscope				
Output Termination	50 Ω scope input				
Probe Type	Single Ended				

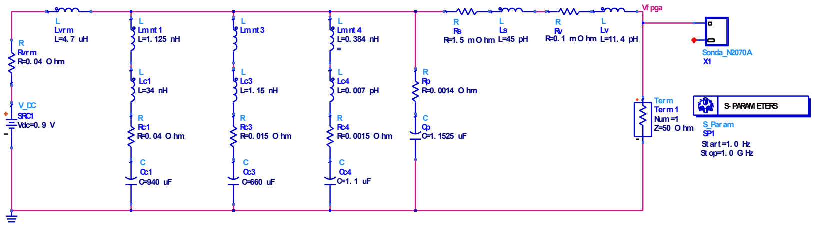
Simulazione N7020A: impedenza

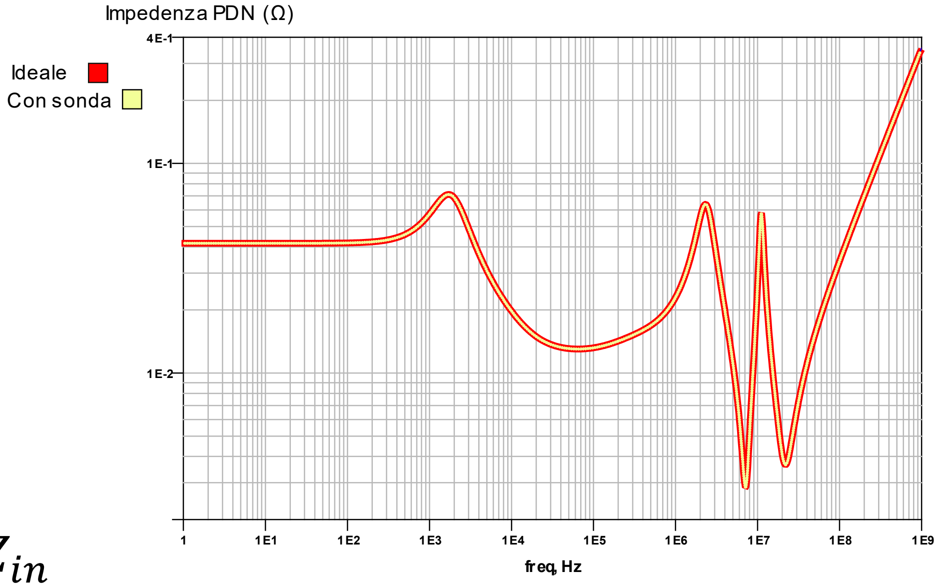


$$Z_{eq} = 50k\Omega \quad f \leq 100\ Hz$$

$$Z_{eq} = 50\Omega \quad f \geq 1\ \text{MHz}$$

Simulazione N7020A: effetto di carico





In questo caso:

$50\Omega \gg Z_{target}$

⬇

La sonda non perturba la misura di Z_{in} neanche ad alta frequenza

Referenze

- S. Lin and N. Chang, "Challenges in power-ground integrity," IEEE/ACM ICCAD 2001, San Jose, CA, USA, 2001, pp. 651-654, doi: 10.1109/ICCAD.2001.968730.
- Alex Manukovsky, Shimon Mordooch, Amiram Jibly, Power Delivery Improvement & Noise Reduction Using Ultra-Thin (8um) PCB Layers: Simulation, Board Measurements & Practice, DesignCon 2020
- Oak-Mitsui Company, Online: http://www.oakmitsui.com/pages/copperFoil/copperFoil.asp
- FaradFlex®. Online: https://www.faradflex.com/standard-dk/
- Intel.com. Online: https://www.intel.com/content/www/us/en/products/programmable/fpga/stratix-iv.html
- Intel.com. Online: https://www.intel.com/content/www/us/en/programmable/solutions/partners/partner-profile/terasic-inc-/board/de4-stratix-iv-development-board.html
- Mentor. Online https://www.mentor.com/

Referenze

- Erwan Petillon, Power Delivery Network Analysis, Application Report, SWPA222A – November 2012
- Keysight, Making Your Best Power Integrity Measurements, Application note
- Keysight. Online: https://www.keysight.com/en/pdx-x202066-pn-DSOS054A/high-definition-oscilloscope-500-mhz-4-analog-channels?cc=US&lc=eng
- Keysight. Online: https://www.keysight.com/en/pd-2471132-pn-N7020A/power-rail-probe
- Keysight. Online: https://www.keysight.com/en/pdx-x202079-pn-MSOS804A/high-definition-oscilloscope-8-ghz-4-analog-plus-16-digital-channels?cc=US&lc=eng