Quiz 1

Implement a device which connects Input X(i) to Output Z(j) where i
and j are input port and output port selects range between 0 to 3.
Other Outputs Z(k)'s where k is not equal to j, are assigned to logic
'0'. Demonstrate that your implementation is correct.
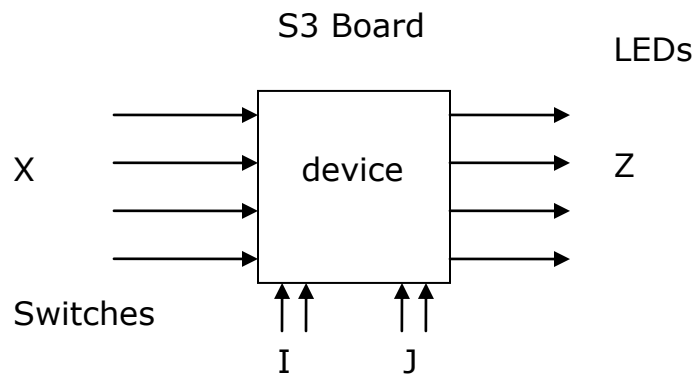
Entity device is
Port (X : in   std_logic_vector(3 downto 0);
             Z : out std_logic_vector(3 downto 0);
          I, J : in   std_logic_vector(1 downto 0));
End device;