Problem

Design a decoder with generic parameter m.

```
entity decg is
generic(m : natural);
port (x : in   std_logic_vector(m-1 downto 0);
       en: in   std_logic;
        z:  out std_logic_vector(2**m - 1 downto 0)
     );
end decg;
```

if en='1' then the output z(j) is a one if the m-bit binary number input x is equal j and z(i) is zero for i not equal to j. If en='0' then the outputs are zero (others => '0').

Implement a 3-to-8 decoder using two 2-to-4 decoders.

```
entity dec328_2x224 is
port (x : in   std_logic_vector(2 downto 0);
      z:  out std_logic_vector(7 downto 0)
     );
end dec3to8x2to4;
```

The dec328_2x224 does not have en input.
Connect the input x(2) to the en ports of the 2-to-4 decoder instance that outputs to z(7 downto 4).
Connect not x(2) to the en ports of the 2-to-4 decoder instance that outputs to z(3 downto 0).
Connect x(1) and x(0) to the input ports of the two instances of the 2-to-4 decoders.

```
-------------------------------------------------
-- Company: Drexel ECE
-- Engineer: Prawat
-- Decoder with generic parameter m.
-- if en='1' then the output z(j) is a one if
-- the m-bit binary number input x is equal j and
-- z(i) is zero for i not equal to j. If en='0'
-- then the outputs are zero (others => '0').
-------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity decg is
generic(m : natural);
port (x : in   std_logic_vector(m-1 downto 0);
       en: in   std_logic;
        z:  out std_logic_vector(2**m - 1 downto 0)
     );
end decg;

architecture Behavioral of decg is
begin

process(x, en)
subtype my_int is integer range 0 to 2**m - 1;
variable j : my_int;
begin

if en = '0' then z <= (others => '0'); else

j := 0;
for i in 0 to m-1 loop
   if x(i) = '1' then j := j + 2**i; end if;
end loop;

for i in 0 to 2**m - 1 loop
  if i=j then z(i) <= '1'; else
  z(i) <= '0';
  end if;
end loop;
end if;
end process;
end Behavioral;

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity dec328_2x224 is
port (x : in   std_logic_vector(2 downto 0);
      z:  out std_logic_vector(7 downto 0)
     );
end dec328_2x224;

architecture struc of dec328_2x224 is
component decg
generic(m : natural);
port (x : in   std_logic_vector(m-1 downto 0);
       en: in   std_logic;
        z:  out std_logic_vector(2**m - 1 downto 0)
     );
end component;
signal w : std_logic;
begin
w <= not x(2);
u1: decg generic map (2) port map
(x => x(1 downto 0), en => x(2), z => z(7 downto 4));
u2: decg generic map (2) port map
(x => x(1 downto 0), en => w, z => z(3 downto 0));
end struc;
```