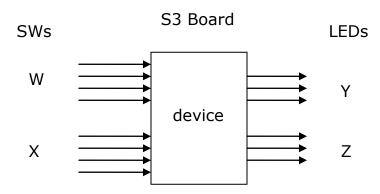**Quiz 1**

Implement a combinational device whose outputs Y and Z are 3-bit vectors representing integers range 0 to 7. The output Y is equal to the number of cases when both inputs W(i) and X(i) for i = 0, …, 3, are a one. And the output Z is the number of cases W(i) and X(i) are both zero.

Entity device is
Port (W, X : in   std_logic_vector(0 to 3);
        Y, Z : out std_logic_vector(2 downto 0));
End device;
Architecture …
-- W(i) = X(i) and W(i) = '1' then count
variable count1, count0 : integer;
begin
count1 := 0; count0 := 0;
for I in 0 to 3 loop
if W(i) = X(i) and W(i) = '1' then count1 := count1 + 1; end if;
end loop;
case count1 is
when 0 => y <= "000";
…
-- the same for counting '0' match.
for I in 0 to 3 loop
if W(i) = X(i) and W(i) = '0' then count0 := count0 + 1; end if;
end loop;