Drexel University
College of Engineering
ECEC 302, Digital System Projects

1. ECEC 302, Digital System Projects, ece.drexel.edu/courses/ECE-C302

2. Credits: 4.00 Contact Hours: Two 80-minute Lectures and one 110-minute Lab

3. Instructor: Prawat Nagvajara, Ph.D. (Associate Professor)

4. Textbook and Materials
Digital Systems Projects Class Notes, Prawat Nagvajara
Textbook: J. Bhasker, *A VHDL Primer,* Englewood Cliffs, NJ: Prentice Hall, 1995
Recommended References:
A.B. Marcovitz, *Introduction to Logic Design, 3rd Edition*, McGraw Hill, 2010
J.F. Wakerly, *Digital Design: Principles and Practice*, Englewood Cliffs, NJ: Prentice Hall, 2000
Mano and Kime, *Logic and Computer Design Fundamentals*, Englewood Cliffs, NJ: Prentice Hall, 1998
S. Yalamanchili, *VHDL Starter's Guide*, Englewood Cliffs, NJ: Prentice Hall, 1998
D.L. Perry, *VHDL* (2nd Ed), New York, NY: McGraw-Hill, 1993.
R.H. Katz, *Contemporary Logic Design*, Redwood City, CA: Benjamin/Cummings, 1992

5. Specific Course Information
   a. Brief description of the course (Course Catalog Description)
      To study the theory of digital system design and the top-down design methodology using hardware description language and software tools for simulation, synthesis and Field Programmable Gate Array (FPGA) implementation.
   b. Pre-requisites or Co-requisites: ECE 200 (Minimum Grade: D)
   c. Required course in Computer Engineering program. Selected elective in Electrical Engineering program

6. Specific Goals for the Course

   a. Course Outcomes:
      1. Understanding of digital hardware systems – synchronous systems, state machines, bus topology and memory structures.
      2. Basic understanding of specification, and verification (debug and testing).
      3. Strong experience of design with Hardware Description Language (HDL), simulation, and synthesis of hardware from HDL on programmable electronics (Field Programmable Gate Array, FPGA).
      4. Understanding of mapping algorithms to hardware using data dependency graph and pipeline parallelism implementation.
      5. Having laboratory experiences.

   b. Students Outcomes
      (a) an ability to apply knowledge of mathematics, science, and engineering
      (b) an ability to design and conduct experiments, as well as to analyze and interpret data
      (e) an ability to identify, formulate, and solve engineering problems
      (k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

c. Drexel Student Learning Priorities (DSLPs)
   Creative and Critical Thinking
   Information Literacy
   Self-directed Learning
   Use of Technology Use
   Professional Practice
   Research, Scholarship And Creative Expression

7. Brief List of Topics to be Covered by Weeks

7.1 Digital Systems Introduction – Theory, Hardware Description Language and Integrated Design Environment
7.2 Registers and Synchronous Circuits
7.3 State Machines
7.4 Combinational and Generic Parameters
7.5 Structural Description and Test Bench
7.6 Mapping algorithms to hardware: Data dependency graph, array structures
7.7 Pipeline Structure
7.8 Design with Intellectual Property Cores
7.9 Storages – Block RAM, Stack and First-In First-Out (FIFO) queues
7.10 Bit-vector arithmetical circuits (signed and unsigned) and binary coded representation.

8. Evaluation

a. Evaluations of the assignments, lab works, quiz, and exams are based on student's demonstration of the design correctness and understanding. Students earn partial credits on incomplete designs by submitting attempted design codes for grading.

b. Design Assignments
   i. Nine Lab meetings 18%
      Pre-lab and in-lab works (2% per meeting) are graded before the end of each lab meeting. Students can earn partial credits
   ii. Five Homework Assignments 7%
      Late homework 50% reduction and no credit after one week

c. Exams
   i. Quiz 10% is during the week 5 lab meeting
   ii. Midterm 25% is during the week 6 lab meeting
   iii. In-lab Final 40% during the examination week

d. Grades assignment

A	:	scores $\geq$ 93%
A-	:	93% > scores $\geq$ 88%
B+	:	88% > scores $\geq$ 83%
B	:	83% > scores $\geq$ 78%
B-	:	78% > scores $\geq$ 73%
C+	:	73% > scores $\geq$ 68%
C	:	78% > scores $\geq$ 63%
C-	:	63% > scores $\geq$ 58%
D+	:	58% > scores $\geq$ 53%
D	:	53% > scores $\geq$ 48%
F	:	scores $\leq$ 48%

9. Academic Policies
    a. Academic Integrity, Plagiarism and Cheating Policy: Refer to "Student Conduct and Community Standards" www.drexel.edu/studentaffairs/community_standards/studentHandbook/
    b. Students with Disabilities: Refer to http://drexel.edu/oed/disabilityResources/faculty/SyllabusStatement/
    c. Course Drop Policy: Refer to http://www.drexel.edu/provost/policies/course_drop.asp
    d. Course Change Policy: The instructor has the right to make changes to the course contents and the pedagogy. The changes will be announced prior to the action and the reasons will be communicated to students.