Introduction to Transistor-Level Logic Circuits[1]

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At the transistor level of logic circuits, transistors operate as switches with the logic variables controlling the open or closed state of the switches. Figure 1 shows a transistor-level diagram of an inverter (Fig. 1-a) and a 2-input NOR-gate (Fig. 1-b). The parallel and series structures for the n-type transistor(s) (the structure connecting the output to ground – 0 volt for Logic 0) and the p-type transistor(s) (the structure connecting the output to V_{DD} – V_{DD} volts for Logic 1), respectively, result in the NOR function of the control variables at the output of the gate.

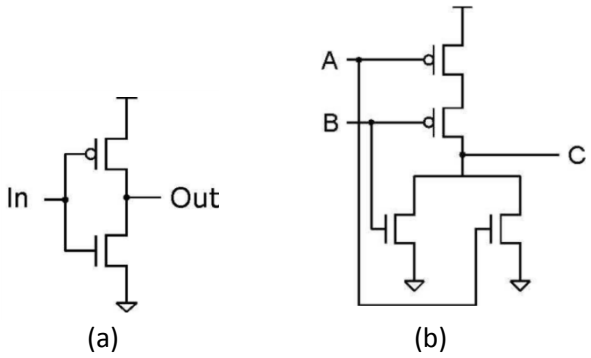


Fig. 1 CMOS Transistor Circuits (a) Inverter Out = NOT In, (b) NOR-gate C = NOT (A or B)

The transistors are the Field Effect Transistors (FET). The terminals of the transistor are source, gate and drain terminals. The logic variables are the input voltages at the gate-terminals controlling the switch state. Figure 2 shows a cross section of the transistors diagram of the p-type (left) and n-type (right) transistor. The terminals of the transistors can be connected (wired) by a layer of conductors (metal). The input and output wires are not shown.

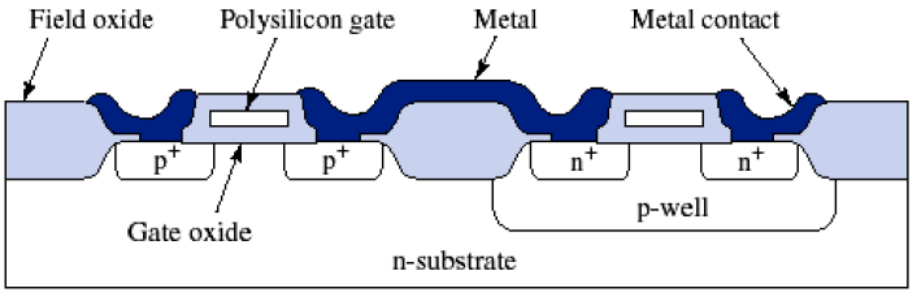


Fig. 2 CMOS inverter layout Cross Section

[1] Figures were taken from presentations with their sources cited in the references. Only for student use.

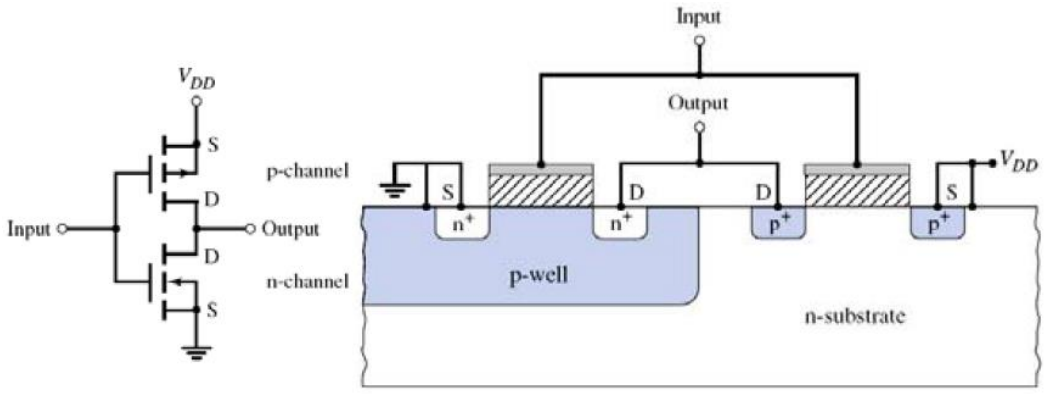


Fig.3 CMOS Inverter Circuit and Layout Cross Section Diagram

Figure 3 shows the terminal S of the p-type is connected to V_{DD} which is the voltage for Logic 1. The S terminal of the n-type transistor is connected to ground. The D and D of n-type and p-type are connected and an output is wired at the connection. The input is wired to both G terminals. The diagrams include terminals for the substrate (Bulk) voltages for the operation of the transistors. They do not represent the logic variables.

Steady-state Circuit model

In the p-type transistor, when the gate voltage is 0V a conducting channel is formed between D and S (field-effect transistor), that is, the p-type switch is closed (Fig. 4). With the n-type transistor, when the gate voltage is V_{DD} the n-type switch is closed (Fig. 5). The p-type and n-type are complementary with respect to the control logic variables.

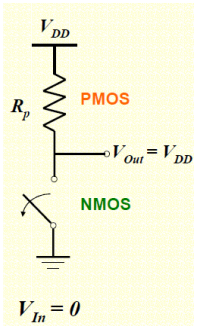


Fig. 4 CMOS Inverter Steady-state Circuit ($V_{SGp} = V_{DD}$, $V_{GSn} = 0$)

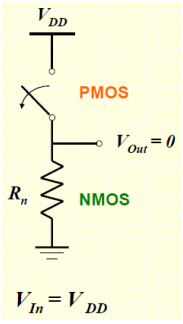


Fig. 5 CMOS Inverter Steady-state Circuit ($V_{SGp} = 0$, $V_{GSn} = V_{DD}$)

Figure 4 and Figure 5 show the CMOS inverter steady-state output voltage V_{out} due input voltage $V_{in} = V_{GSn}$, for the n-type and $V_{in} = V_{SGp} + V_{DD}$, for the p-type. V_{GSn} and V_{SGp} denote the n-type and p-type gate voltages.

For the NOR-gate (Fig. 1), the p-type (top structure) the output C = not A and not B, i.e., when both A and B are logic zero the output is a logic one – a series structure. For the n-type (bottom structure), not C = A or B, i.e., the output is a logic zero when either A or B or both is a logic one – a parallel structure. The p-type (top structure) and the n-type (bottom structure) are complementary.

Switching Electrical Characteristic:

This technology is called CMOS. The name "MOS" transistor, metal oxide silicon, came from the first version of the transistor where metal was used for the gate terminal over silicon dioxide and substrate. Shortly after the early design, polysilicon was used replacing metal.

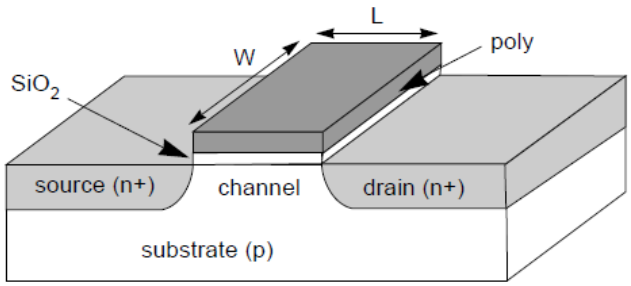


Fig. 6 n-type MOSFET

Figure 6 shows the geometry of the gate terminal at which the control logic voltage is applied in charging or discharging the parallel plates of the gate terminal. The channel length L is fixed for a given technology and W varies for different sizes for transistors in the circuit.

Box. 1 nMOS I_{ds} v.V_{ds} Equations

Non-Sat:

$$I_{ds} = \beta_n\left[(V_{gs} - V_{tn})V_{ds} - \frac{1}{2}V_{ds}^2\right]$$

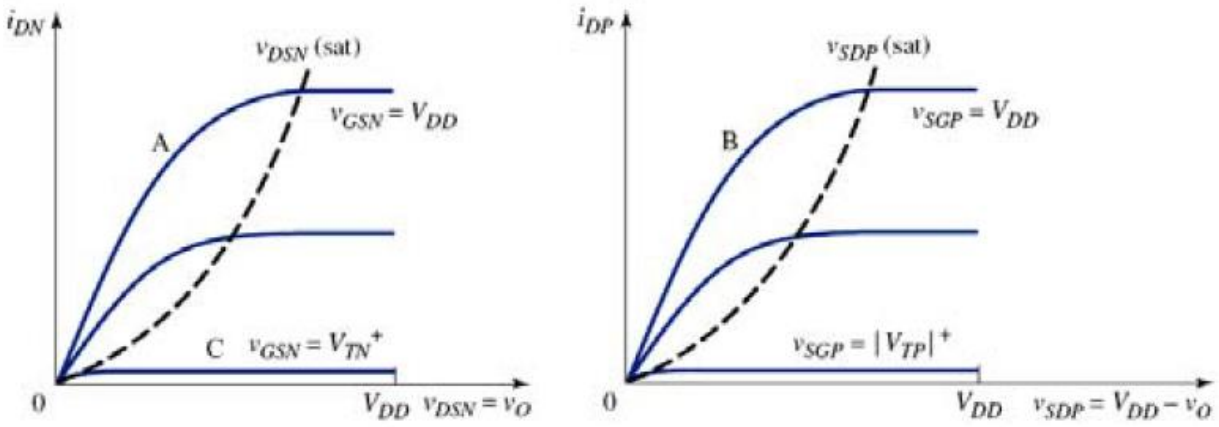
Saturation:

$$I_{ds} = \frac{\beta_n}{2}(V_{gs} - V_{tn})^2$$

where

$$\beta_n = \mu\frac{\varepsilon}{t_{ox}}\left(\frac{W}{L}\right)_n$$

Box 1 shows the equations for I_{DS} as a function of V_{DS} for nMOS which consists of two operating regions - non-saturated and saturated. The transistor is in non-saturation when $V_{GS} - V_{tn} \geq V_{DS} \geq 0$ and in saturation when $V_{DS} \geq V_{GS} - V_{tn} \geq 0$, where V_{tn} is the NMOS threshold voltage. The saturation voltage is when $V_{DSn} = V_{sat} = V_{GS} - V_{tn}$. The parameter β_n is a function of the width-length ratio $(W/L)_n$ and the process parameters – the electron mobility μ, the oxide permittivity ε and the oxide thickness t_{ox}.



(a) nMOS I_{Dn} v V_{DSn} (b) pMOS I_{Dp} v V_{SDp}

Fig. 7 Drain Current v Drain Voltage Characteristics for CMOS Invertor Analysis

Figure 7 shows nMOS I_{Dn} v.V_{DSn} plot and pMOS I_{Dp} v V_{SDp} plot for an analysis of the steady-state characteristic of the CMOS invertor. These characteristic consists of multiple plots correspond to different gate voltages. When the gate voltage is less than the threshold voltage the devices are in the cut-off mode. These are modeled by an open switch in Fig. 4 and Fig. 5.

In Fig. 4, the nMOS is in cut-off. For the pMOS the drain current I_{Dp} is zero but the gate voltage, V_{SGp} = V_{DD}, whose characteristic is the curve B in Fig. 8. The pMOS is in non-saturation region in the vicinity of the origin where V_{SDp} is also zero, hence, $V_O = V_{DD} - V_{SDp} = V_{DD}$. This characteristic of the CMOS technology gives its very-low (no) static power dissipation advantage. Similarly in Fig. 5 the pMOS is in non-saturate with $V_{DSn} = 0$ and $I_{Dn} = 0$, $V_O = V_{DD} - V_{DSn}$.

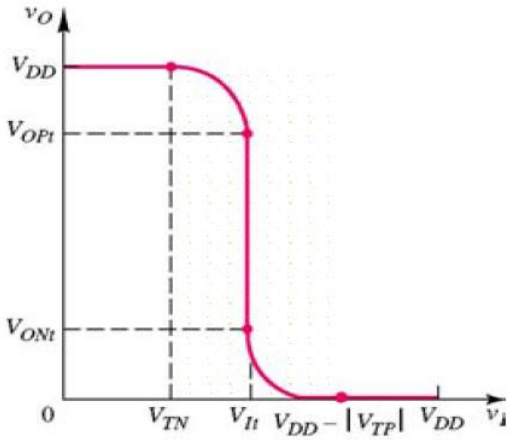


Fig. 8 CMOS Switching Inverter Characteristic: Input Voltage v Output Voltage

The switching characteristic of the CMOS inverter in terms of V_O v V_i (Fig. 8) consists of the transitions of the nMOS operating regions from the cut-off region, saturated region, saturated region, non-saturated region and non-saturated region as the invertor input voltage (nMOs gate voltage) varies from 0 to VDD. Table 1 summarizes pMOS and nMOS transitions of operating regions as the intervals of the input voltage V_i, where V_{TN} and V_{TP} denote the threshold voltage for the pMOS and nMOS, respectively. Recall also that $V_i = V_{GSn}$, and $V_i = V_{SGp} + V_{DD}$. When $V_i = V_{It}$, the critical voltage, both transistors are in the

saturated region a short circuit occurs between V_{DD} and ground). With the nMOS and pMOS transistor widths, $W_n = W_p$, $V_{lt} = V_{DD}/2$.

Table1. Operating Regions of CMOS Transistors

V_i	pMOS	nMOS
$0 \le V_i \le V_{TN}$	Non-saturated	Cut-off
$V_{TN} \le V_i \le V_{lt}$	Non-saturated	Saturated
V_{lt}	Saturated	Saturated
$V_{lt} \le V_i \le V_{DD}-\|V_{TP}\|$	Saturated	Non-saturated
$V_{DD}-\|V_{TP}\| \le V_i$	Cut-off	Non-saturated

Switching Delay and Frequency:

Important parameters associating with the performance of logic circuits are the rise-time and the fall-time of circuit output voltages (logic values) due to input changes. These time durations determine the clock frequency or the clock period of a synchronous digital system, that is, the maximal delay in the switching logic circuit for the output voltages to reach steady state values dictates how fast these values can be updated into registers.

Rise time of the RC circuit is defined as the duration for a response voltage across the capacitor,

$$v(t) = 1 - e^{-(1/\tau)t},$$

where $\tau = RC$ is the time constant, to reach 0.9 V (90%) from 0.1 V (10%). Figure 9 shows the capacitor voltage v time. The rise time is approximately $(2.302 - 0.105)\tau = 2.197\tau \approx 2.2\tau$.

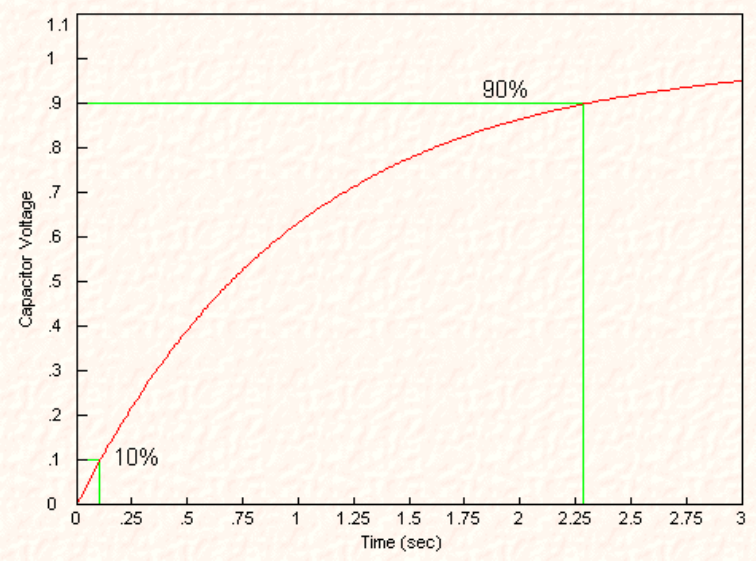


Fig. 9 Rise Time for RC Circuit – Definition

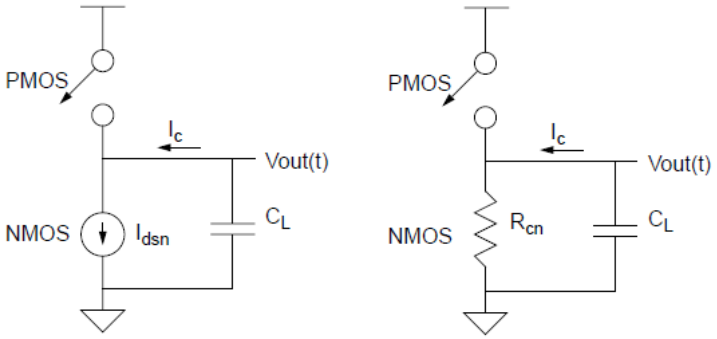


Fig. 10 Fall-time Analysis Circuit Models (a) nMOS: Saturated (b) nMOS: Non-Saturated

The CMOS inverter analysis of the fall time involves the circuit models (Fig. 10) where the nMOS operates in the saturated region $V_{out} \geq V_{DD} - V_{Tn}$ and then the non-saturated region $0 < V_{out} \leq V_{DD} - V_{Tn}$ as the output voltage $V_{out} = V_{DSn}$ transitions (see Fig. 7(a)). Initially, the pMOS is in the saturated region with $I_{DSp} = 0$, and the nMOS is in the cut-off where the input $V_{in} = V_{GSn} = 0$ and $V_{out} = V_{DD}$. When the input changes from 0 to V_{DD}, the pMOS moves to the cut-off state $I_{DSp} = 0$, and the nMOS moves to the saturated region $V_{GS} = V_{DD}$ and a constant I_{DSn} equals to the capacitor current I_C (Fig. 10(a)). When the voltage across C_L, $V_{out} = V_{DS}$ drops below $V_{DD} - V_{Tn}$ the nMOS is the non-saturated region until V_{out} reaches the steady-state value of 0 volt and I_{DSn} reaches 0 Amp.

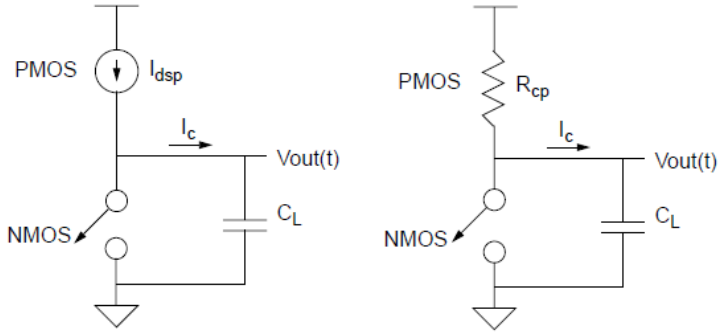
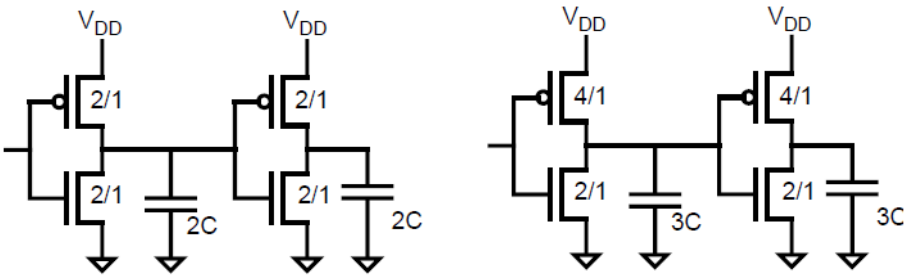


Fig. 11 Rise-time Analysis Circuit Models (a) pMOS: Saturation (b) pMOS: Non-Saturation

Similarly, the CMOS inverter analysis for the rise time is based on the circuit model shown in Fig. 11, where Fig. 11(a) the nMOS is in the cut-off region and the pMOS transitions from the saturated region $V_{out} \leq V_{Tp}$ (Fig. 11(a)) to the non-saturated region $V_{Tp} < V_{out} \leq V_{DD}$ (Fig. 11(b)) as the output voltage $V_{out} = V_{DD} - V_{SDp}$ transitions to steady-state, i.e., $V_{SDp} = 0$ and $I_{SDp} = 0$ (see Fig. 7(b)).

The results from the above analyses are that the rise time $t_r = [k/\beta_p V_{DD}]C_L$ and the fall time $t_f = [k/\beta_n V_{DD}]C_L$.

The RC circuit models are used, omitting the saturated and non-saturated region models, for analyzing the rise time and fall time. In this RC-circuit model $t_r = R_p C_L$ and $t_f = R_n C_L$, (the time constants are approximately the rise time and fall time with the 2.2 factor included). The resistors $R_p = k/\beta_p V_{DD}$ and $R_n = k/\beta_n V_{DD}$ are functions of the constant k and β_p (or β_n) and V_{DD}. In Box 1, beta varies with the ratio W/L and the mobility μ. Since the mobility $\mu_n = 2\mu_p$, for equal rise time and fall time, $t_r = t_f$, $\beta_p = \beta_n$, which means that $(W/L)_p = 2(W/L)_n$. In other words, for a fixed channel length L, an equal rise-time and fall-time means the pMOS width is twice the nMOS width (pMOS is twice larger than nMOS).



(a) Non-equal Rise/Fall Times (b) Equal Rise/Fall Times

Fig. 12 Series Inverters Rise-time and Fall-time RC Circuit Model Analysis

Figure12 shows two inverters in series. The W/L sizing parameters and the equivalent load capacitors are indicated. The rise time is the time from when the input changes from 0V to V_{DD} to the time the output of the circuit reaches 0.9 V_{DD}. Similarly, the fall time is calculated as the time from when the input changes from V_{DD} to 0Vto the time the output of the circuit reaches 0.1V.

For the circuit (a) with the load capacitor at the output equals 2C, the rise time t_r = (2R)(2C) + R(2C) = 6RC, the first inverter fall time plus the second inverter rise time, where R_n = 2R, R_p = R, C_n = C and C_p = C. With the ration $(W/L)_p = (W/L)_n$ = 2/1 which means that $2\beta_p = \beta_n$ and $R_n = 2R_p$.

The fall time for the circuit (a) is t_f = R(2C) + (2R)(2C) = 6RC.

Similarly for the circuit (b) with the load capacitor at the output equals 3C, the rise time t_r = R(3C) + R(3C) = 6RC, the first inverter fall time plus the second inverter rise time, where R_n = R, R_p = R, C_n = C and C_p = 2C when $(W/L)_p$ = 2/1 and $(W/L)_n$ = 4/1. The fall time is t_f = R(3C) + R(3C) = 6RC.

Power Dissipation:
Power dissipation in the CMOS inverter comprises the dynamic capacitive power, the power dissipated during the short circuit condition (see Fig. 8) and the static dissipation due to the leakage current. The dominant dissipation is the capacitive power equals to $C_L V_{DD}^2 f$, where f is the clock frequency determined by the switching delay.

References

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