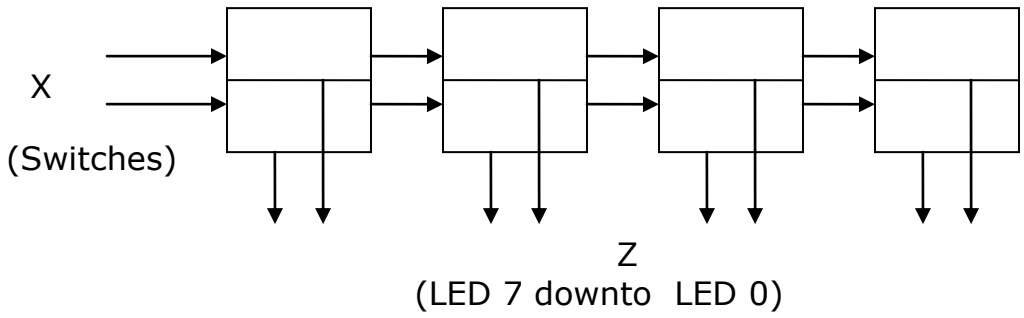
Electrical and Computer Engineering
ECE-C302

Quiz 2

Implement a 4-stage 2-bit wide shift register whose contents are the output port Z connected to the LEDs. The input X (2-bit vector) is the input to the leftmost stage of the register. The four 2-bit vectors are shifted to the right when the register is single stepped (using two-button debounce), x becomes the new content of the left most stage and the left neighbor's content becomes the new content of the other stages.

4-stage 2-bit wide shift register




```
Entity sh_reg_2 is
Port (  x : in    std_logic_vector(0 to 1);
          Z: out std_logic_vector(0 to 7);
         Ck: in    std_logic;
        Btn: in    std_logic_vector(0 to 1));
End sh_reg_2;
```

Solution

```
Architecture beh of sh_reg_2 is
Type vector_array is array (natural range <>) of std_logic_vector(0 to 1);
Signal temp: vector_array(0 to 3);
Signal en : std_logic;
type debounce_state is (rdy, pulse, not_rdy);
signal d_n_s : debounce_state;
```

```
Begin

-- wiring
g1: For i in 0 to 3 generate
Z (2*I to 2*I + 1) <= temp(i);
End generate g1;

-- four-stage two-bit wide register
Process(en)
--signal en: std_logic;
Begin
If en'event and en='1' then
Temp <= x & temp(0 to 2);
End if;
End process;

-- single-step process
process(ck)
begin
if ck'event and ck='1' then
        case d_n_s is
                when rdy =>
                        en <= '0';
                        if btn(0)='1' then
                                d_n_s <= pulse;
                        end if;
                when pulse =>
                        en <= '1';
                        d_n_s <= not_rdy;
                when not_rdy =>
                        en <='0';
                        if btn(1)='1' then
                                d_n_s <= rdy;
                        end if;
        end case;
end if;
end process;

End beh;
```