Electrical and Computer Engineering

Homework 1

Problem 1 Unsigned Multiplier with Input and Output Registers

1.1 Design an n-bit unsigned multiplier with two input-registers storing the operands and an output register storing the result. The design is similar to the example in the Introduction to Digital Systems note.

1.2 Implement and verify on FPGA for 3-bit operands. Explain how pipeline of the input and output registers have the effects on the results.

Problem 2 Sequence Detector

Implement a sequence detector to detect a string “1101” on the FPGA board using the switches for setting the input bit and reset, and the push buttons for single stepping. The output is connected to one of the LEDs.

```
entity seq_det is
port( x, b1, b2,reset,ck: in std_logic;
      z: out std_logic);
end seq_det;

architecture beh of seq_det is
type my_state is (s0, s1, s2, s3, s4);
signal n_s : my_state;
-- signal for single stepping
signal en: std_logic;
-- sequence detector
process(en)
begin
if en’event and en = ‘1’ then
  if reset = ‘1’ then n_s <= s0; else
    case n_s is
      when s0 => ...
```