Electrical and Computer Engineering
ECE-C302

Problem: Implement and show the correctness a combinational 8-bit two's complement circuit declared as

```
Entity twosC is
Port (  x : in    std_logic_vector(7 downto 0);
        Z: out  std_logic_vector(7 downto 0));
End twosC;
```

where Z is the two's complement of x using for generate construct to code an array of the PE component given below (Fiq. 1 below)

```
entity PE is
port(xi, ci: in std_logic;
      xo, co: out std_logic);
end PE;
architecture struc of PE is
signal temp : std_logic;
begin
  temp <= not xi
  xo <= temp xor ci;
  co <= temp and ci;
end struc;
```

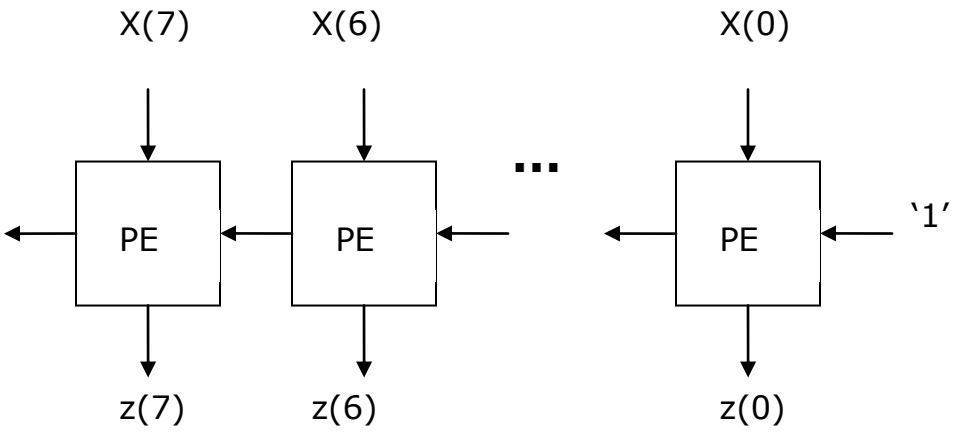

Fig. 1 Two's Complement Circuit Array Structure

```
Architecture struc of twosc is
component PE
port(xi, ci: in std_logic;
      xo, co: out std_logic);
end component;
signal c: std_logic_vector(7 downto 0);
begin
c(0) <= '1';
G1: for I in 0 to 7 generate
G2: if i<7 generate
Cell: pe port map(x(i), c(i), z(i), c(i+1));
End generate G2;
G3: if i=7 generate
Cell: pe port map(x(i), c(i), z(i), open);
End generate G3;
End generate G1;
End struc;
```