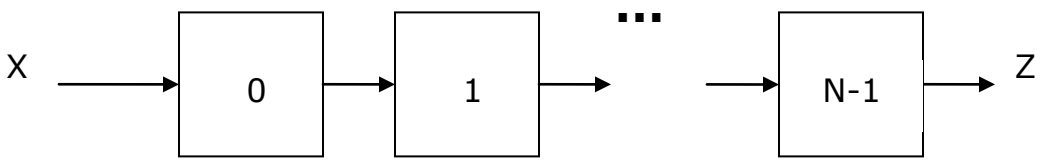
Electrical and Computer Engineering
ECE-C302

Quiz 3: An N-stage shift register bank is an interconnected array of N registers as shown below.

N-stage W-bit shift register bank



The entity is given as

```
Entity sh_reg_bank is
Generic (N: natural := 8;
          W: natural := 2);
Port (  x : in    std_logic_vector(W-1 downto 0);
          Z: out  std_logic_vector(W-1 downto 0);
    Ck, en: in    std_logic);
End sh_reg_bank;
```

where the input en is shift (load) enable for the registers.

Part A : Design and simulate a W-bit register with load enable

```
Entity regW is
Generic(W: natural := 4);
Port (  x : in    std_logic_vector(W-1 downto 0);
          Z: out  std_logic_vector(W-1 downto 0);
    Ck, en: in    std_logic);
End regW;

Architecture beh of regw is
Signal temp: std_logic_vector(w-1 downto 0);
Begin
Z <= temp; -- wiring
Process(ck)
```

```
Being
If ck='1' and ck'event then
If en = '1' then
   Temp <= x;
Else null;
End if;
End if;
End process;
```

Part B: Design and simulate an N-stage shift register bank by using for generate construct to wire W-bit registers in an array.

```
Entity sh_reg_bank is
Generic (N: natural := 8;
          W: natural := 2);
Port (  x : in    std_logic_vector(W-1 downto 0);
          Z: out  std_logic_vector(W-1 downto 0);
   Ck, en: in    std_logic);
End sh_reg_bank;

Architecture struc of sh_reg_bank is
component regW
Generic(W: natural := 4);
Port (  x : in    std_logic_vector(W-1 downto 0);
          Z: out  std_logic_vector(W-1 downto 0);
   Ck, en: in    std_logic);
End component;
Type w_wire is array (natural range <>) of std_logic_vector(W-1
downto 0);
Signal wire : w_wire(0 to N-1);
Begin
-- structural description
Wire(0) <= x;
G1: for I in 0 to N-1 generate
G2: if i<N-1 generate
Cell: regW generic map(W) port map(wire(i),wire(i+1),ck,en);
End generate G2;
G3: if i=N-1 generate
Cell: regW generic map(W) port map(wire(i),z,ck,en);
End generate G3;
End generate G1;
End struc;
```