

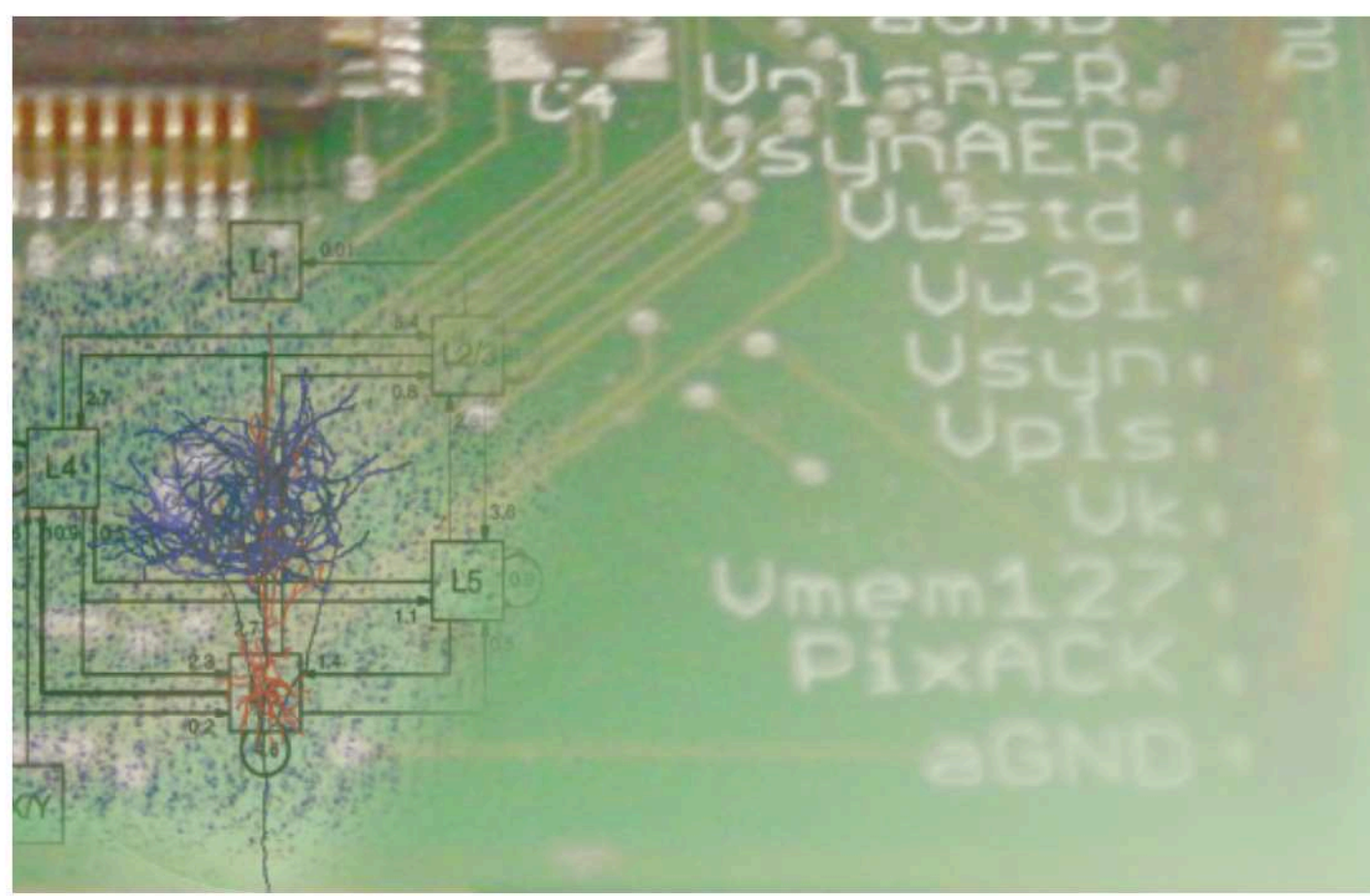
Spike-based synaptic plasticity for on-chip, online learning in real-time

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Neuromorphic Cognitive Systems



Introduction

The remarkable ability of biological systems to adapt to new, unknown environmental conditions, learn from their experience, and extract relevant information from the world, is yet unparalleled by artificial systems. Software simulations are demanding in terms of computing power and are not suited for robotic applications. Analog neuromorphic hardware is compact and low-power but it is unprecise and inhomogeneous. Here we investigated the properties of neuromorphic hardware related to the intrinsic variability of its components. Inspired by theoretical analysis, methods of computer science and biological evidences, we developed a network that exploits the intrinsic variability of the hardware implementation to improve classification performance.

Classification of real-world stimuli

A linear classifier (e.g. a perceptron) is a key element for memory formation in neural networks. We applied our approach to solve the task of classifying hand-written characters from the MNIST database [1].

- Input stimuli are projected into a *high-dimensional space* using a large population of neurons and random connections [2].
- Classes become *linearly separable*.
- The classifier comprises a single neuron receiving inputs through plastic synapses with *stochastic STDP*.

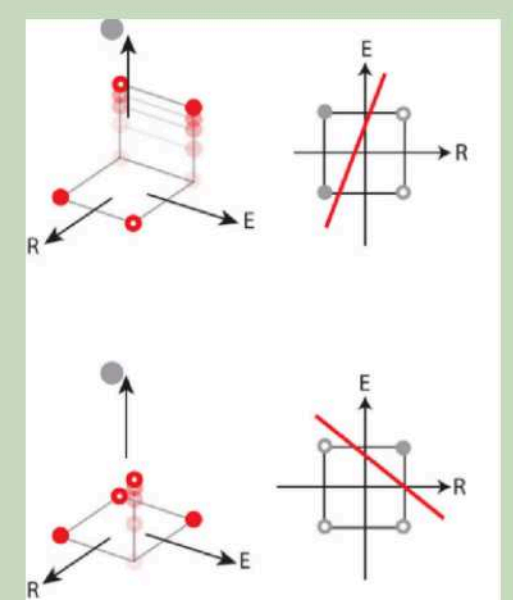


Fig.1 With randomly connected neurons it is possible to solve the non-linear separability of the input classes. The XOR case is shown as an explanatory example.

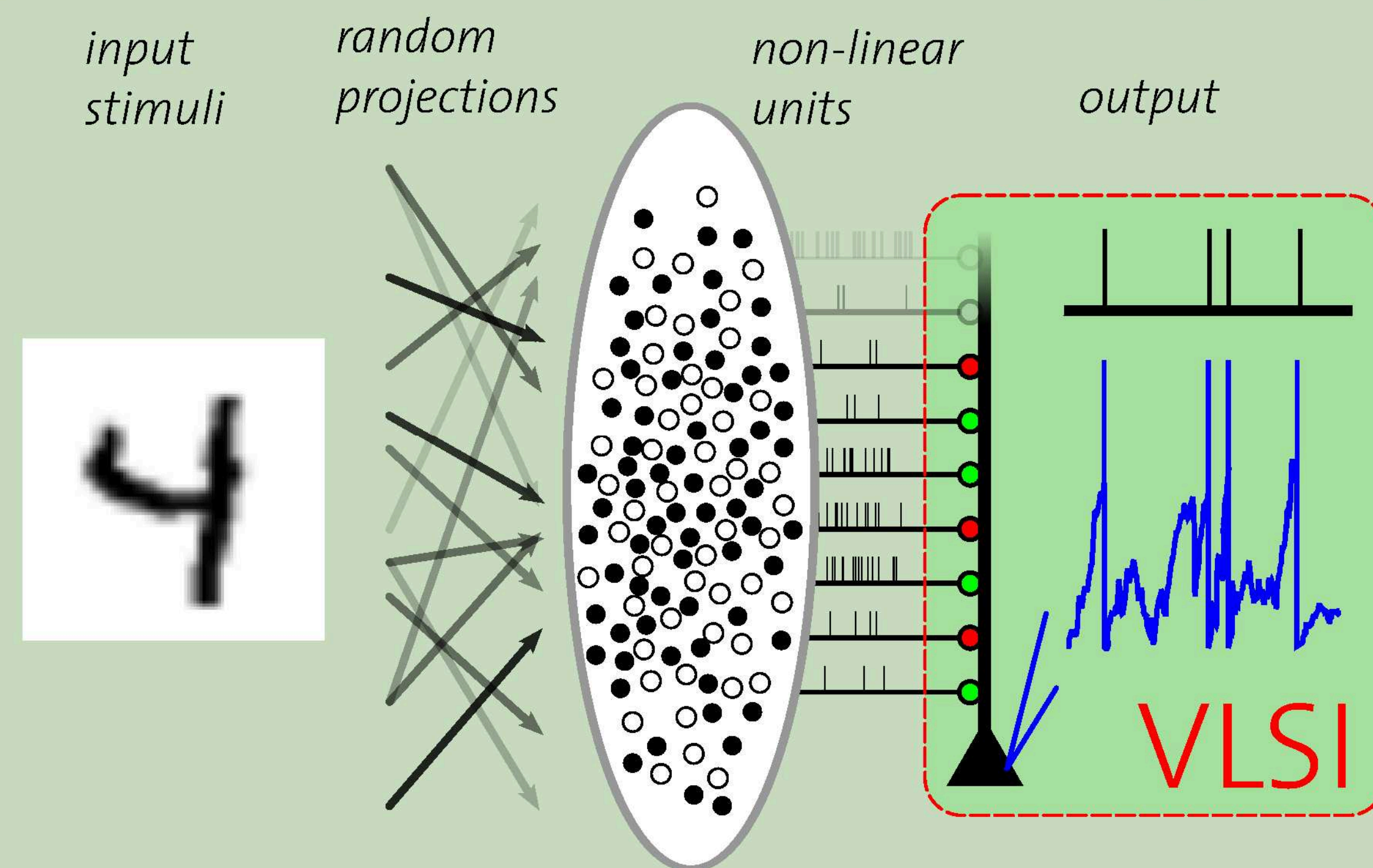


Fig.2 Scheme of the neural network for pre-processing and classification on VLSI.

Neuromorphic hardware setups

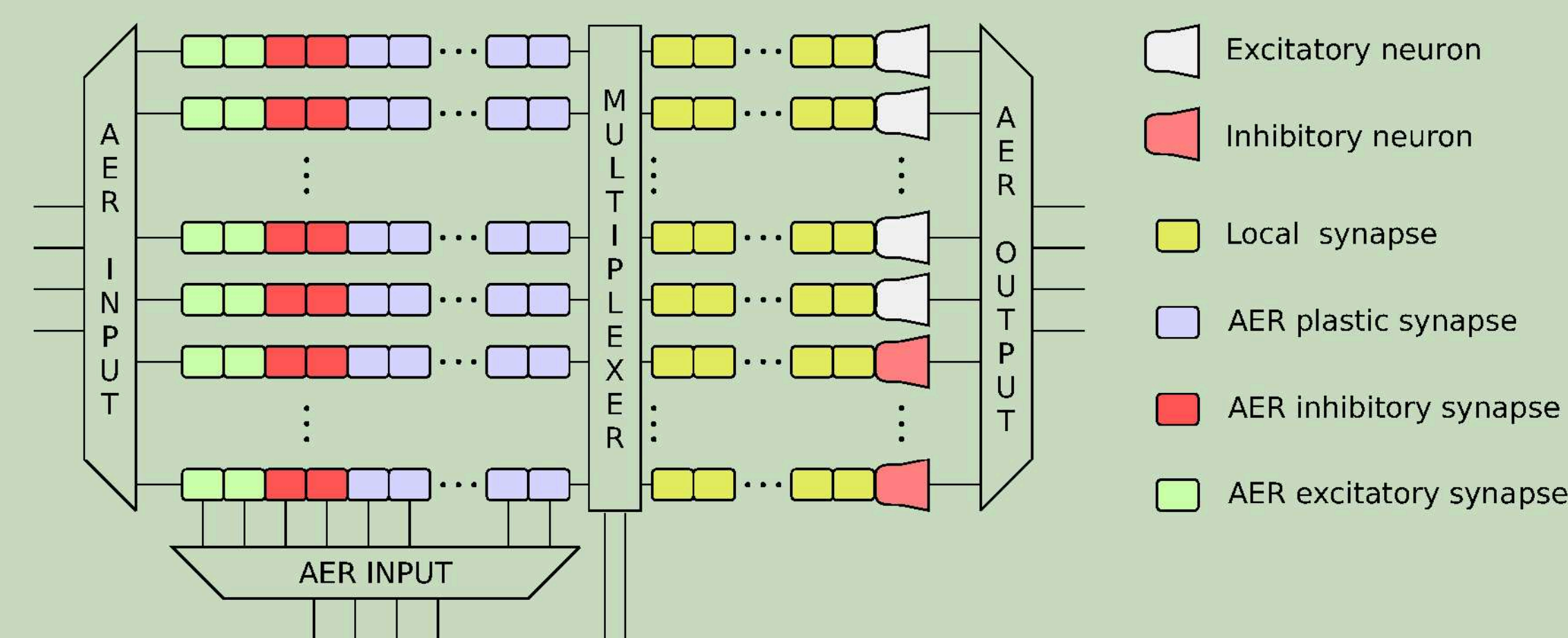
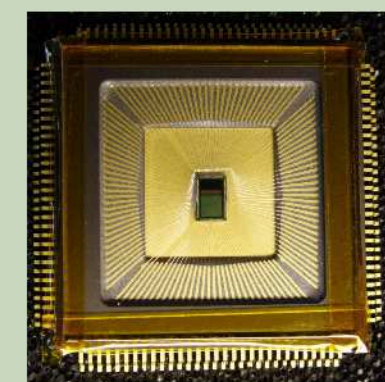


Fig.3 Block diagram of the neuromorphic chip with plastic synapses (CMOS, 0.35µm technology, ~10mm²)

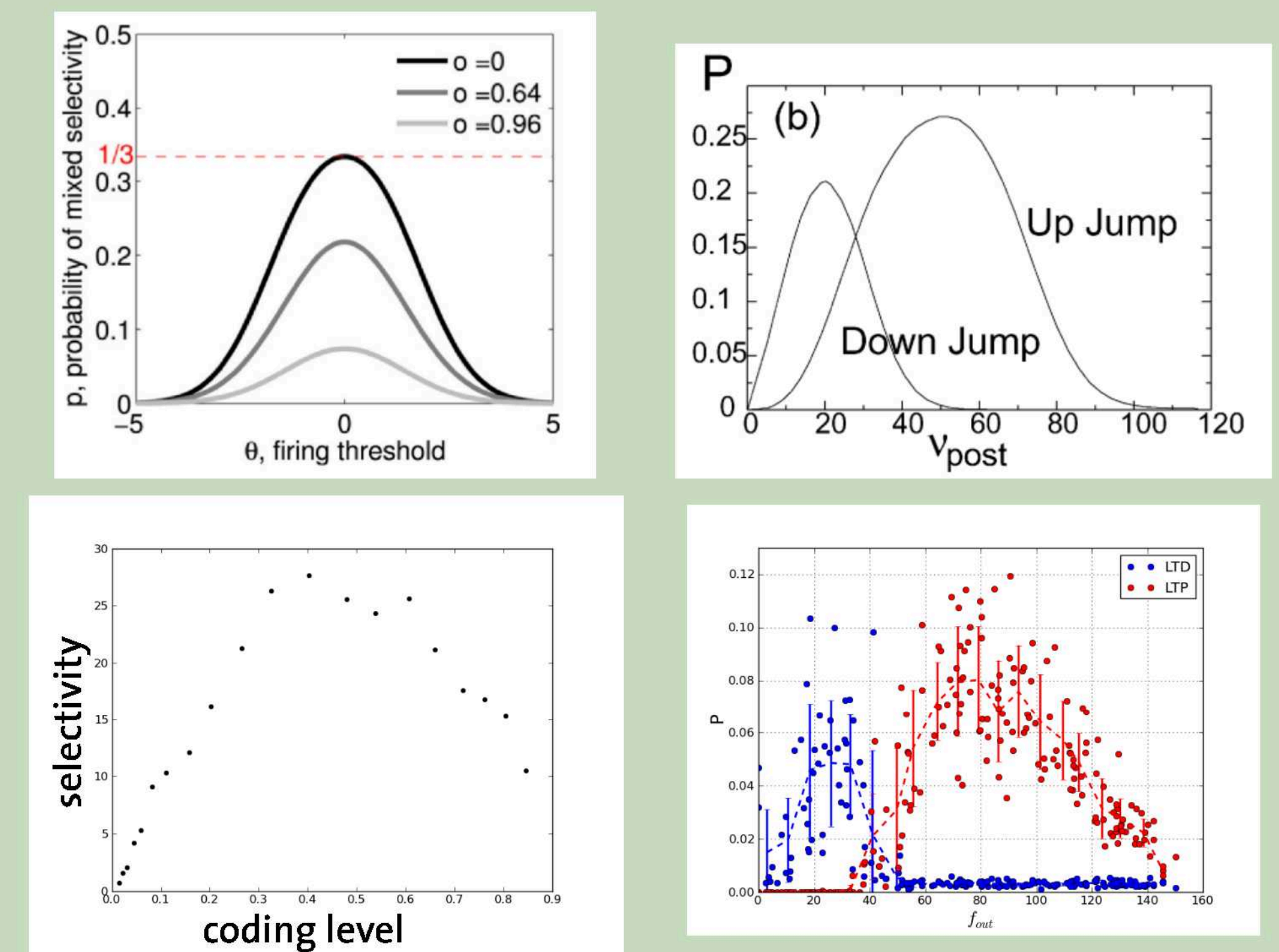


- Compact, low-power, real-time, bio-inspired computation [3]
- Hybrid analog-digital implementation using standard VLSI, CMOS technology
- Circuits for synapses with STDP and Leaky Integrate-and-Fire neuron models

Classification with imprecise hardware

We use neuromorphic hardware in VLSI technology to emulate spiking neural networks in real-time. We carried-out simulations to assess the effects of variability of the learning dynamics.

- The stochastic plasticity *slows-down* the learning, only after multiple presentations the input pattern is stored.[4]
- A slow-learning process maximizes memory capacity and prevents overfitting at the cost of learning time.
- Several *weak* classifiers can be combined to improve performances and learning speed. [5]

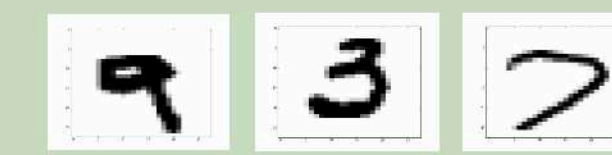


We carried out non-spiking simulations of the network obtaining 96% generalization performance. The performance of the single classifiers is comparable to their hardware, spike-based implementation and suggests the viability of the hardware solutions. The imprecise, analog circuits of our hardware are therefore compatible with machine-learning and neural-network theories that explain how variability in the classifier responses and simple pre-processing can be used to solve typical machine-learning tasks.

Some examples of correctly labeled data

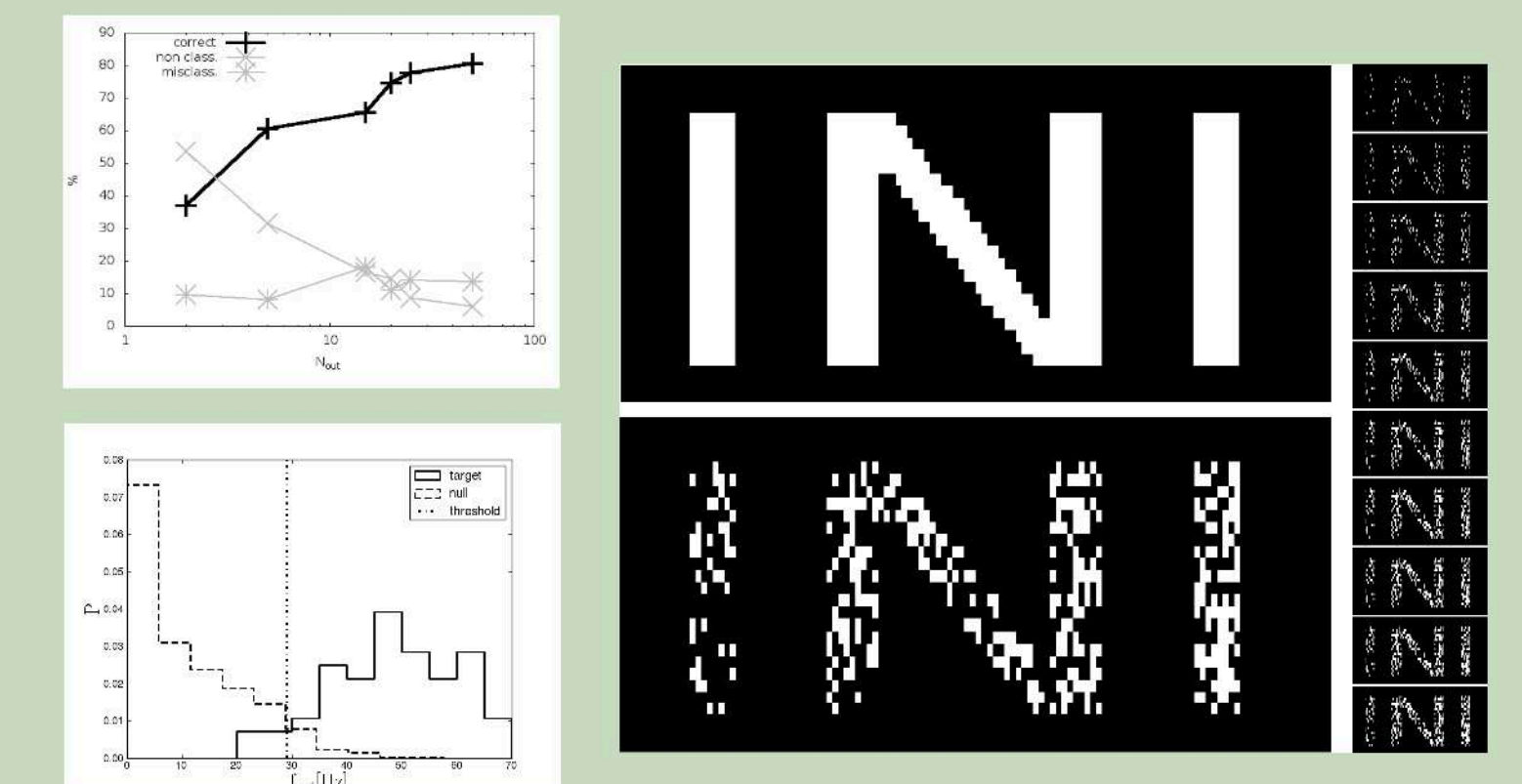


Some examples of wrongly labeled data



labeled as: 4 6 0

Fig.4 A toy example of the stochastic plasticity at work. *Middle*: the "INI" pattern is converted into trains of spikes and stimulates 3472 VLSI synapses. *Right*: the evolution of synaptic connectivity (white, potentiated synapse; black, depressed). *Bottom*: resulting synaptic levels. *Top-Left*: Combinations of classifiers improve performances of the weak hardware classification. *Bottom-Left*: Output histograms of the perceptron after learning. The neuron is considered selective for the target class.



References

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Acknowledgments

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