ECE335 Introduction to Electronic Devices

Lab 3 – MOSFETs and BJTs

Edward S. Rogers Sr. Department of Electrical and Computer Engineering
University of Toronto

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1 Introduction

This lab has two parts. Part 1 is an in-lab measurement and part 2 is a take-home lab. You measure the IV characteristics of *n*-channel and *p*-channel MOSFETs to extract the major model parameters from standard DC measurements. Then you use numerical methods to analyze supplied data of nanoscale planar, FDSOI and finFET MOSFETs which are previously measured at the *University of Toronto*. From the data, you investigate the IV characteristics and extract the threshold voltage (V_T), DIBL parameter (η), channel modulation parameter (λ), and electron mobility (μ_n), then compare the devices. Next, you are provided with data of BJT devices previously measured at the *University of Toronto.* You will extract the f_T *vs.* I_C characteristics of four SiGe *npn* Heterojunction Bipolar Transistors fabricated in four different generations of commercial SiGe BiCMOS technologies. Post-lab and pre-lab questions are to be completed in your lab groups. Submit the post lab as a PDF to Quercus. 20 marks for post lab analysis, 3 marks pre-lab, 2 marks for attendance.

2 Objectives

- To measure the IV characteristics of planar *n*-MOSFET and *p*-MOSFET
- To compare the measured IV characteristics of planer MOSFETs, FDSOI, and finFET MOSFETs.
- To learn how to extract the DC compact model parameters of MOSFETs.
- To learn how to extract f_T of different BJT devices

3 Background

- MOS Capacitor and MOSFET (Ch. 9—11, Neamen)
- Bipolar Transistors and Related Devices (Ch. 12, Neamen)

4 Equipment

- Breadboard 1 pc
- Digital multimeters (DMMs) 2 pcs
- DC power supply 1 pc
- ALD1101 and ALD1102 transistors 1 each

5 Important Note

Before beginning the experiment**, current MUST BE LIMITED TO 100 mA** from the power supply via following procedure:

1) Disconnect everything from the output port of the power supply except the connection between the '-' and GND terminals.
2) Turn the current limit to an arbitrary high value.
3) Set the output voltage to 5 V.
4) Turn the current limit to zero.
5) Connect a wire across the '+' and '-' terminals.
6) Slowly increase up the current limit until the ammeter reading of the power supply reaches 100mA.
7) Turn off the power supply and remove the short.
8) Repeat 1) through 8) on the other output of the power supply.
9) Turn on the power supply. Do not change the current limit.

6 Procedure

6.1 Quick MOSFET check with a multimeter:

MOSFET is like a capacitor between its Gate and Source terminals and between its Gate and Drain terminals. Test MOSFET using the following steps:

1- Caution! Don't touch by hand only the gate terminal as it may damage the transistor.
2- Short all terminals i.e., Gate, Source and Drain of the MOSFET with your hand, making sure you touch either the source or the drain terminal first. This step discharges the capacitor in case it was already charged.
3- Measure the resistance between the Drain and Source terminals with a multimeter. It should be an open circuit for a good MOSFET.
4- Apply a V_{GS} of a few volts (positive for NMOS and negative for PMOS) for a few seconds and then measure the Drain to Source resistance again. It must be short circuit for a working MOSFET.

6.2 Part I - Planer MOSFET IV characteristics measurement (in-lab)

To help you with the measurements, the output characteristics of the ALD1101 and ALD1102 MOSFETs have been measured with a Semiconductor Parameter Analyzer (Agilent 4155C) and are reproduced in Figure 1.

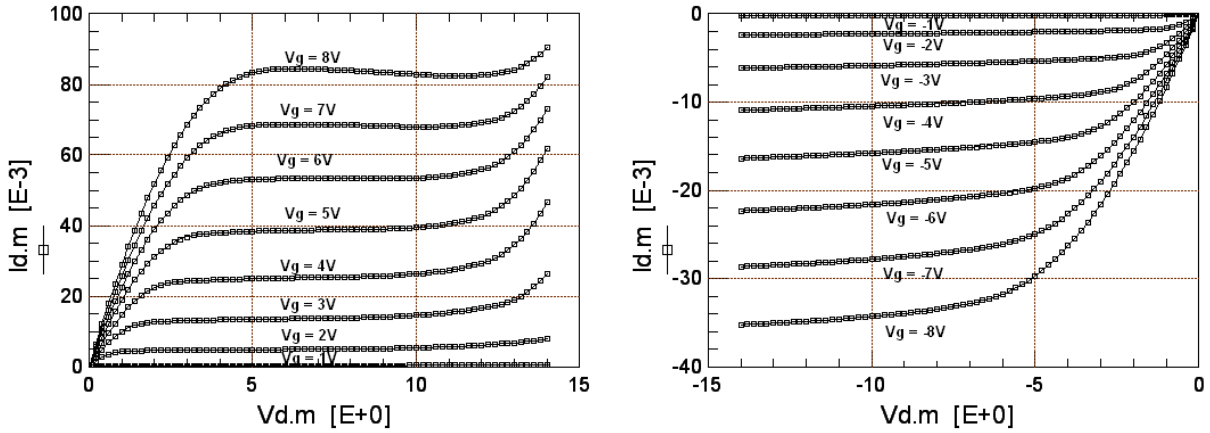


Figure 1: Output characteristics of the (a) *n*-channel MOSFET (ALD1101) and the (b) *p*-channel MOSFET (ALD1102)

The test setups for the *n*- and *p*-channel MOSFETs are shown in Figure 2 (a) and (b), respectively. Figure 2 (c) shows the package pins. Please note that the ALD1101 and the ALD1102 ICs contain an *n*-MOS and a *p*-MOS pair, respectively. Each device in the pair has its own source, gate, and drain terminal, and shares a common substrate (Bulk) terminal connected to the substrates of the both the devices. For this experiment, you will need only one of the two devices of the pair.

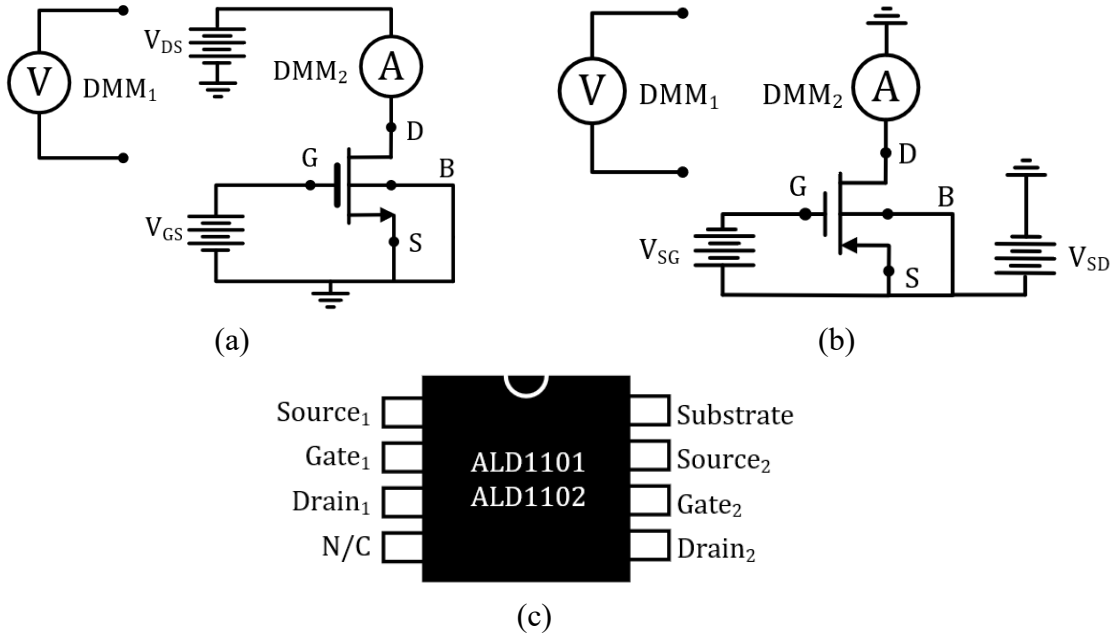


Figure 2: DC measurement circuit schematics of (a) the *n*-MOSFET and (b) *p* -MOSFET. (c) package pins for the *n*- and *p*-channel MOSFET pairs

1) Build the test setup for the *n*-MOSFET (ALD1101) on the breadboard (See Figure 2(a)). Set DMM_1 for the DC voltage measurement and DMM_2 for the DC current measurement.

DMM$_1$ is used to measure the drain-source (V_{DS}) and gate-source (V_{GS}) voltages. DMM$_2$ is connected in series to monitor the drain current (I_{DS}).

2) Measure the transfer characteristics of the *n*-MOSFET by setting V_{DS} to 0.04V, 1V, 4V, and 10V and measuring I_D *vs.* V_{GS} with 1V increments from 0V to 10V. Plot I_D *vs.* $V_{GS.}$ What is the maximum drain current (I_{ON})?

3) Measure the output characteristics of the *n*-MOSFET by setting V_{GS} to 0.4V, 1V, 4V, and 10V and measuring I_D *vs.* V_{DS} with 1V increments from 0V to 10V. Plot I_D *vs.* $V_{DS.}$

4) ***This step may cause destructive damage to the MOSFET, so proceed only after you are satisfied with the data from steps 2) and 3).*** Measure the breakdown region of the output characteristics by using the set-up from step 3) and by incrementing V_{DS} beyond 10V while V_{GS} remains fixed at 4V. For this measurement, V_{DS} should be increased at smaller increments (e.g. 0.25V) in order not to burn the MOSFET. Increase V_{DS} until I_D is 150% of I_D at V_{DS} = 5V.

5) Repeat steps 1) through 3) for the *p*- MOSFET (ALD1102) with V_{DS} reversed to V_{SD} and V_{GS} reversed to V_{SG} (See Figure 2(b))

6.3 Part II – Data analysis (Take home)

This part requires the use of *MATLAB* or similar software. Compare the nanoscale planer, finFET and FDSOI MOSFET technologies by analyzing the data provided. Answer the questions in your post-lab report.

6.3.1 Planar MOSFET

The measured data used in this part are included in the following files:

Table I planar MOSFET files

No.	File name	Device description		
		Channel	L_{drawn} (nm)	W (μm)
1	planar_lp065_w1_n80_transfer.txt	*n*	65	80×1
2	planar_lp065_w1_n80_output.txt	*n*	65	80×1
3	planar_lp090_w1_n80_transfer.txt	*n*	90	80×1
4	planar_lp090_w1_n80_output.txt	*n*	90	80×1
5	planar_lp13_w1_n80_transfer.txt	*n*	130	80×1
6	planar_lp13_w1_n80_output.txt	*n*	130	80×1
7	planar_lp18_w1_n80_transfer.txt	*n*	180	80×1
8	planar_lp18_w1_n80_output.txt	*n*	180	80×1
9	planar_lp25_w1_n80_transfer.txt	*n*	250	80×1
10	planar_lp25_w1_n80_output.txt	*n*	250	80×1
11	planar_lp35_w1_n80_transfer.txt	*n*	350	80×1
12	planar_lp35_w1_n80_output.txt	*n*	350	80×1

These measurements were performed on *n*-channel MOSFETs with different channel lengths (L) fabricated in a 65 nm technology. Along with the measurement data, these files also contain the measurement conditions. For example, the transfer characteristics files contain the V_{DS} values at which the I_{DS} *vs.* V_{GS} sweeps were measured, and the output characteristics files contain the V_{GS} values at which the I_{DS} *vs.* V_{DS} sweeps were measured.

Alternatively, you may use the following MATLAB file which has the data pre-imported: *planar_lpxxx_w1_n80_data.mat.*

After you have imported the data, perform the following steps: (*MOSFET Parameter Extraction procedures are given in the appendix at the end).*

1) Extract the threshold voltage (V_{t0}) from the transfer characteristics in the triode region (I_{DS} *vs.* V_{GS} for V_{DS} = 0.04V) for each of the MOSFETs with L = 65, 90, 130, 180, 250, and 350 nm. Describe the observed trend for threshold voltage vs channel length. For the L = 65 nm device only, plot I_{DS} *vs.* V_{GS} and g_m *vs.* V_{GS} at V_{DS} = 0.04V. Identify V_{t0} on the plot. (1 mark)

2) Extract the DIBL parameter (η) from the transfer characteristics (I_{DS} vs V_{GS} at V_{DS} = 0.04V, 1.2V) of the L = 65 nm device. Plot $log_{10}(I_{DS})$ *vs.* V_{GS} at V_{DS} = 0.04 and 1.2V. Determine η. (1 mark)

3) Extract the channel length modulation (λ) parameter from the output characteristics (I_{DS} *vs.* V_{DS} for V_{GS} = 0.2, 0.4, 0.6, 0.8, 1.0 and 1.2V) for the *n*-MOSFET with L = 65 nm. Why does λ change with V_{GS}? (1 mark)

4) Find g_{mlin} of linear region where $g_{mlin} = \frac{(V'_{DS} \cdot W)}{g_{mlin(peak)}} = \frac{(L_{drawn} - \Delta L)}{k'_n}$ (See appendix). Plot $\frac{(V'_{DS} \cdot W)}{g_{mlin(peak)}}$ vs L_{drawn}, where L_{drawn} is the drawn gate length for the 65 nm to 350 nm devices. V'_{DS} is the drain to source voltage that has been corrected for IR losses. Extract k_n from the slope and ΔL from the *x*-intercept. What is the effective gate length ($L_{eff} = L_{drawn} - \Delta L$) of the 65 nm device? (1 mark)

6.3.2 FD-SOI and finFET MOSFETs

The measured IV characteristics of the *n*- & *p*-FDSOI and *n*- & *p*-finFET MOSFET devices are provided in the following files listed in the tables below,

Table II FDSOI MOSFET files

No.	File name	Device description		
		Channel	L_{drawn} (nm)	W (μm)
1	nfdsoi_lp02_wp43_n40_transfer.csv	*n*	20	40×0.43
2	nfdsoi_lp02_wp43_n40_output.csv	*n*	20	40×0.43
3	pfdsoi_lp02_wp43_n40_transfer.csv	*p*	20	40×0.43
4	pfdsoi_lp02_wp43_n40_output.csv	*p*	20	40×0.43

Table III finFET MOSFET files

No.	File name	Device description				
		Channel	N_f	N_{fin}	L_{drawn}	W (μm)
5	nfinfet_lp008_wp09_n192_transfer.csv	*n*	48	4	8 nm	48×4× 90
6	nfinfet_lp008_wp09_n192_output.csv	*n*	48	4	8 nm	48×4× 90
7	pfinfet_lp008_wp09_n192_transfer.csv	*p*	48	4	8 nm	48×4× 90
8	pfinfet_lp008_wp09_n192_output.csv	*p*	48	4	8 nm	48×4× 90

Like with the planar MOSFET data of the previous section, the transfer characteristics files contain the V_{DS} values at which the I_{DS} vs V_{GS} sweeps were measured, and the output characteristics files contain the V_{GS} values at which the I_{DS} vs V_{DS} sweeps were measured.

After you have imported the data, follow similar steps to that performed on the planar *n*-MOSFET in the previous section to compare the three different technologies. Use the L = 65nm *n*-MOSFET analyzed previously for your comparisons to the FDSOI MOSFET (*n*-channel: L_{drawn} = 20 nm, W = 80×0.43 μm) and the finFET (*n*-channel: L_{drawn} = 8 nm, W = 48×4× 90 nm).

1) Plot I_{DS} vs V_{GS} and g_m vs V_{GS} at the smallest V_{DS} bias indicated and identify V_{t0} on the plot (See appendix). Plot together to enable comparisons.

a) Compare the threshold voltages between FDSOI and finFET technologies. Note that the V_{GS} values for which measurements are provided are the safe DC voltage operating range without risking damage. (1 mark)

b) Compare the peak transconductance (g_m/W) and on-current (I_{ON}/W) values between FDSOI and finFET technologies at their respective largest V_{DS} bias for which data is provided. Note that comparisons are only fair if they are normalized to the effective device width since transconductance is proportional to device width in the MOSFET IV characteristics equations. (1 mark)

c) Compare the subthreshold slope of the minimum gate length *n*-MOSFETs in each technology (1 mark)

d) Compare the DIBL parameter between technologies. (1 mark)

2) Plot the output characteristics for the FDSOI and finFET *n*- and *p*- channel devices and extract the channel length modulation parameter (λ) for each. (1 mark)

3) The measured HF C-V characteristics of *n*-FDOIS and *n*-finFET are shown in the Figure 3 and 4, respectively. Using the provided data, answer the following questions.

a) Identify the range of V_G values for which the MOSFET is in inversion or depletion. (1 mark)

b) What are the maximum and minimum capacitance values? (1 mark)

c) If the measured FDSOI MOSFET in Figure 3 is composed of 40 gate fingers in parallel, each with length $L_g = 20\,nm$ and width $W_f = 430\,nm$, then estimate the equivalent oxide thickness t_{OXE} of the *n*-FDSOI MOSFET (1 mark)

d) If the measured *n*-finFET in Figure 4 is composed of 192 fins in parallel, each with length $L_g = 8\,nm$ and effective width $W_f = 90\,nm$, estimate the equivalent oxide thickness t_{OXE} of the *n*-finFET and the thickness of the silicon fin. (1 mark)

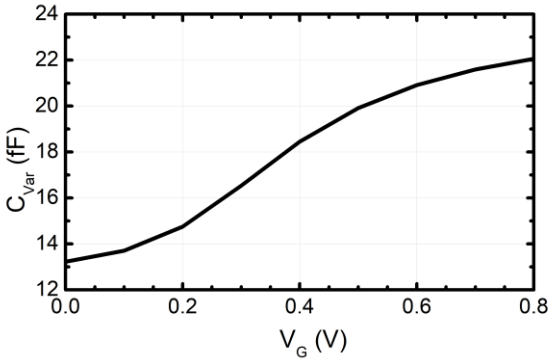


Figure 3 The measured HF C-V characteristics of a FDSOI n-MOSFET varactor with 40 devices in parallel, gate length $\boldsymbol{L_g = 20\,nm}$ and finger width $\boldsymbol{W_f = 430\,nm}$.

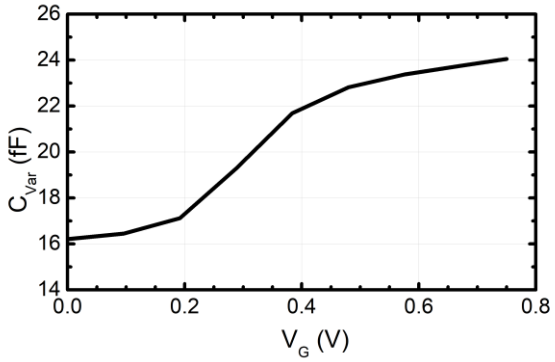


Figure 4 Measured HF C-V characteristics of a *n*-FinFET with 192 fins, gate length $\boldsymbol{L_g = 8\,nm}$ and effective fin width $\boldsymbol{W_f = 90\,nm}$.

6.3.3 Commercial BiCMOS Technologies

You are provided with the following *$20log_{10}|H_{21}|$ vs. frequency measurements* of *npn* SiGe HBTs in three commercial SiGe BiCMOS technologies:

- bicmos6g_H21_vs_freq.txt
- bicmos9_H21_vs_freq.txt
- b9mw_H21_vs_freq.txt

Please note that the data contained in these files have been de-embedded.

1) Plot *$20log_{10}|H_{21}|$ vs. frequency* on a semi-log scale. From the -20 dB/decade region of the plot, extract the f_T for all devices and at each bias point. (1 mark)
2) On the same figure, plot the f_T *vs.* I_C characteristics for each device on a semi-log scale. For each technology provide the peak f_T frequency and the current density at which it occurs. (1 mark)

7 Pre-Lab Questions

1) What is the meaning of the threshold voltage (V_t)? Explain a procedure to measure the threshold voltage. (1 mark)
2) MOSFETs are four-terminal devices. For each *n*-channel and *p*-channel device, explain how the body (substrate) terminal should be connected. What could happen if the substrate voltage is not appropriately biased? (1 mark)
3) What is the DIBL and channel length modulation and how to measure them? Comparing between measured planar MOSFETs and nanoscale planar MOSFET (data provided) which would show higher impact of DIBL and channel length modulation? (1 mark)

8 Results

For the measured *n*- and *p*-channel MOSFETs, include the following data in your post-lab report:

- Plot I_D *vs.* V_{GS} at V_{DS} = 10V with I_{ON} labeled (1mark)
- Plot g_m *vs.* V_{GS} ($g_m = \Delta I_D/\Delta V_{GS}$) at V_{DS} = 10V with $g_{m(peak)}$ labeled (1mark)
- Compute the threshold voltage (V_{T0}) (1mark)
- Plot I_D *vs.* V_{DS} and identify the breakdown region (1mark)
- Plot g_d *vs.* V_{DS} ($g_d = \Delta I_D/\Delta V_{DS}$) and extract λ (1mark)

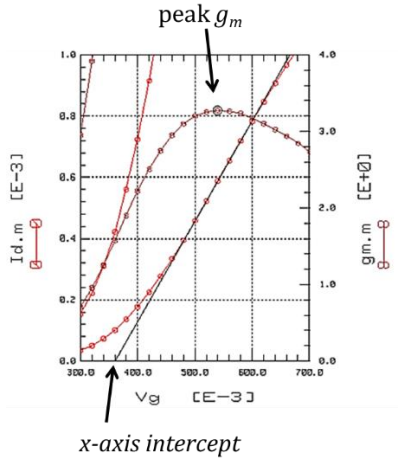
For the data analysis, include all the answers to the questions in your post-lab report.

9 Post-Lab Questions

Post lab report should include all the results from Part 1 and 2 data analysis as described in the previous sections.

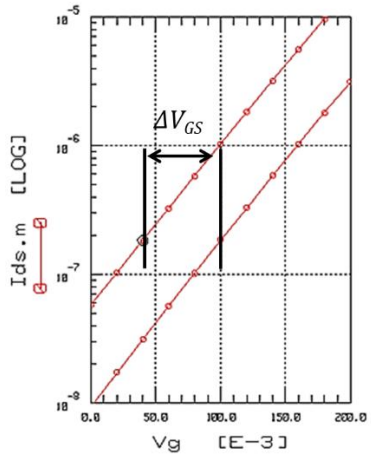
10 Appendix : Parameter Extraction

Threshold voltage (V_{t0})



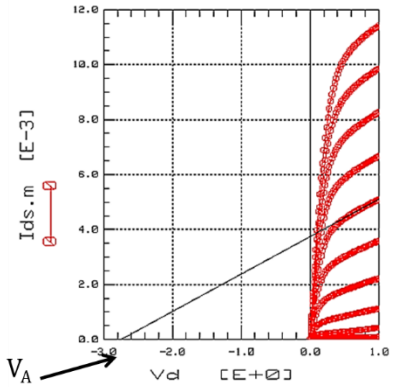
- Use the linear region of the transfer characteristics (I_{DS} vs. V_{GS}) when V_{DS} is close to zero (i.e. V_{DS} = 0.04V)
- Plot g_m vs. V_{GS}. *Remember* $g_m = \frac{\partial I_D}{\partial V_{GS}}$, *so obtain* g_m *from the plot of* I_D *vs.* V_{GS}.
- From the region where g_m peaks draw line on the *I-V* characteristics
- Find the x-axis intercept of this line
  V_{t0} = *x-axis intercept* $- \frac{3kT}{q}$

DIBL (η)



- From the sub-threshold region (log_{10} I_D *vs.* V_{GS} plot), several V_t's below the threshold voltage, read the difference in V_{GS} at fixed current between the V_{DS} = 0.04 V and V_{DS} = 1.2 V curves
- The DIBL parameter (η) is found with
  $\eta = \Delta V_{GS}/\Delta V_{DS}$
- Now, the DIBL parameter can be used to find the threshold voltage as a function of V_{DS} with
  $V_t = V_{t0} - \eta V_{DS}$

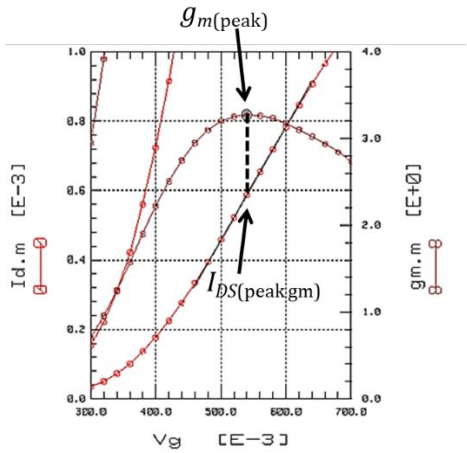
Channel length modulation (λ)



- In the output characteristics (I_{DS} *vs.* V_{DS}), draw a line in the saturation region for each curve corresponding to a constant V_{GS}
- The x-axis intercept of this line is V_A
- The channel modulation parameter is found with

$$\lambda = 1/V_A$$

Effective Channel Length (L_{eff})



- Use the linear region of the transfer characteristics (I_{DS} *vs.* V_{GS}) when V_{DS} is close to zero (i.e. V_{DS} = 0.04V)
- Plot g_m vs. V_{GS} and find the peak g_m ($g_{m(peak)}$) and the current at which it occurs ($I_{DS(peak\,gm)}$)
- Find the *IR** voltage loss and correct the V_{DS} with $V'_{DS} = V_{DS} - I_{DS(peak\,gm)}(R_S+R_D)$
- In a 65nm technology, assume R'_D and R'_S = 220 Ω·µm, to find R_S, R_D divide by the transistor width $R_D = R'_D/W$ *and* $R_S = R'_S/W$

- In the linear region, we have

$$g_{mlin} = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{\partial\left[k_n C_{ox}\frac{W}{L_{drawn}-\Delta L}\left(V_{GS}-V_t-\frac{V'_{DS}}{2}\right)V'_{DS}\right]}{\partial V_{GS}} \Rightarrow \frac{V'_{DS}W}{g_{\mathrm{mlin}\,(peak)}} = \frac{L_{drawn}-\Delta L}{k_n}$$

- Plot $\frac{V'_{DS}W}{g_{\mathrm{mlin}\,(peak)}}$ *vs.* L_{drawn} for measurement data with different channel lengths all in the same technology*

  * *This method works since the delta between L_{drawn} values is defined lithographically (ΔL is constant)*

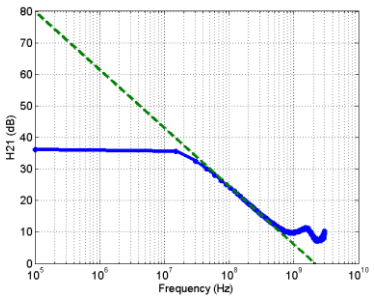
- Find k_n from *1/slope* and ΔL from the *x-axis intercept*

- Calculate the effective channel length with $L_{eff} = L_{drawn} - \Delta L$

Others

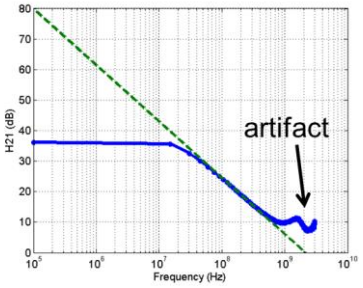
- Use the oxide thickness, t_{OX} to find $C_{OX} = \varepsilon_0\varepsilon_{ox}/t_{OX}$ where $\varepsilon_{ox} = 4$ for SiO_2
- Electron mobility (μ_n) can be found using $k_n = \mu_n C_{OX}$

Extracting f_T from S-parameter Measurements



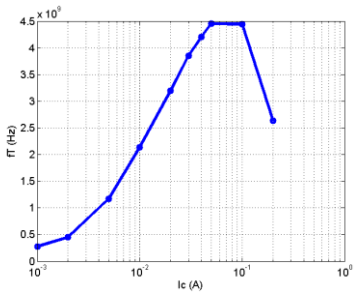
- Transform S_{DUT} into H-parameters by using the *s2h() MATLAB* function
- Use $H_{DUT}(2,1)$, which represents the current gain, to plot *$20log_{10}(H(2,1))$ vs. frequency* on semi-log scale
- Draw a line in the -20 dB/decade region
- The x-axis intercept is f_T

Cautionary Note About De-embedding Devices Mounted on a PCB



- There are physical variations between each PCB; these variations are larger on the PCB than on-chip
- As a result, an artifact may appear in the H(2,1) plot at higher frequencies.
- This artifact comes from:
  - physical difference between the fixtures that are measured and the fixture characteristics that are used to de-embed
  - distributed effects of the device package and leads
- As a result, use H_{21} portion below ~1.5GHz to find f_T

f_T vs. I_C Characteristics



- Extracting f_T at different currents and plot it similar to the one shown beside.