

COVER PAGE

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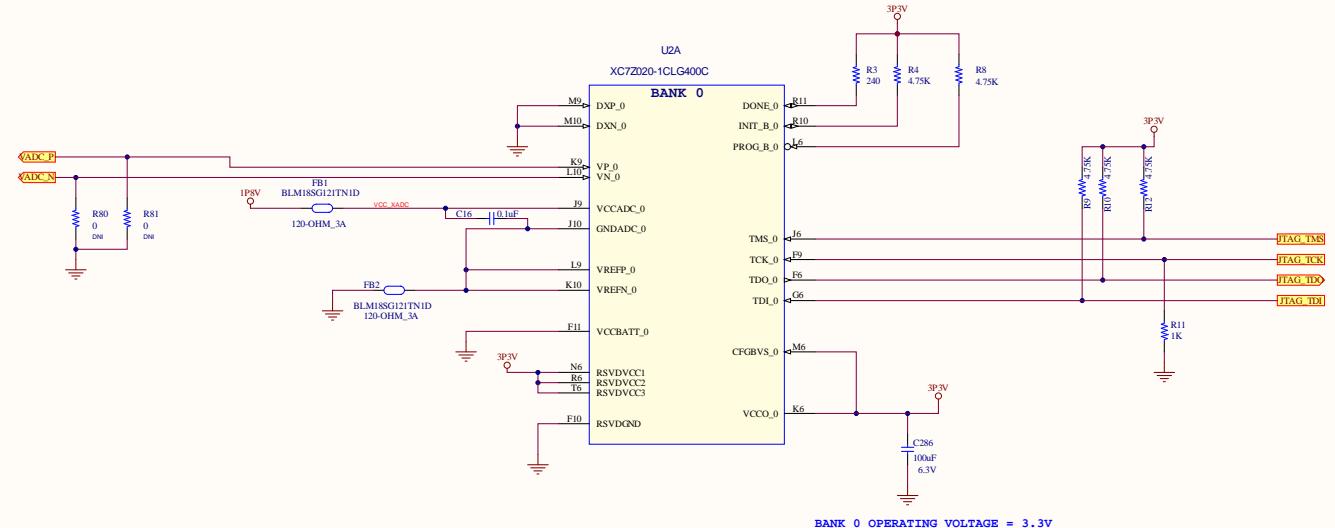
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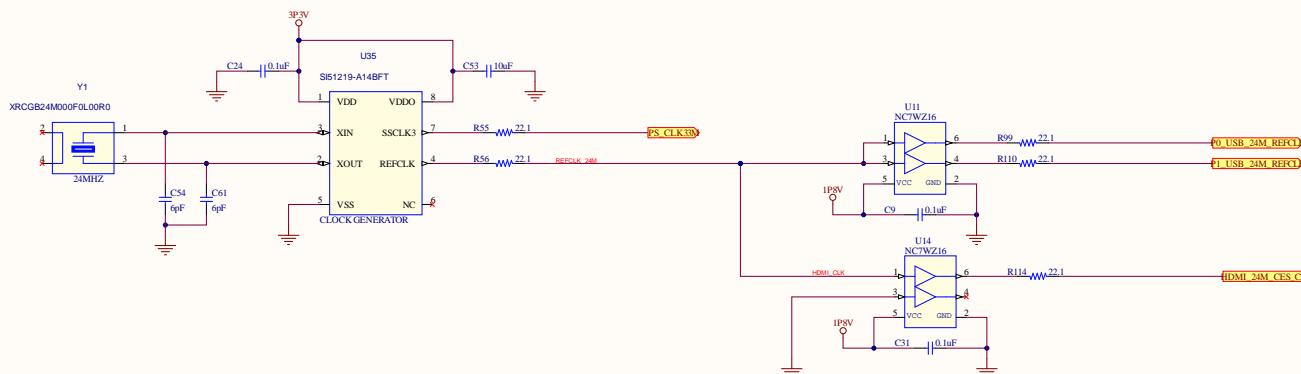
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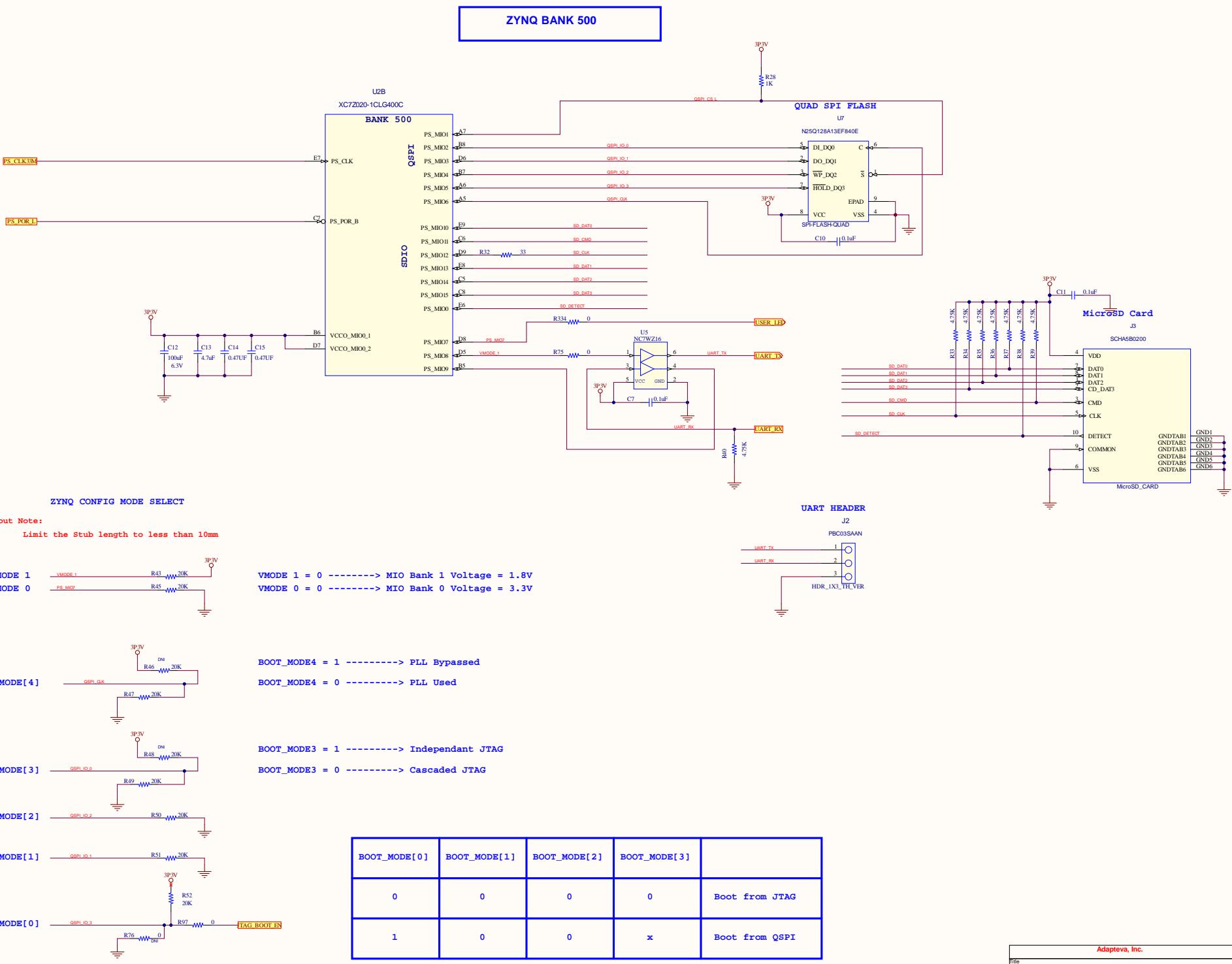
ZYNQ BANK0



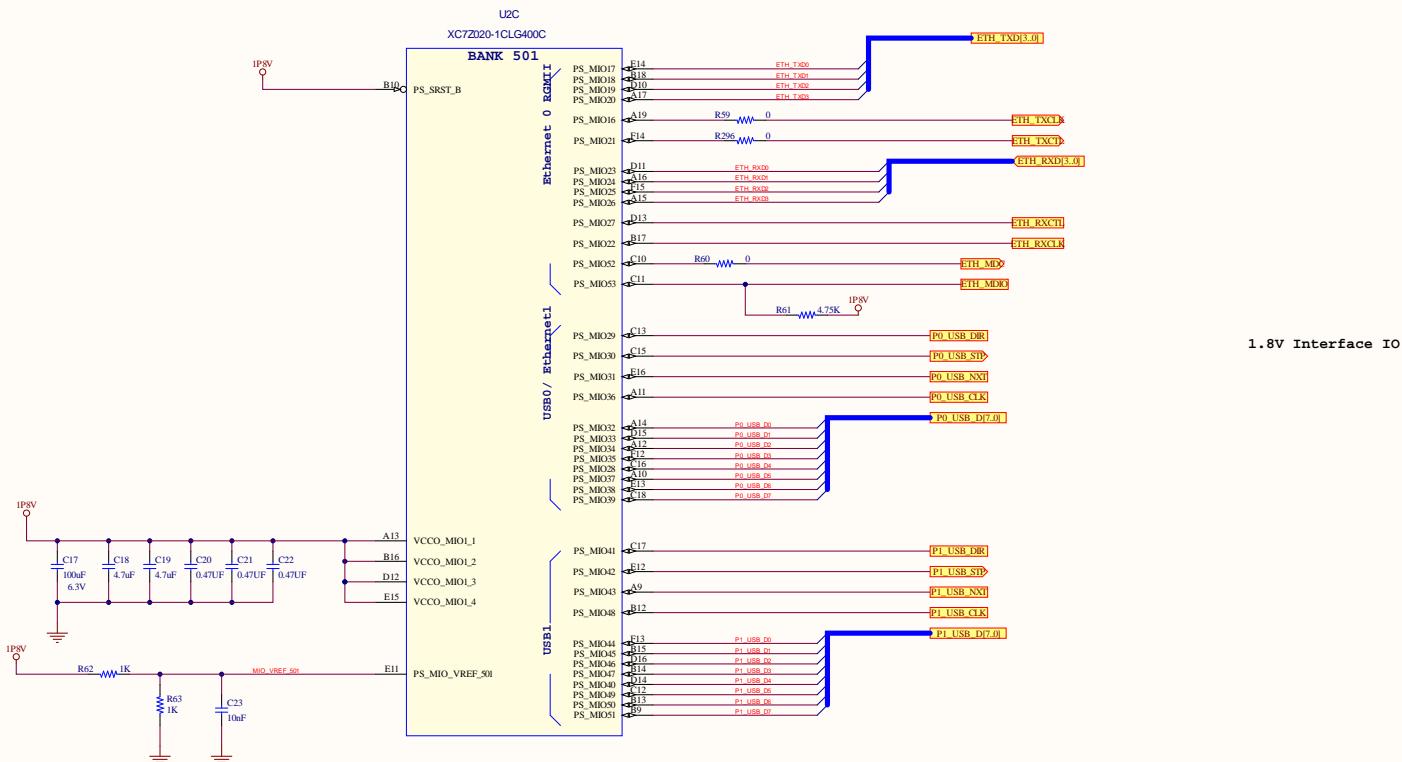
## PROGRAMMABLE CLOCK GENERATOR

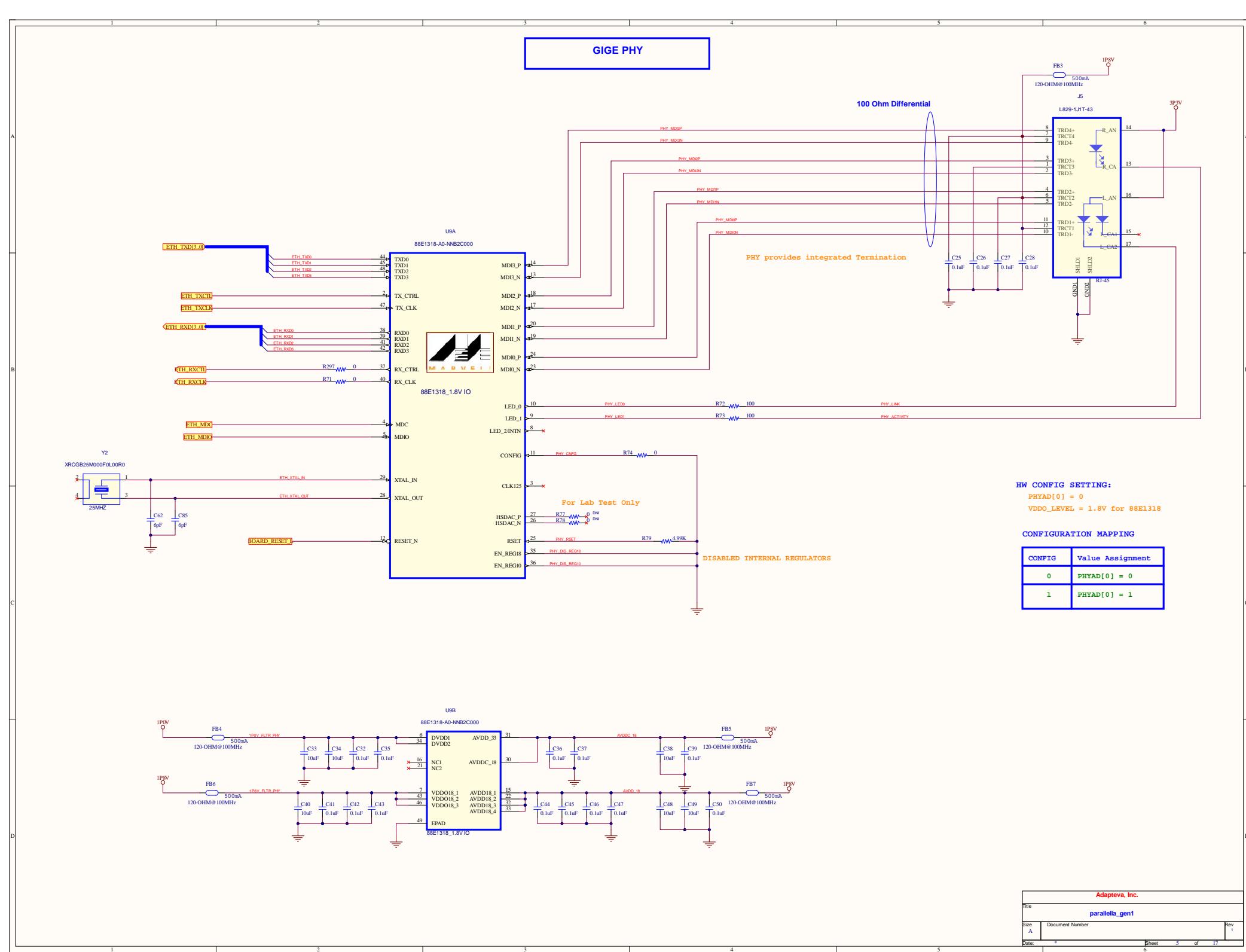
Place Close to U2

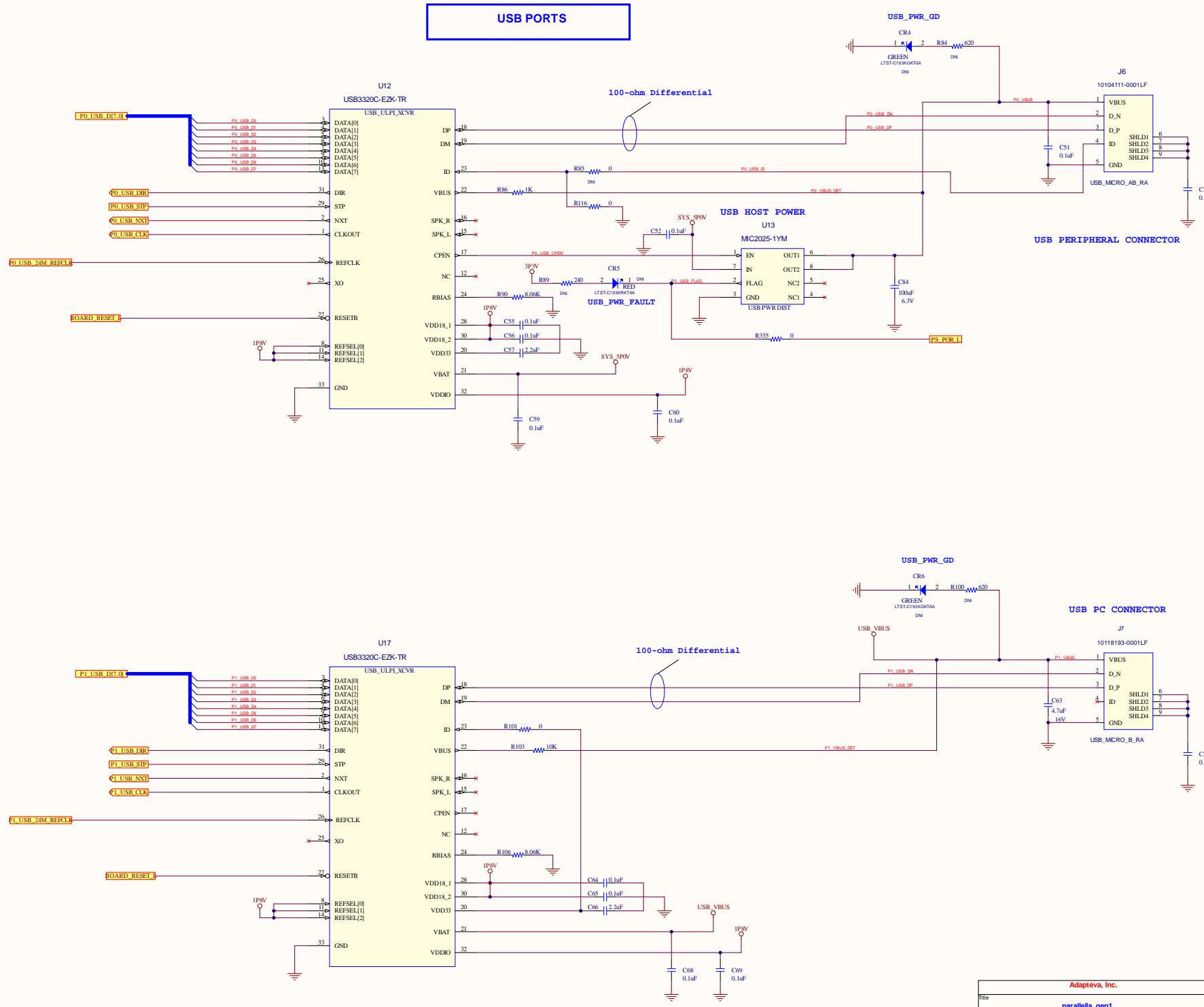




ZYNQ BANK 50

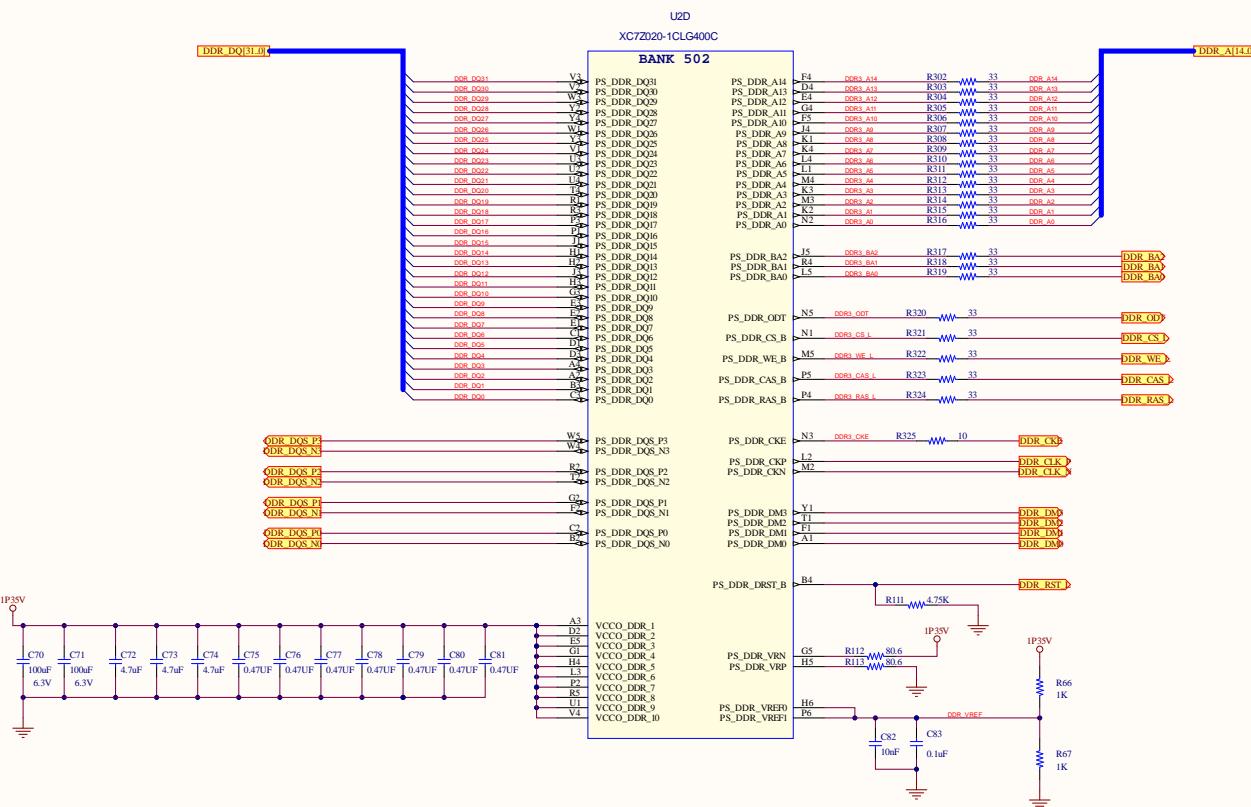




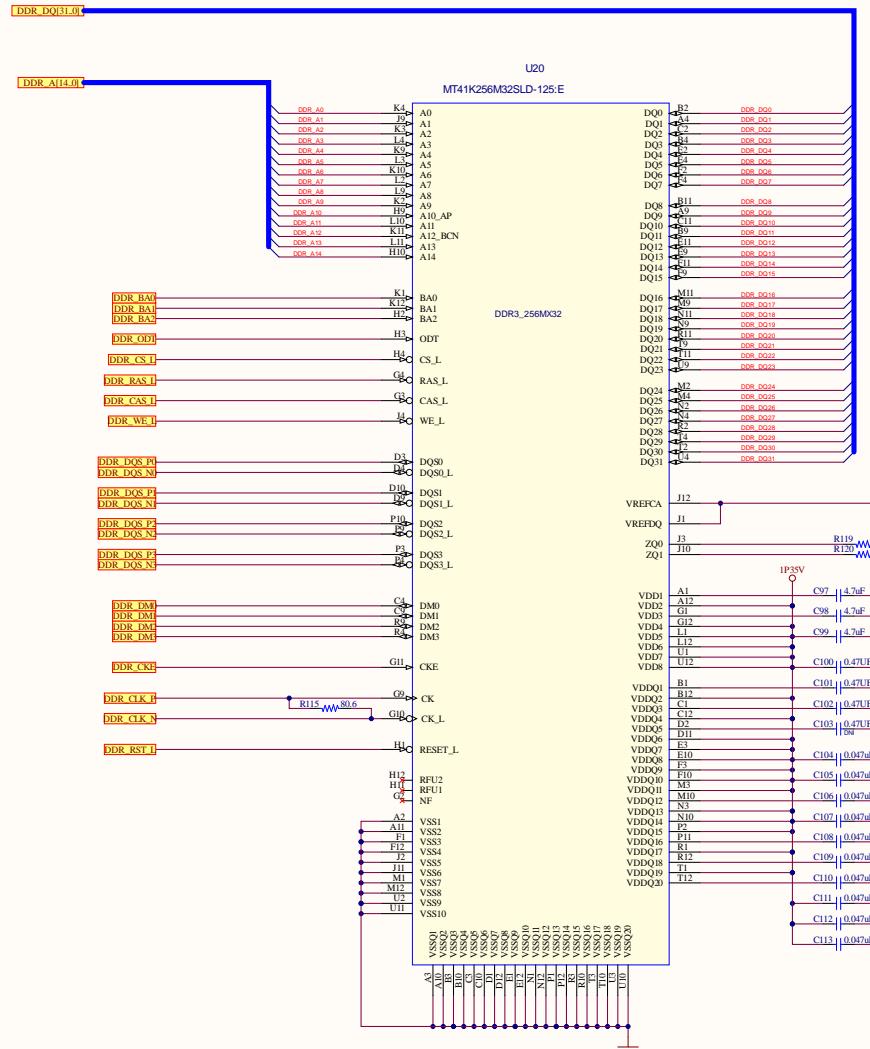


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ZYNQ BANK 502

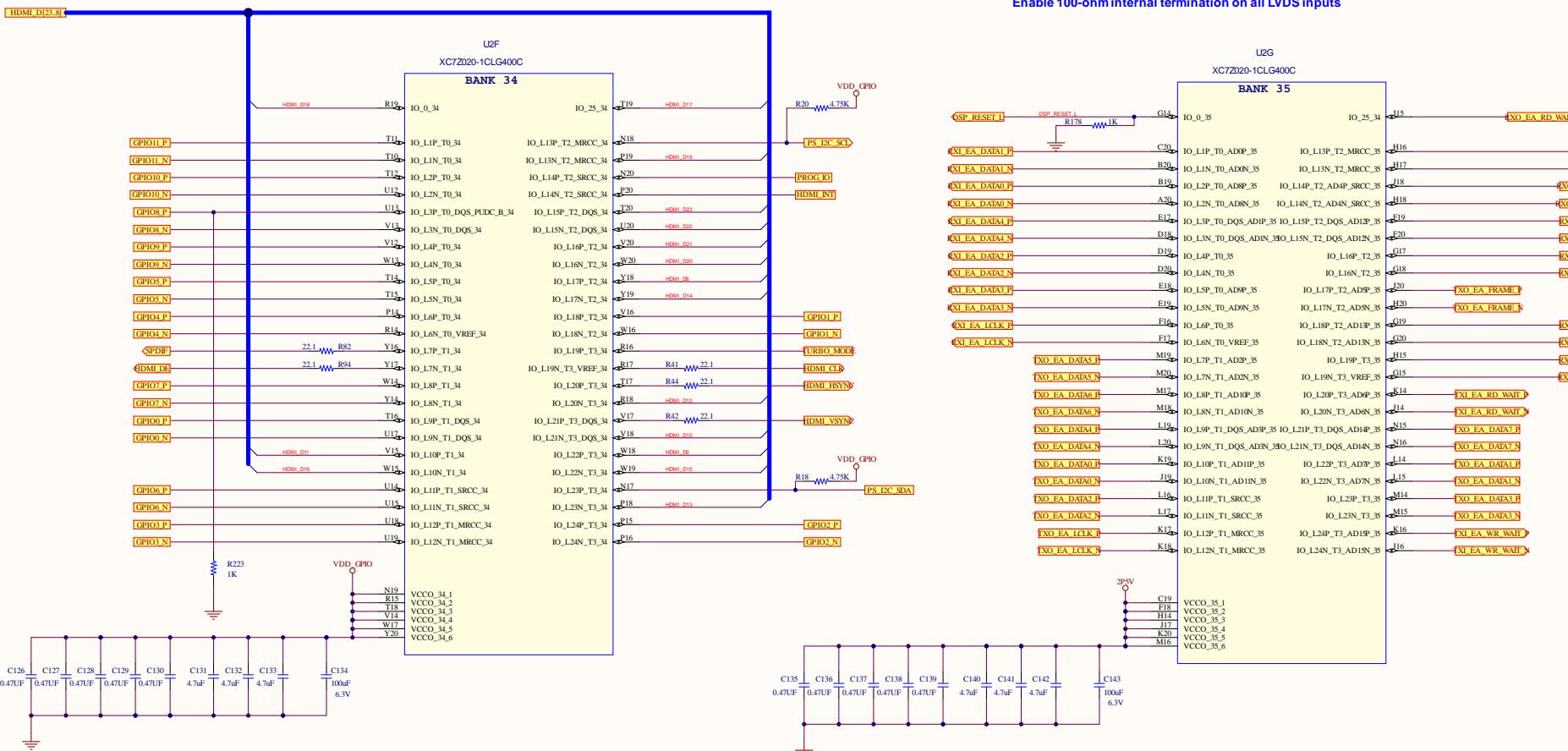


# DDR3 - 256M X 32



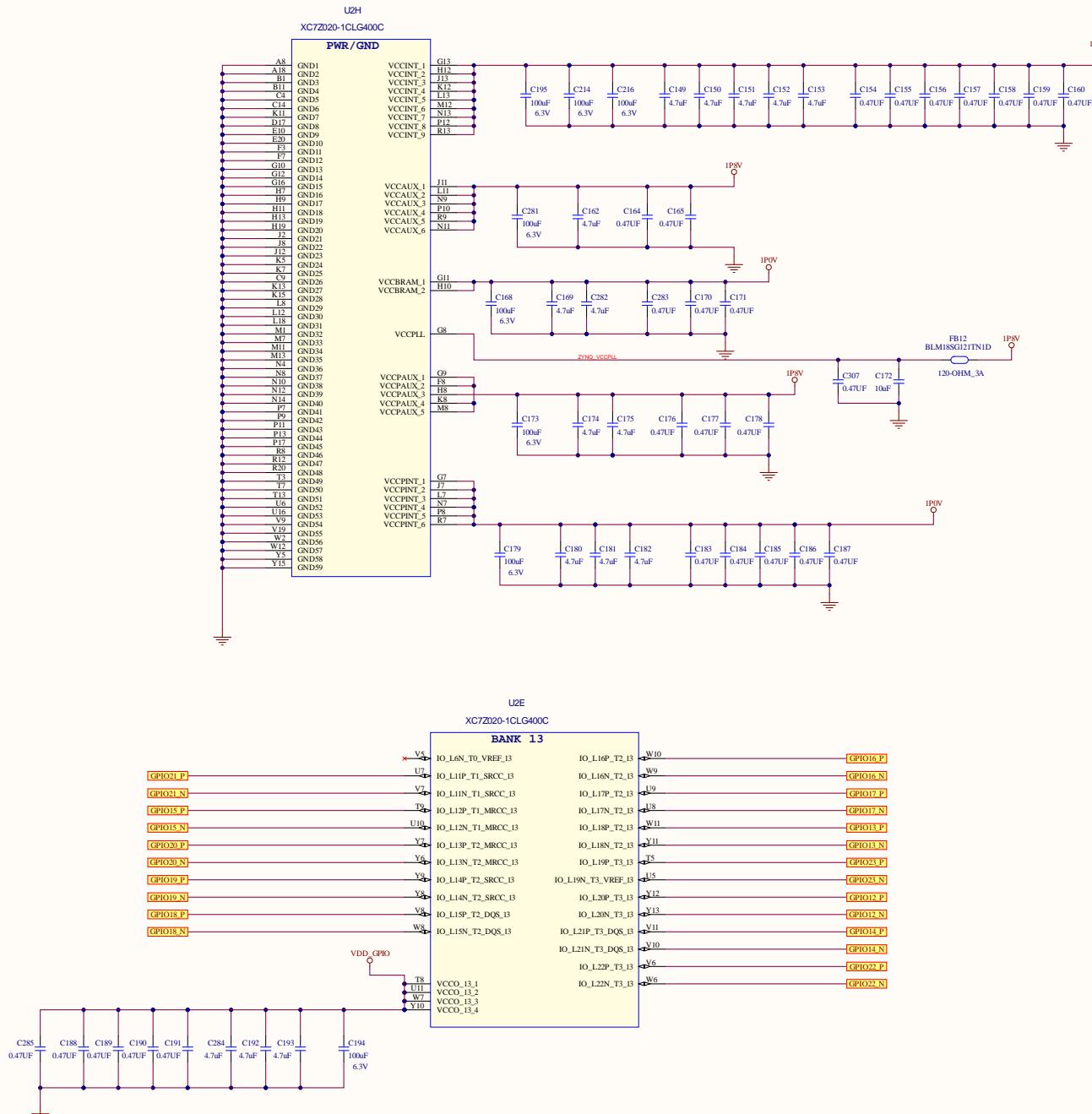
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## BANKS 34 & 35

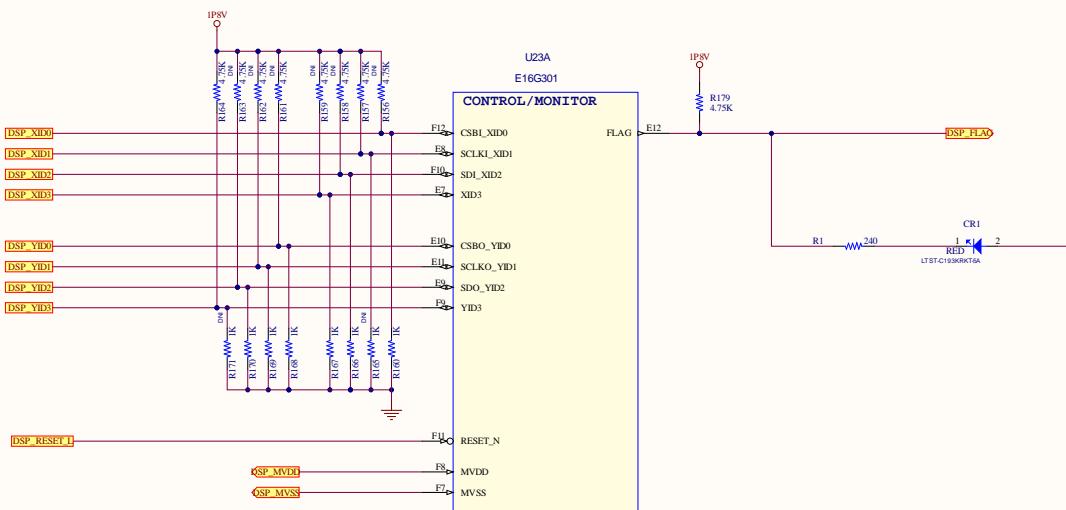


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## ZYNQ POWER &amp; GROUND



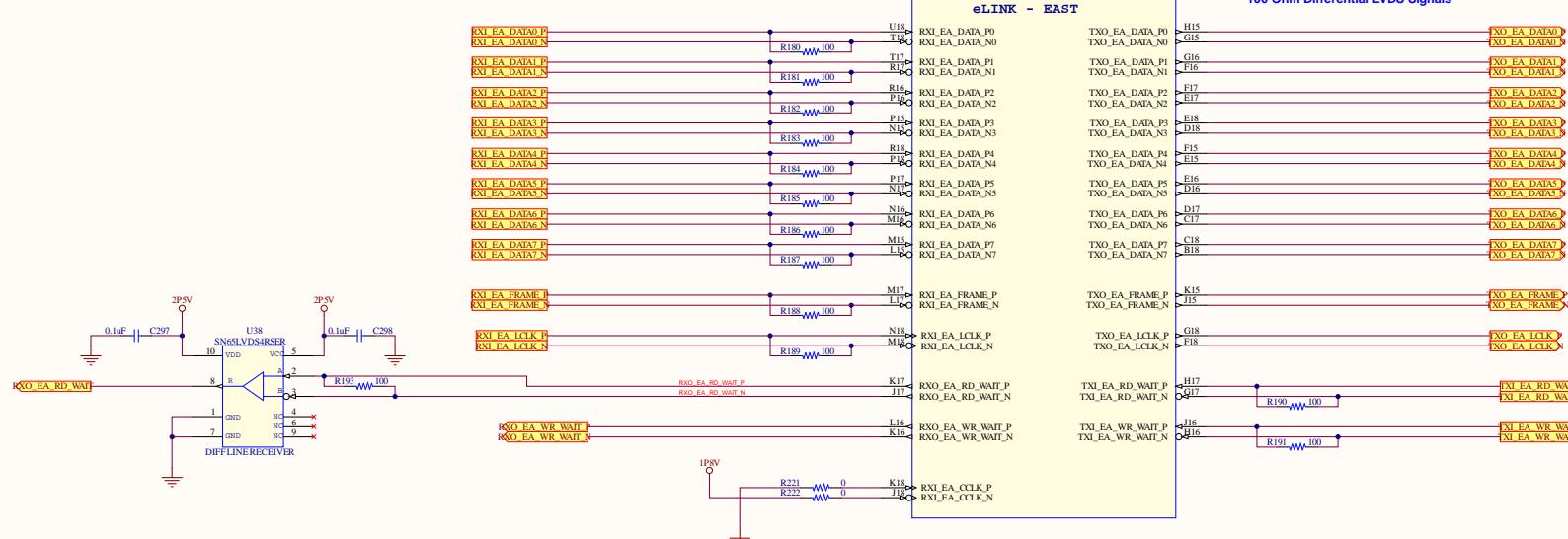
### DSP PROCESSOR 1-OF-3



100 Ohm Differential LVDS Signals

E16G301 eLINK - EAST

100 Ohm Differential LVDS Signals



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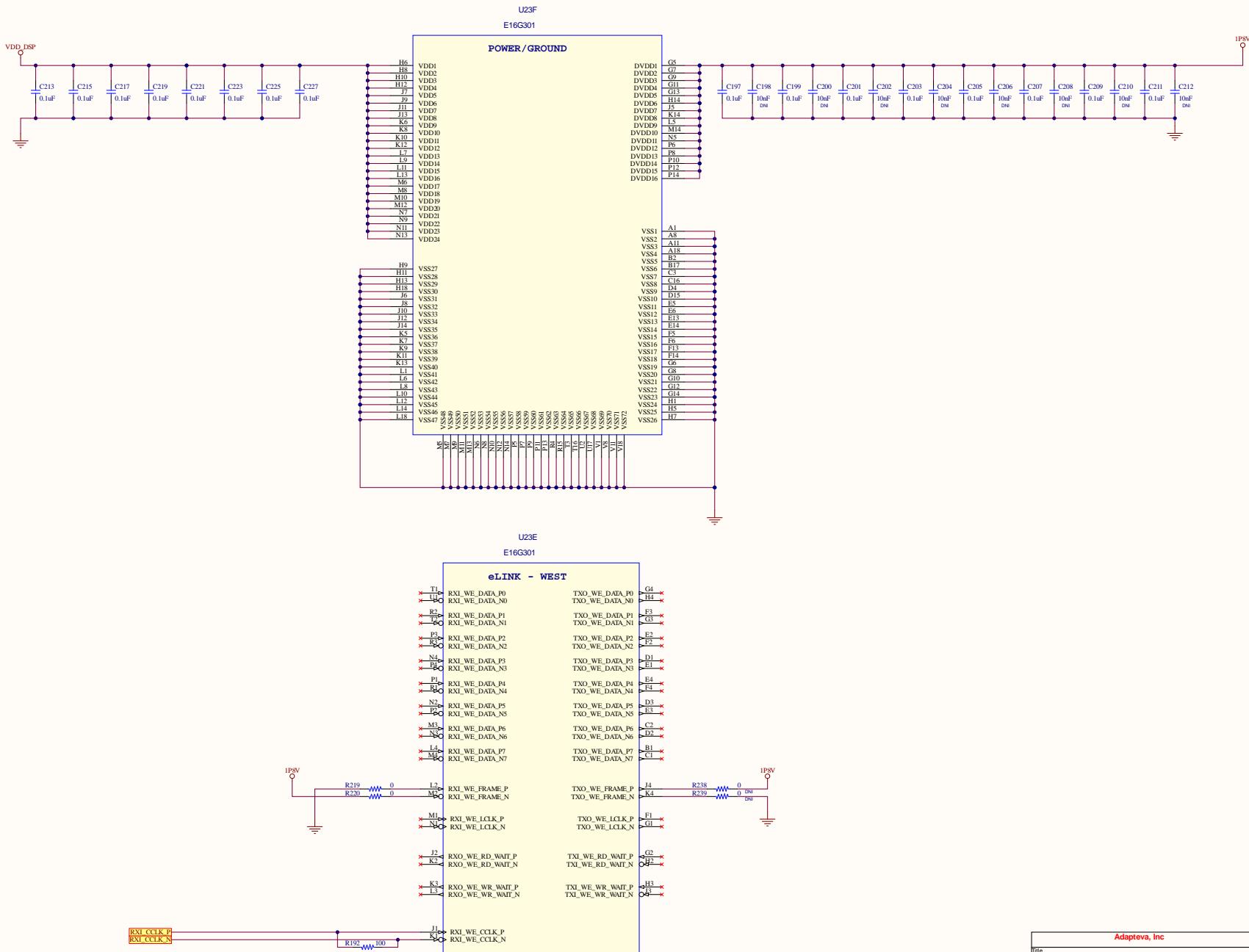
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## DSP PROCESSOR 2-OF-3

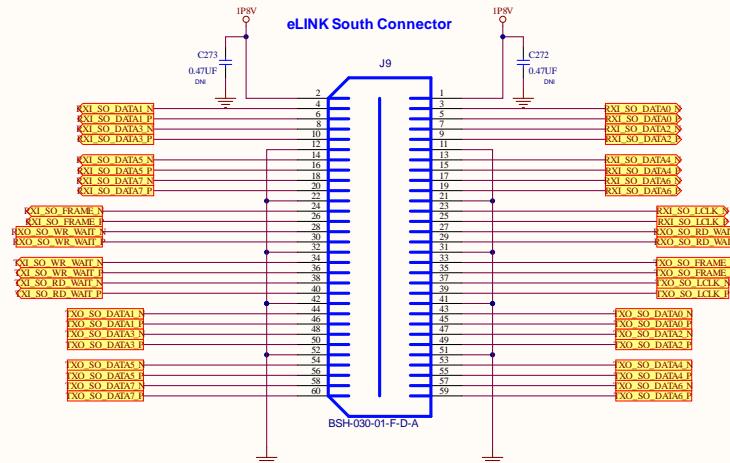
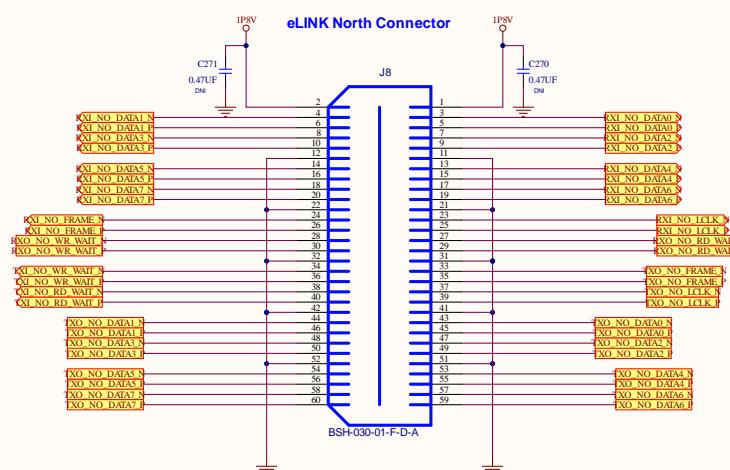


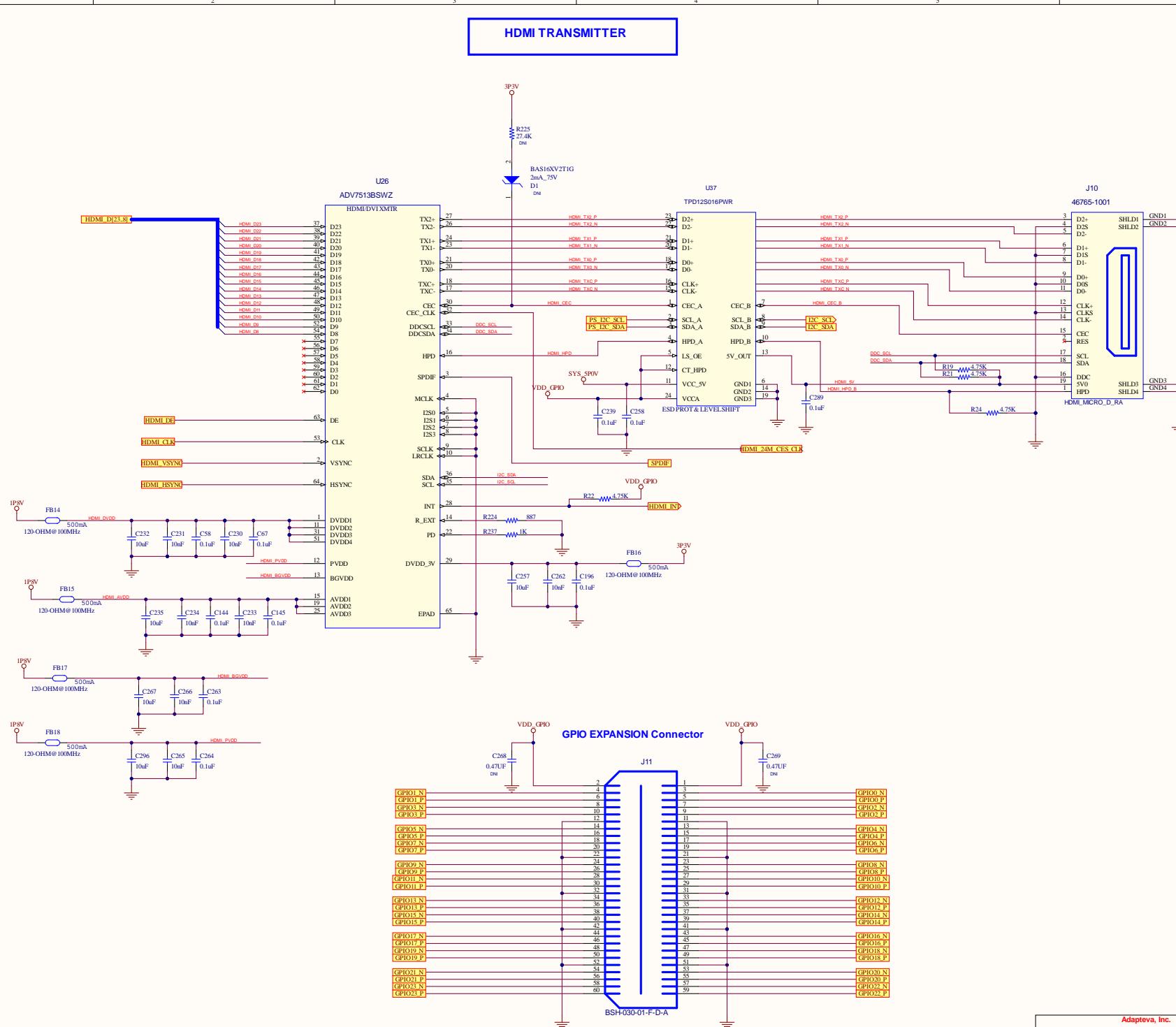
### DSP PROCESSOR 3-OF-3



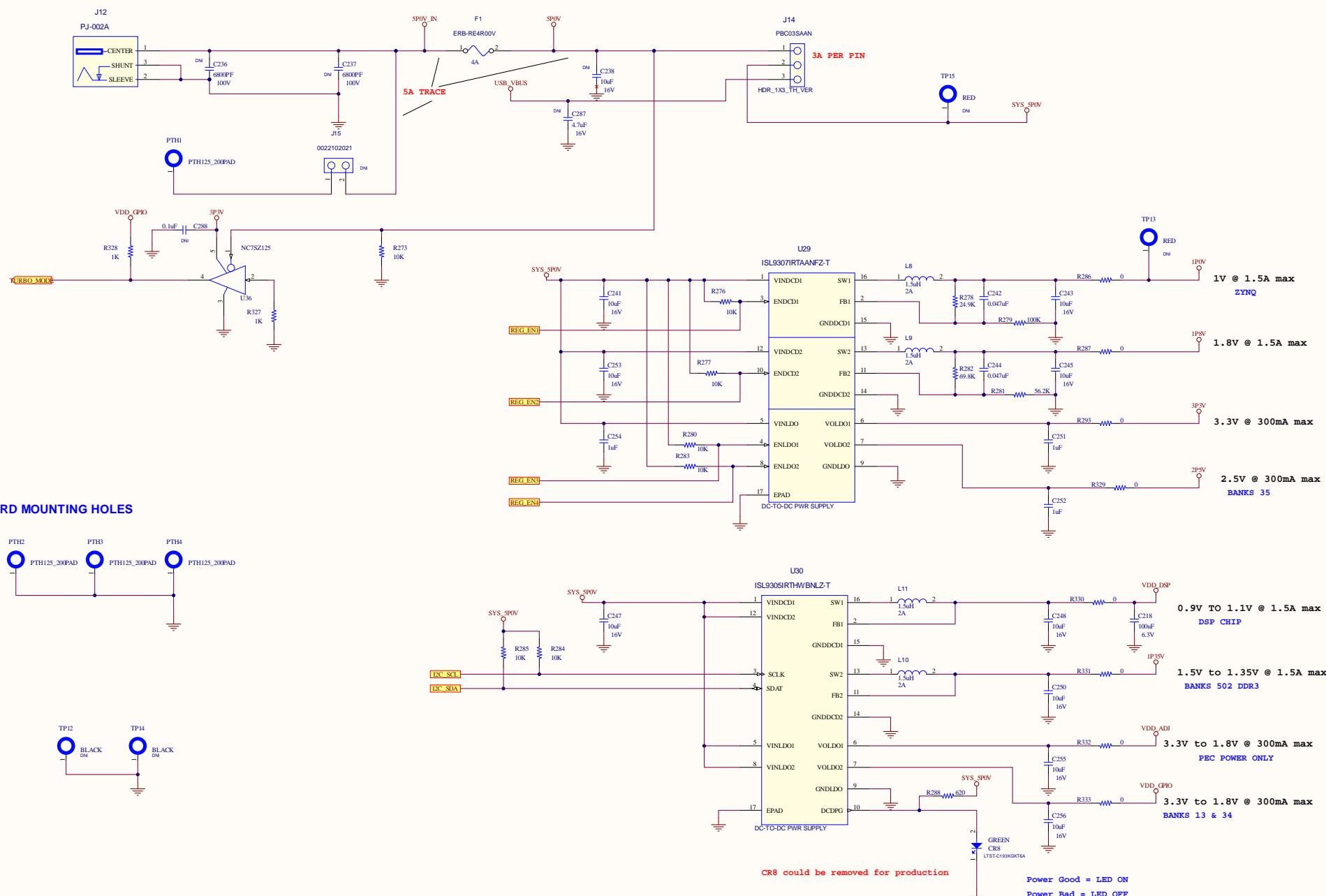
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**DSP eLINK CONNECTORS**





## POWER MANAGEMENT



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## RESET GENERATION

