

COVER PAGE

Page List

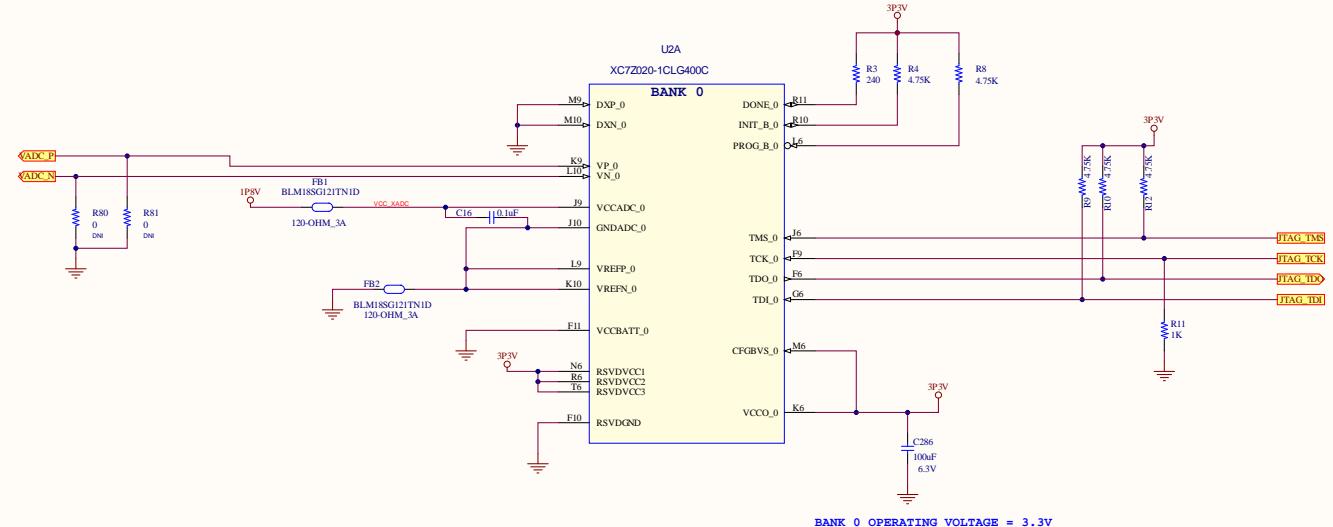
Page	Content
1	COVER PAGE
2	ZYNQ BANK 0
3	ZYNQ BANK 500
4	ZYNQ BANK 501
5	GIGE PORT
6	USB PORTS
7	ZYNQ BANK 502
8	DDR3-256Mx32
9	PL BANK 34 & 35
10	ZYNQ PWR & GND
11	DSP PROCESSOR 1-OF-3
12	DSP PROCESSOR 2-OF-3
13	DSP PROCESSOR 3-OF-3
14	DSP eLINK CONNECTORS
15	HDMI INTERFACE
16	POWER MANAGEMENT
17	RESET GENERATION

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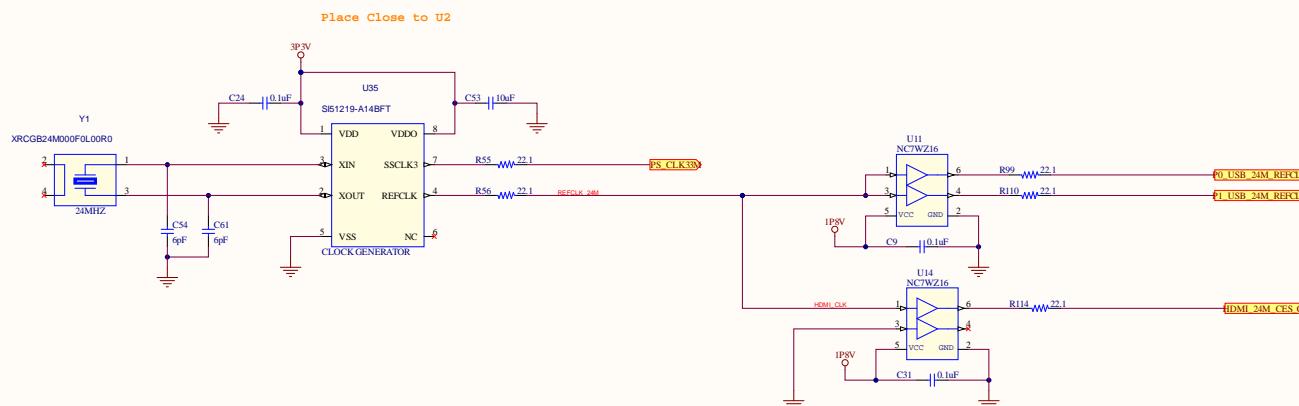
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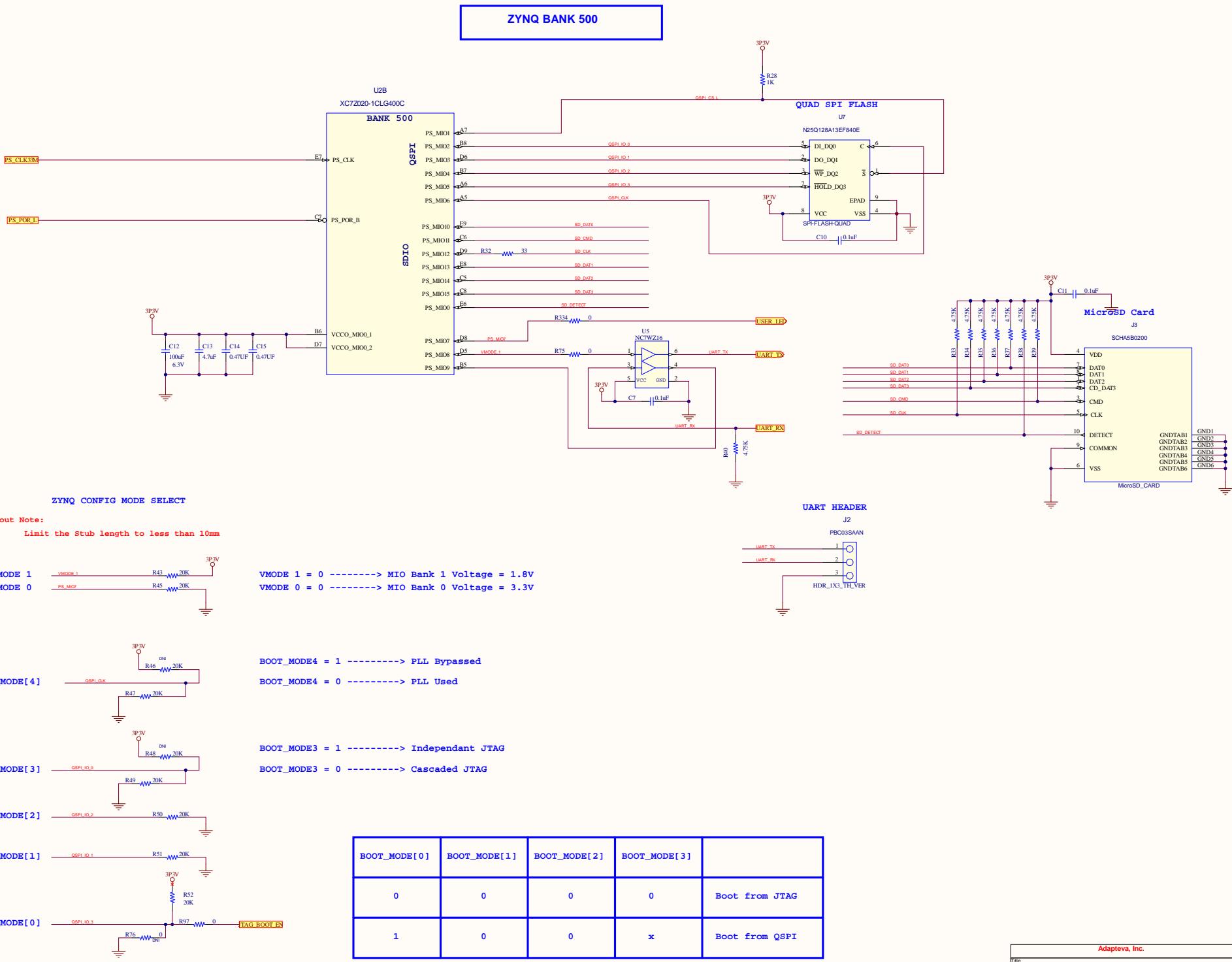
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ZYNQ BANK0

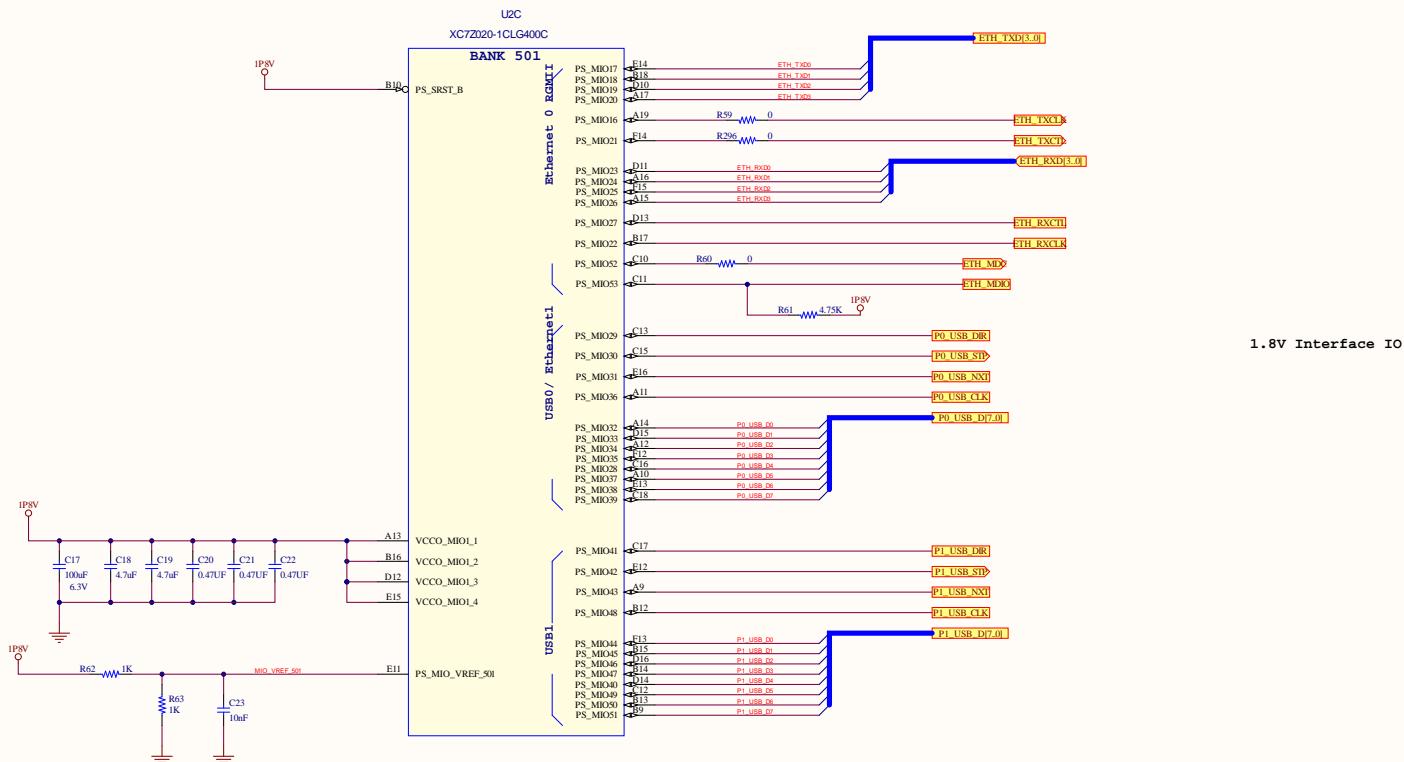


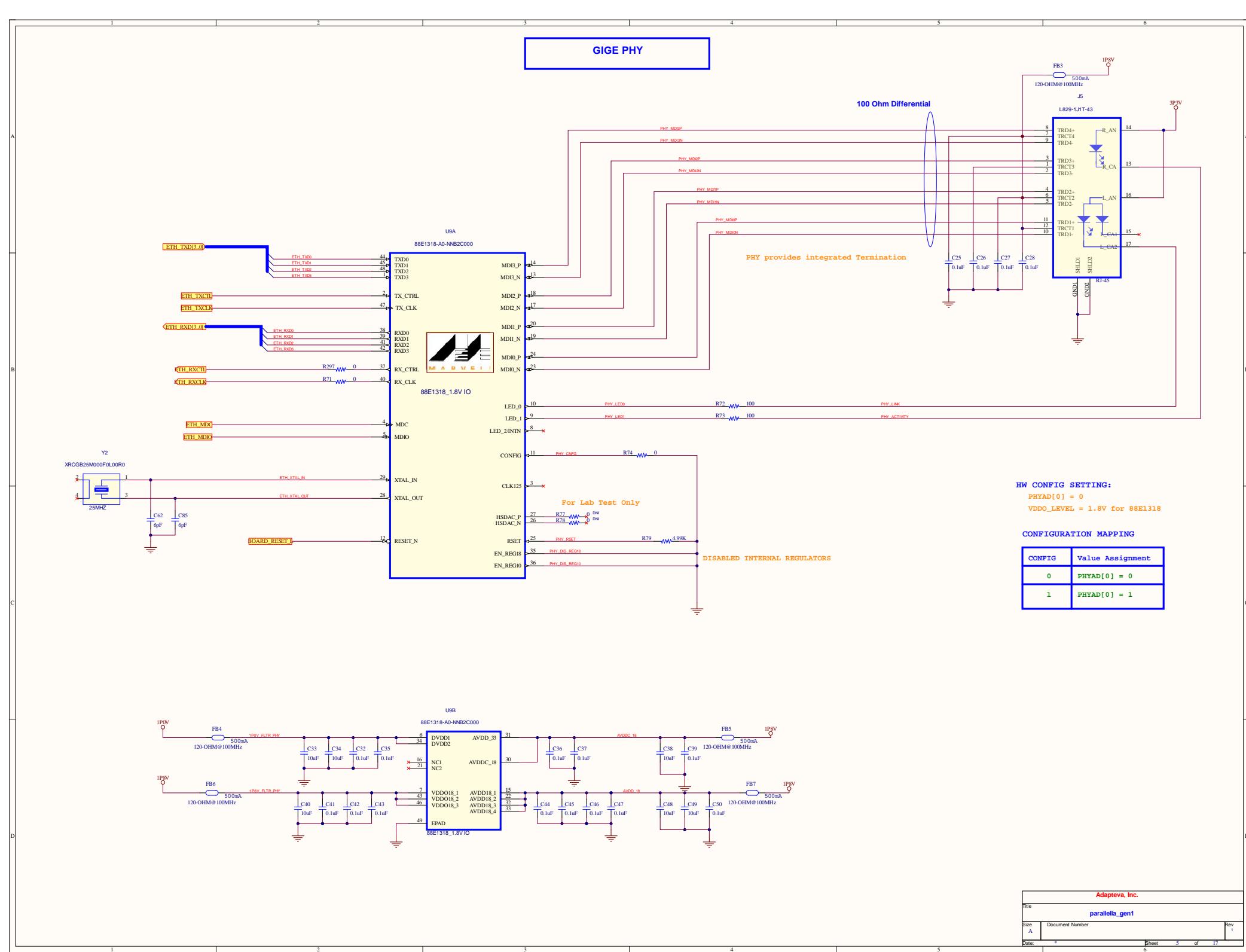
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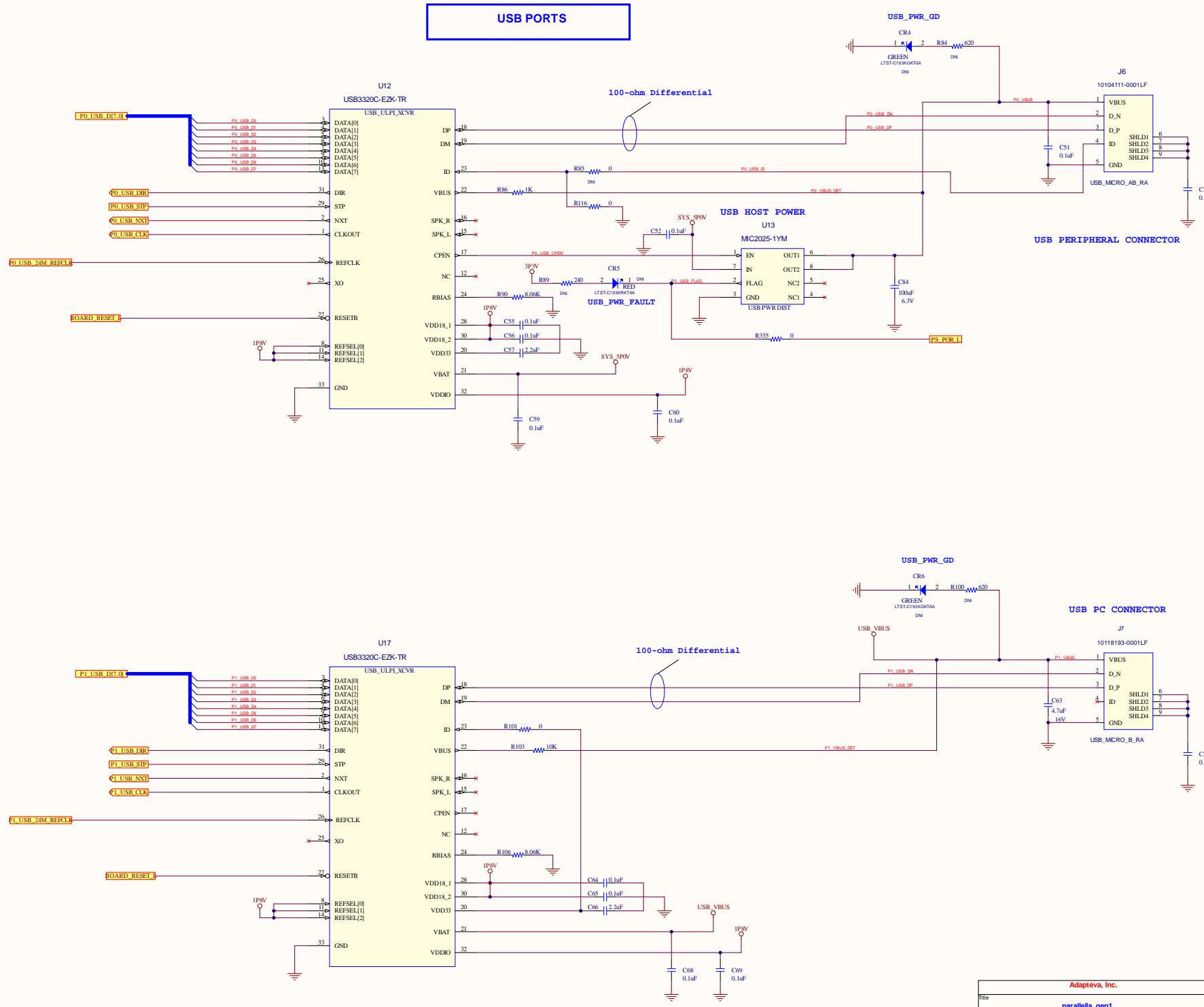




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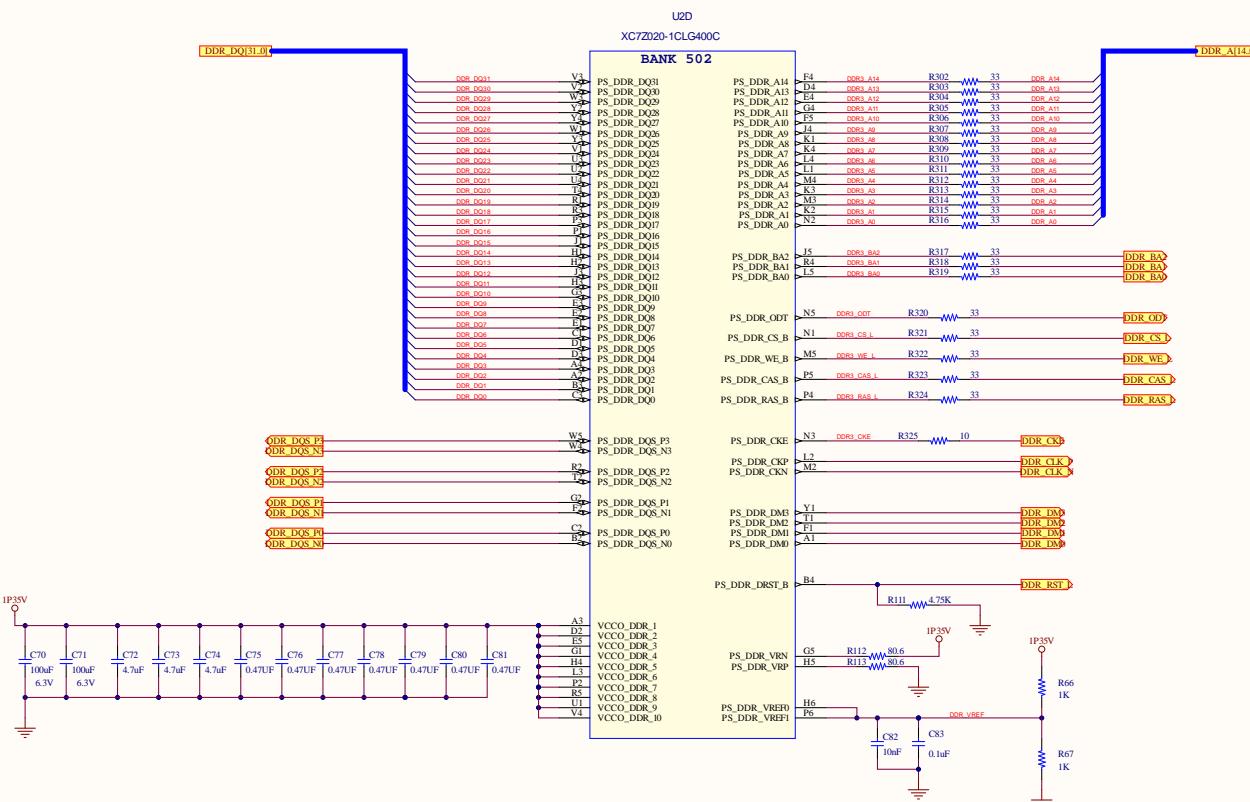




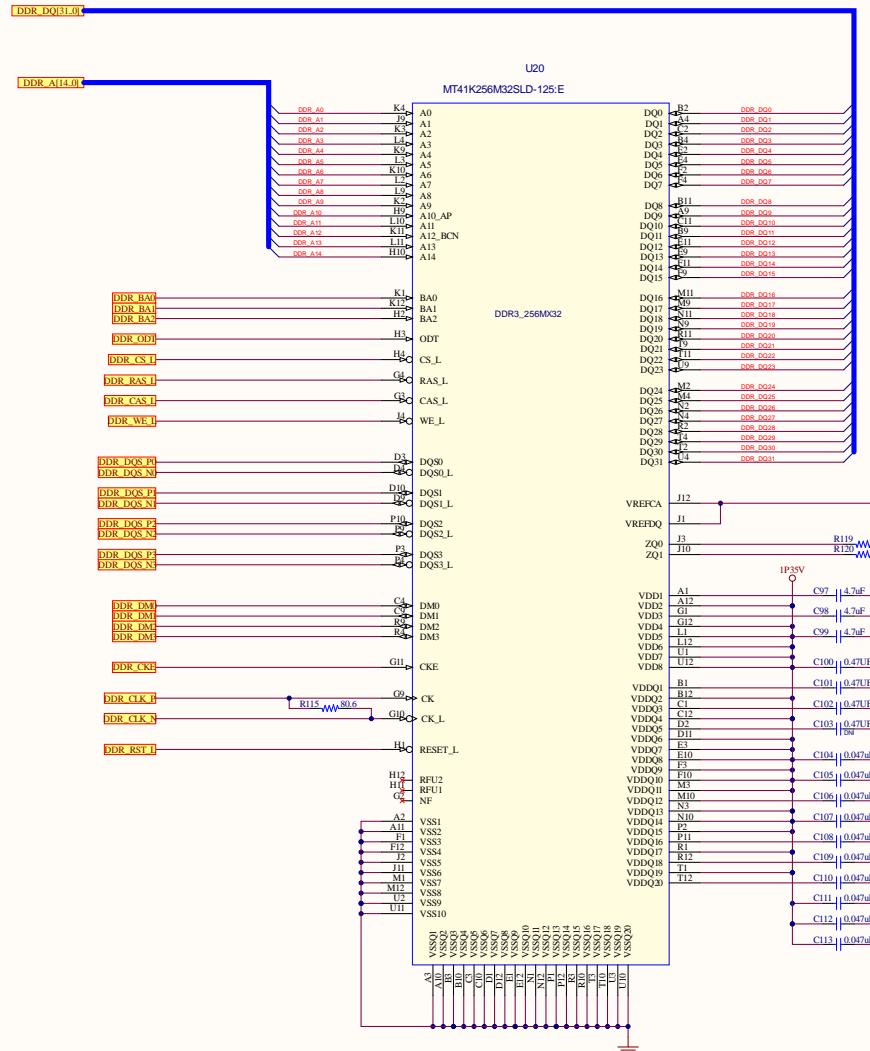


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ZYNQ BANK 502

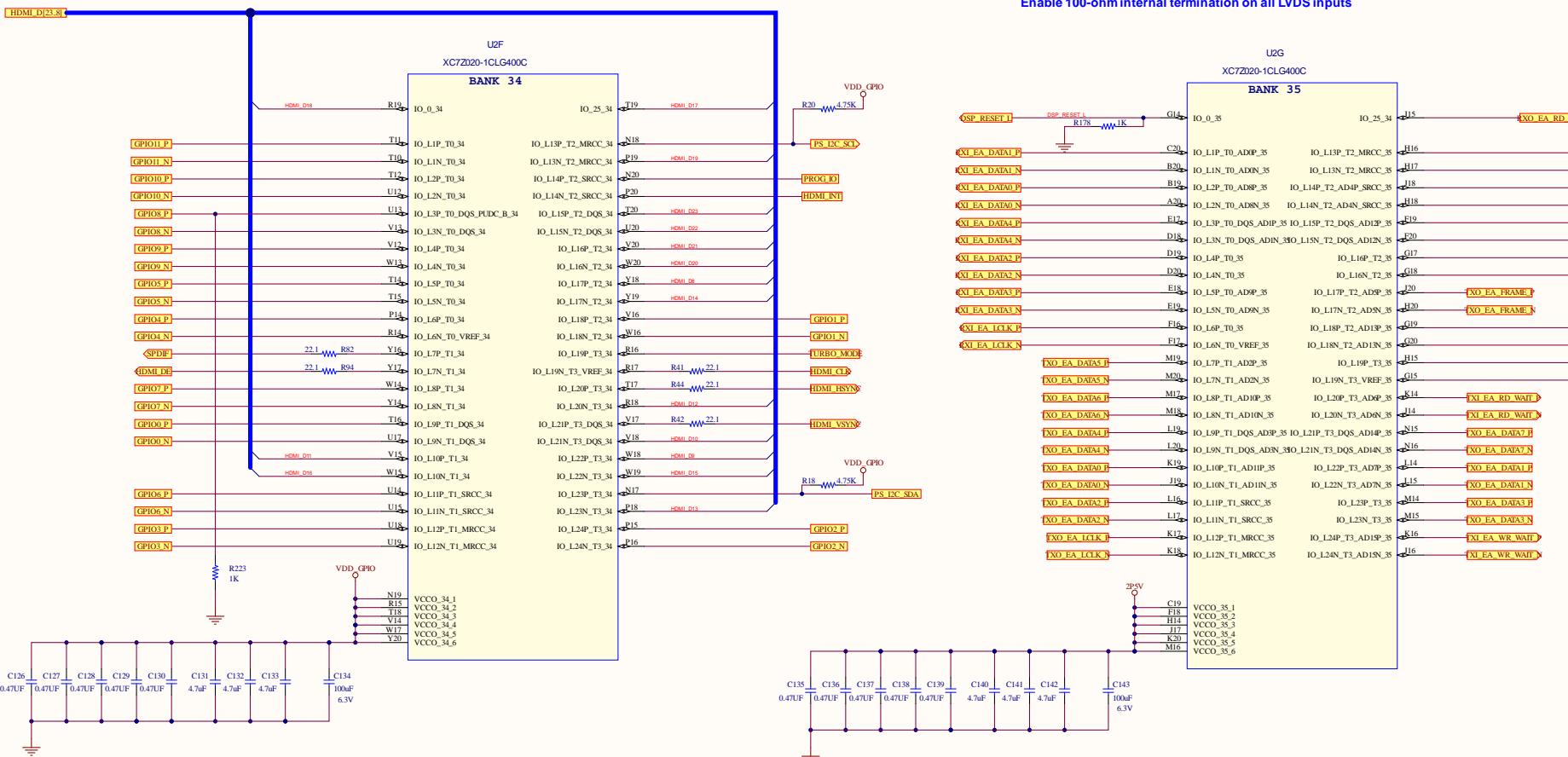


DDR3 - 256M X 32



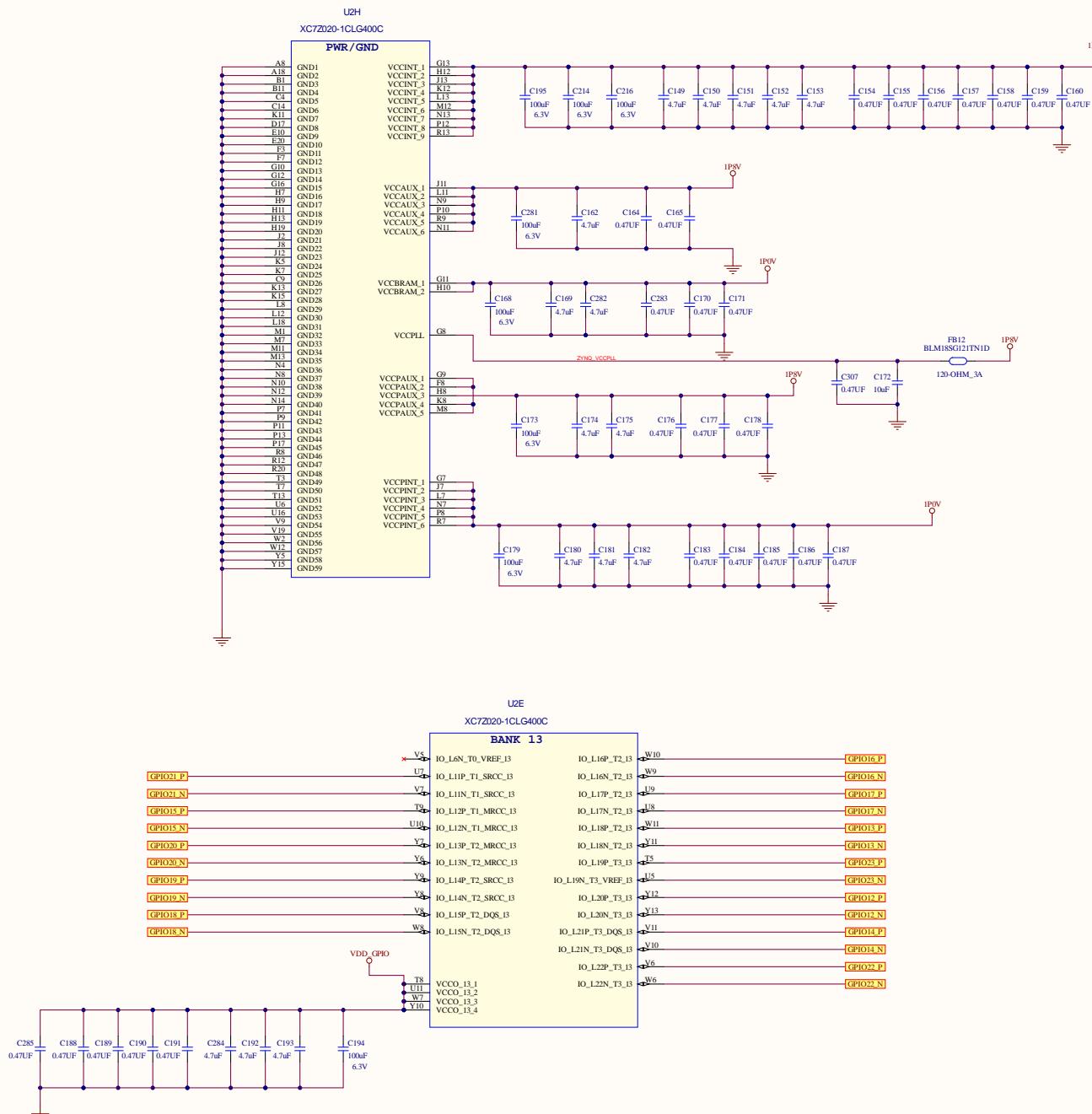
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BANKS 34 & 35

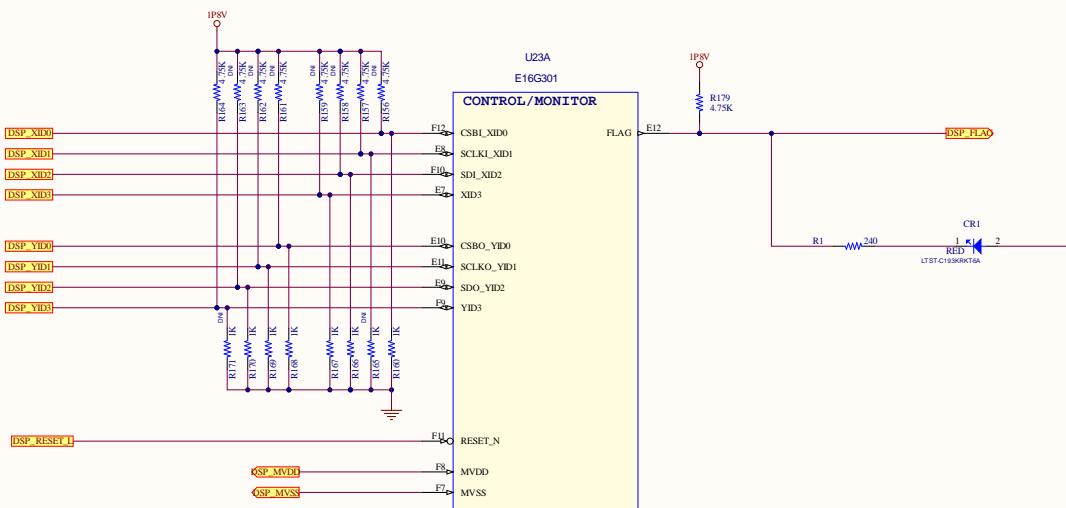


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ZYNQ POWER & GROUND



DSP PROCESSOR 1-OF-3

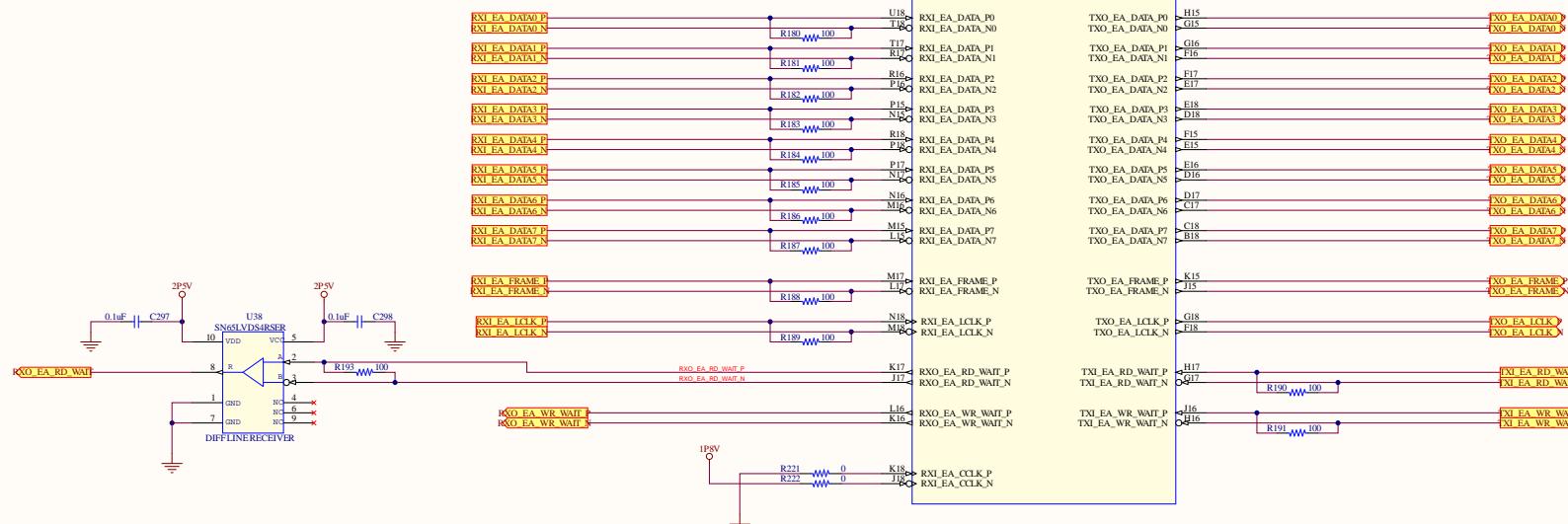


100 Ohm Differential LVDS Signals

E16G301

eLINK - EAST

100 Ohm Differential LVDS Signals



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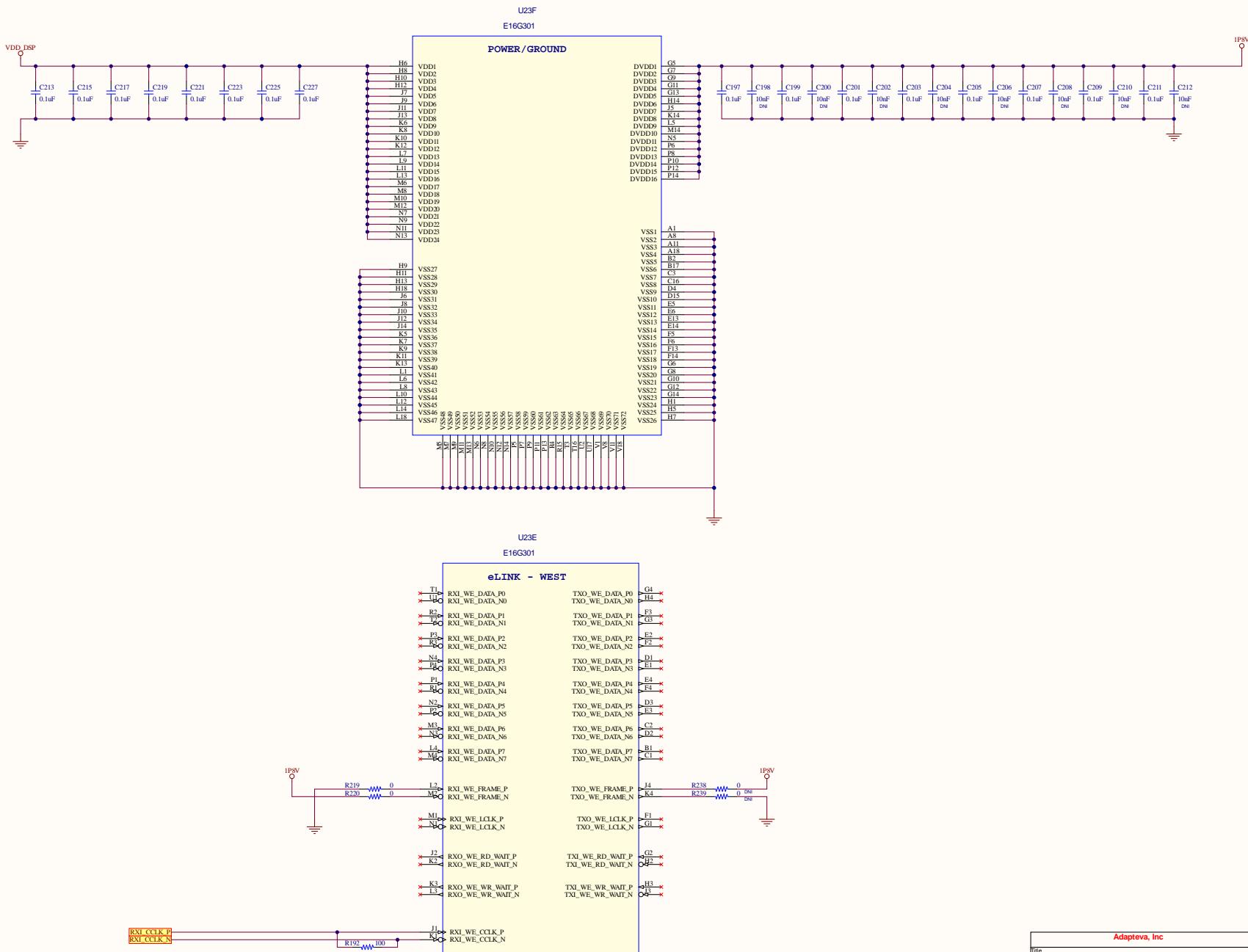
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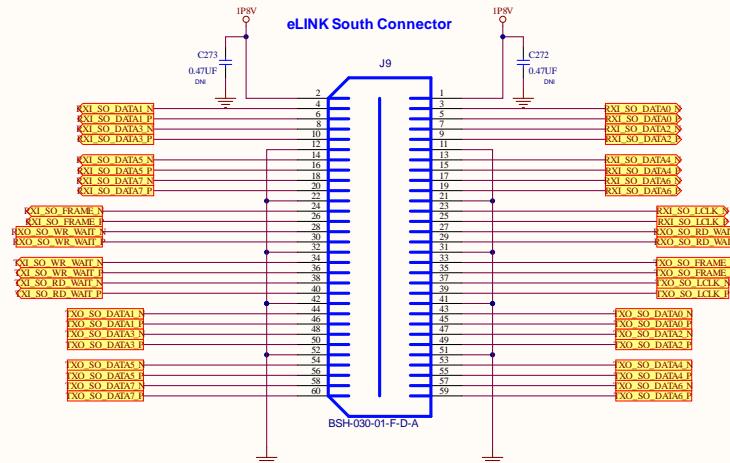
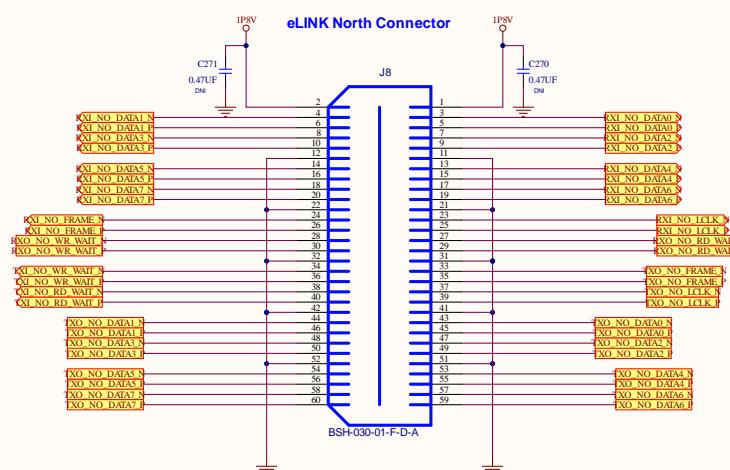


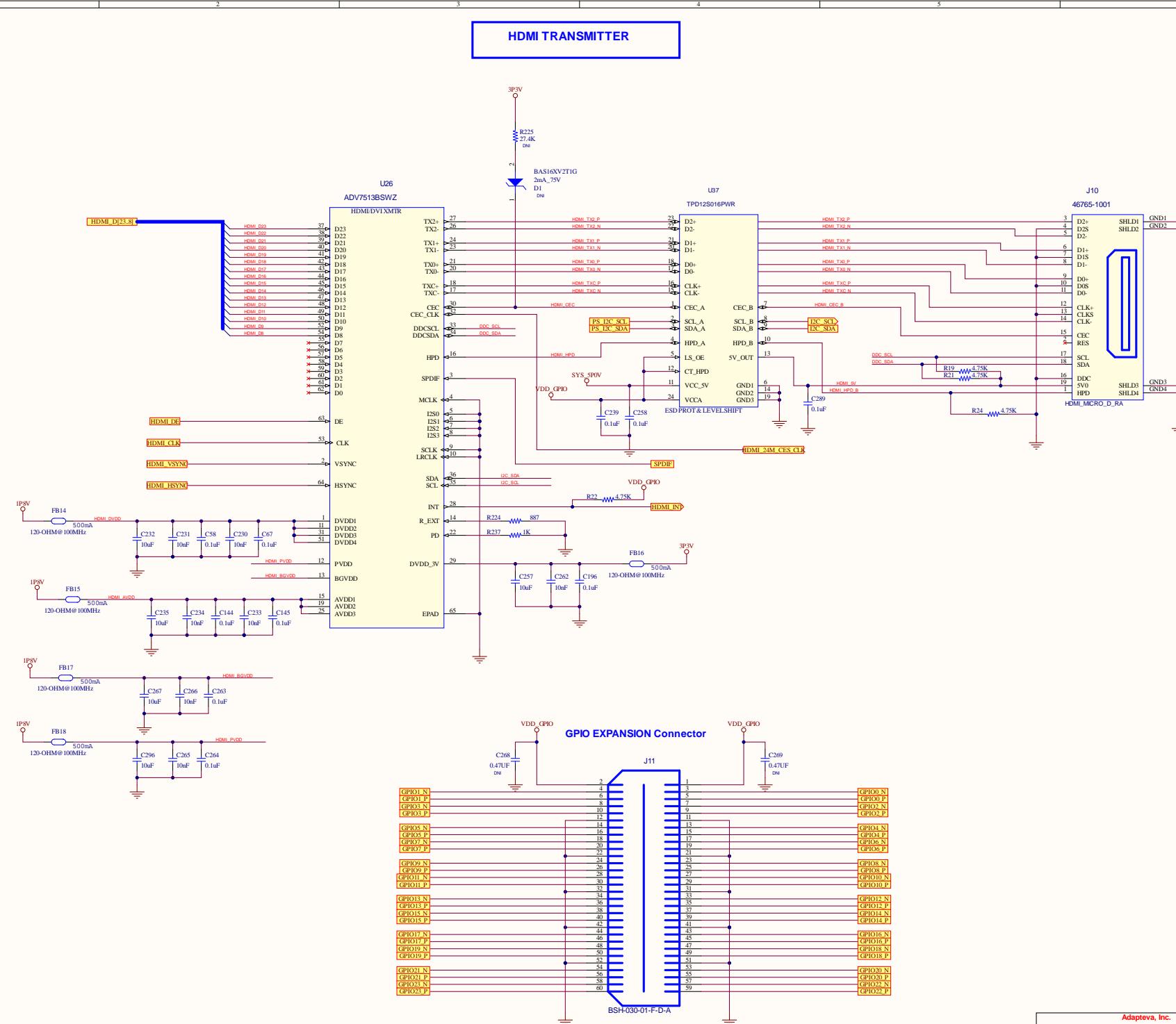
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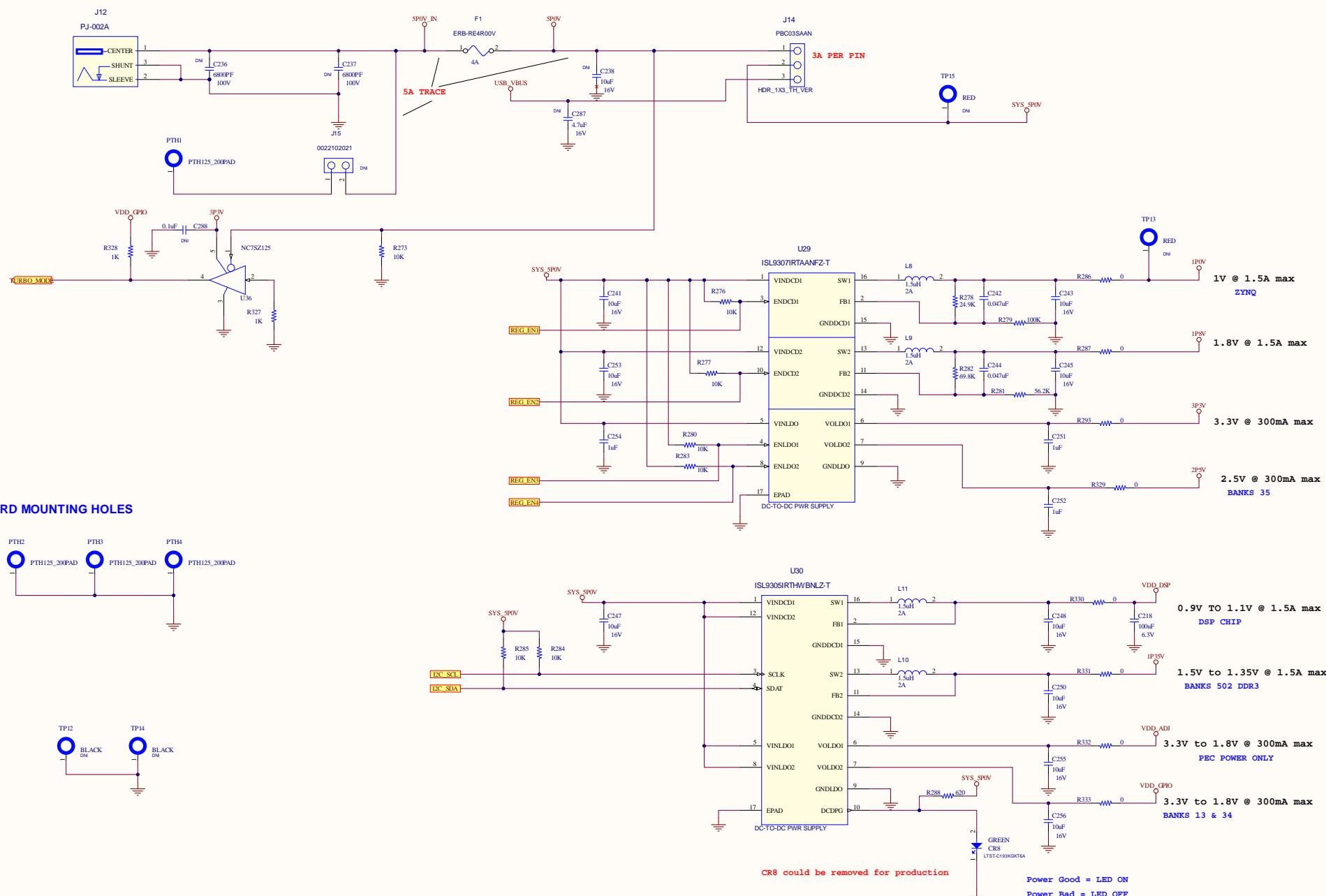
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DSP eLINK CONNECTORS



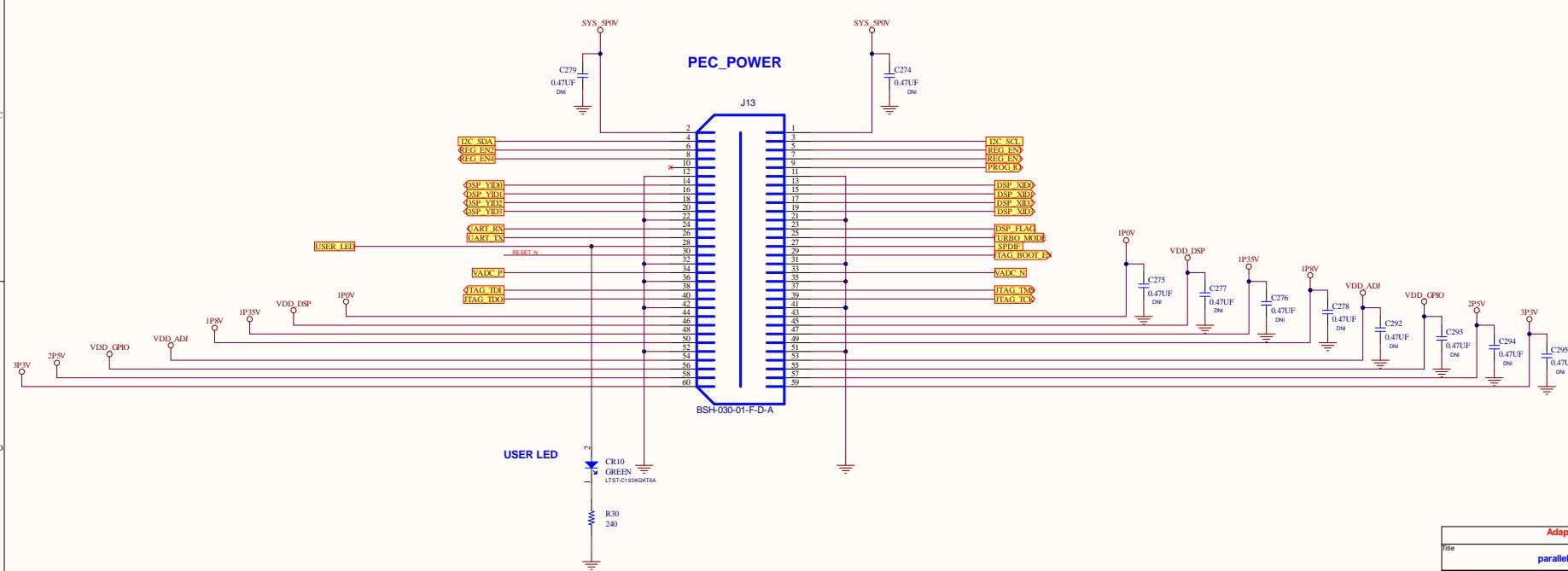
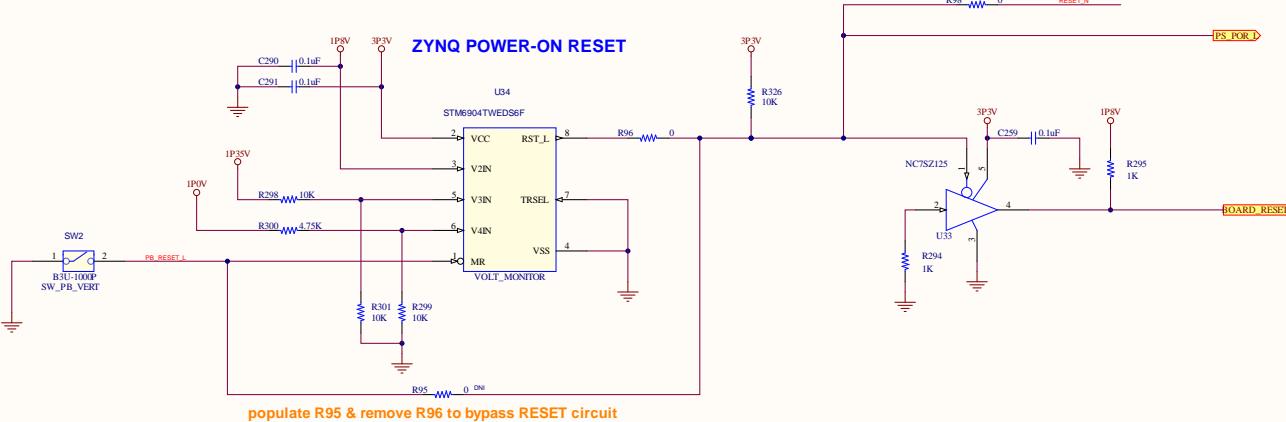


POWER MANAGEMENT



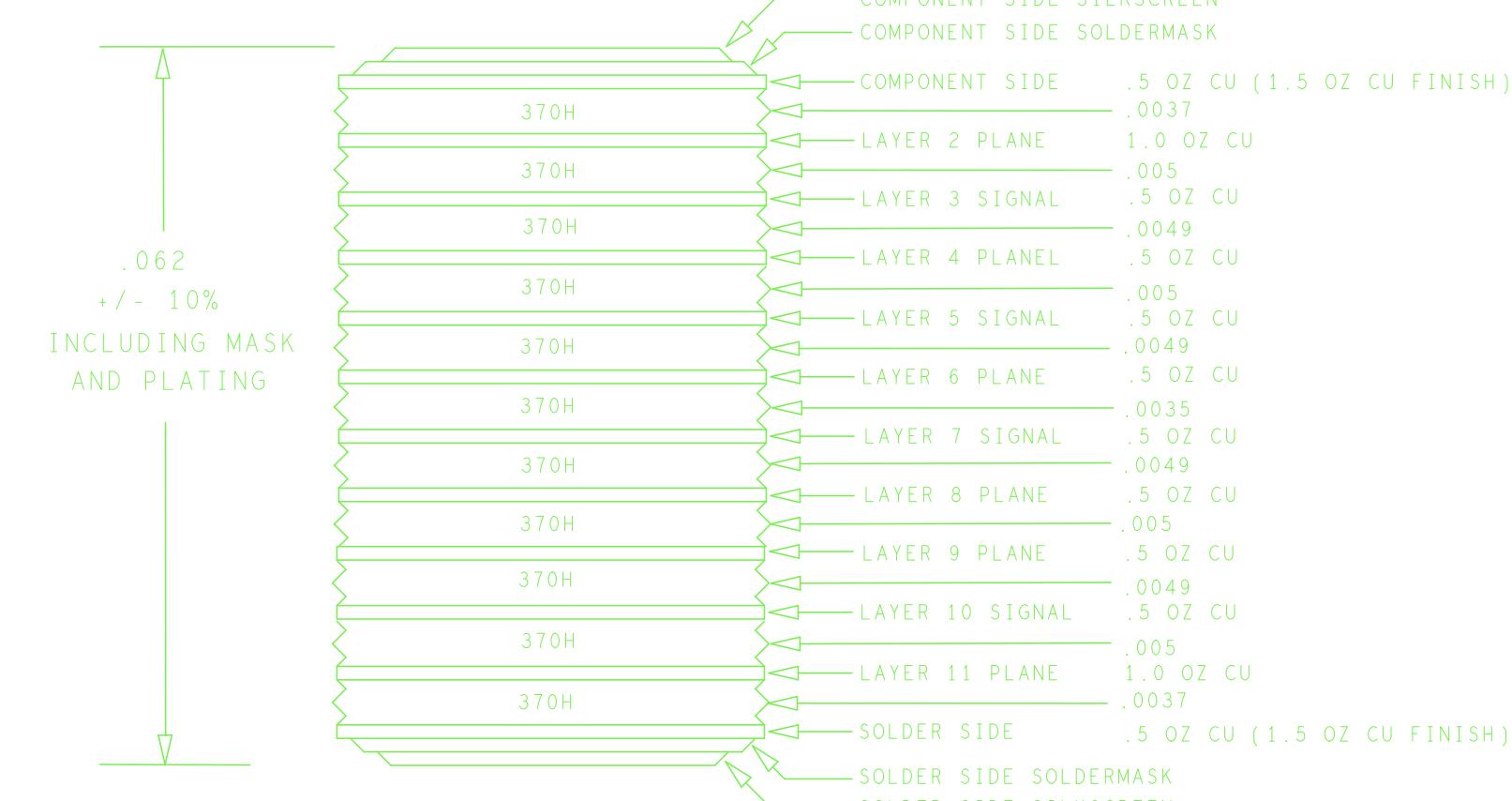
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Size A	Document Number	Rev 1
Date	Page	Sheet 16 of 17

RESET GENERATION



8 7 6 5 4 3 2 1

LTR	DESCRIPTION	DATE	APPROVED



NOTES:

1. LATEST VERSION OF ALL REFERENCED SPECIFICATIONS TO BE USED UNLESS OTHERWISE SPECIFIED.
2. FABRICATE IN ACCORDANCE WITH IPC-A-600, CLASS 2 UNLESS OTHERWISE SPECIFIED.
3. INSPECT IN ACCORDANCE WITH IPC-6012, CLASS 2, UNLESS OTHERWISE SPECIFIED.
4. MATERIAL: FR4 370H
FINISHED BOARD MUST MEET UL94V-0. THICKNESS TO BE .062" - SEE LAYER DETAIL.
5. PLATED THRU HOLES TO HAVE COPPER WALL THICKNESS NOT LESS THAN 0.002". THICKNESS TO BE DETERMINED BY IPC-6012, CLASS 2.
6. SILKSCREEN NOMENCLATURE TO BE WHITE NON-CONDUCTIVE INK AND NOT COVER ANY PORTION OF A COMPONENT PAD. FABRICATOR TO CLIP ANY NON-CONFORMING SILKSCREEN NOMENCLATURE.
7. UL LOGO, DATE CODE AND VENDOR CODE MUST APPEAR IN ETCH ON PRIMARY SIDE. SECONDARY SIDE IS ACCEPTABLE IF THERE IS NO ROOM ON PRIMARY SIDE.
8. USE LPI SOLDER MASK OVER BARE COPPER PER SUPPLIED ARTWORK PER IPC-SM-840, CLASS 2, COLOR - BLUE FINISH - ENIG.
9. SOLDER MASK SHALL BE CAPABLE OF FIVE SOLDER EXPOSURES AT 500 DEGREES F.

10. TOOLING HOLES MUST BE PRIMARY DRILLED AT THE SAME TIME AS PLATED-THRU HOLES. ALL HOLES MUST BE WITHIN .003" OF RADIAL TRUE POSITION.

11. DIMENSIONAL TOLERANCES ON THE PCB ARE AS FOLLOWS UNLESS OTHERWISE SPECIFIED:

HOLE TO HOLE +/- .005"
HOLE TO EDGE +/- .010"
EDGE TO EDGE +/- .010"

12. PADS MUST BE FINISHED TO WITHIN +/- .0015" OF THE MINOR DIMENSION (PAD WIDTH) & +/- .002" OF THE MAJOR DIMENSION (PAD LENGTH)

13. FINISH: IMMERSION GOLD COATING (2-7 MICRO-INCHES) OVER NICKEL (MINIMUM 100 MICRO-INCHES) PER IPC-4552.

14. GLOBAL AND LOCAL FIDUCIALS MUST BE FREE OF ANY MARKINGS.

15. REMOVAL ON NON-FUNCTIONAL PADS ON INNER LAYERS ALLOWED.

16. THEIVING OF OUTER LAYERS IS ACCEPTABLE AS LONG AS THE COPPER IS KEPT A MINIMUM OF .200" FROM ANY DESIGN FEATURE UNLESS OTHERWISE SPECIFIED.

17. ELECTRICAL TEST: FINISHED PCB TO BE SUBJECT TO 100% CONTINUITY AND ISOLATION ELECTRICAL TEST AT 100V MINIMUM. TEST FIXTURES TO BE GENERATED FROM IPC-D-356 FORMATTED NET LIST DATA CROSS-REFERENCED TO GERBER EXTRACTED NET LIST DATA.

18. PRIOR TO BOARD FABRICATION, COMPARE GERBER DATA TO SUPPLIED IPC-D-356 NETLIST. REPORT ALL DISCREPANCIES.

19. IMPEDANCE: MINOR MODIFICATION TO ARTWORK ALLOWED TO MEET IMPEDANCE REQUIREMENTS

5.25 MIL LINES ON LAYER 1 AND 12 TO YEILD 50 OHMS +/- 10%.

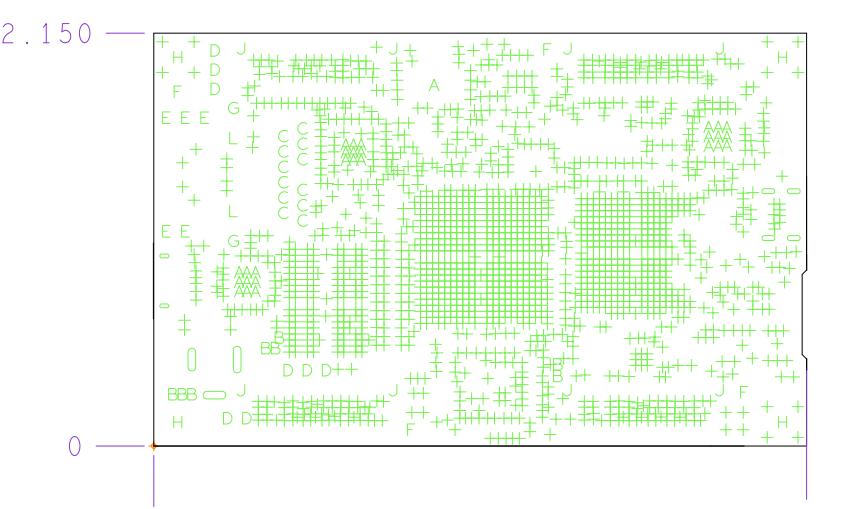
3.75 MIL LINES WITH 8.25 MIL SPACE TO YEILD 100 OHMS DIFFERENTIAL +/- 10% ON LAYERS 3, 5, 8 AND 10.
4.25 MIL LINE ON LAYER 3, 5, 8 AND 10 TO YEILD 50 OHMS +/- 10 %.

20. DIMENSIONS: VENDOR TO USE SUPPLIED FILM FILE "BOARD_OUTLINE.ART" FOR MISSING DIMENSIONS. IF DISCREPENCIES EXIST BETWEEN "BOARD_OUTLINE.ART" AND FAB DWG. "BOARD_OUTLINE.ART" TAKE PRECEDENCE.

21. VIA PLUGGING: VENDOR TO PLUG ALL VIAS .012 INCHES AND SMALLER USING NON-CONDUCTIVE EPOXY AND OVERPLATE WITH COPPER, .0005 INCHES MINIMUM, PRIOR TO APPLICATION OF SOLDERMASK.

22. TEARDROPS: TEARDROPS MAY BE ADDED BY VENDOR TO IMPROVE MANUFACTURING.

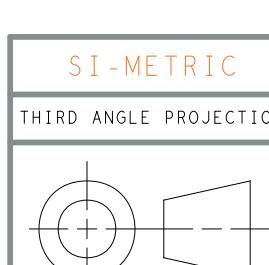
LAYER DETAIL



DRILL CHART: TOP to BOTTOM ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
+	10.0	+0.0/-10.0	PLATED	1810
A	12.0	+0.0/-12.0	PLATED	28
B	20.0	+3.0/-3.0	PLATED	8
C	35.0	+3.0/-3.0	PLATED	12
D	40.0	+3.0/-3.0	PLATED	8
E	50.0	+3.0/-3.0	PLATED	5
F	55.0	+3.0/-3.0	PLATED	4
G	62.0	+3.0/-3.0	PLATED	2
H	125.0	+5.0/-0.0	PLATED	4
J	40.0	+3.0/-3.0	NON-PLATED	8
L	128.0	+5.0/-5.0	NON-PLATED	2
M	47.24x19.69	+3.0/-3.0	PLATED	2
N	66.93x25.59	+3.0/-3.0	PLATED	4
P	118.11x39.37	+3.0/-3.0	PLATED	1
Q	118.11x39.37	+3.0/-3.0	PLATED	1
R	137.8x39.37	+3.0/-3.0	PLATED	1

MAY BE DRILLED AT .020"

COMPONENT SIDE SHOWN



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:	DECIMALS XX .03 XXX .010	ANGLES ±0° 30'
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS TOLERANCES ARE:	DECIMALS X.X .15 X.XX .125	ANGLES 10° 30'

NOTES: UNLESS OTHERWISE SPECIFIED DIMENSIONS AND TOLERANCING PER ANSI Y14.5M DRAWING SYSTEM PER FIGURE 2 REMOVE ALL BURRS BROACHES, 0.005 TO 0.10 ALL MACHINED SURFACES
THREADS PER ANSI Y14.5M ALL THD LENGTHS ARE MIN FULL THD COUNTERSINK INTERNAL THD 90° TO MAJOR DIA CHAMFER INTERNAL THD 45° TO MINOR DIA MACHINED FILLET RADIUS 0.013 TO 0.015
NOTES: UNLESS OTHERWISE SPECIFIED DIMENSIONS AND TOLERANCING PER ANSI Y14.5M DRAWING SYSTEM PER FIGURE 2 REMOVE ALL BURRS BROACHES, 0.005 TO 0.10 ALL MACHINED SURFACES

MATERIAL:
FINISH:
NOTE: ALL HOLE SIZES ARE AFTER PLATING

1

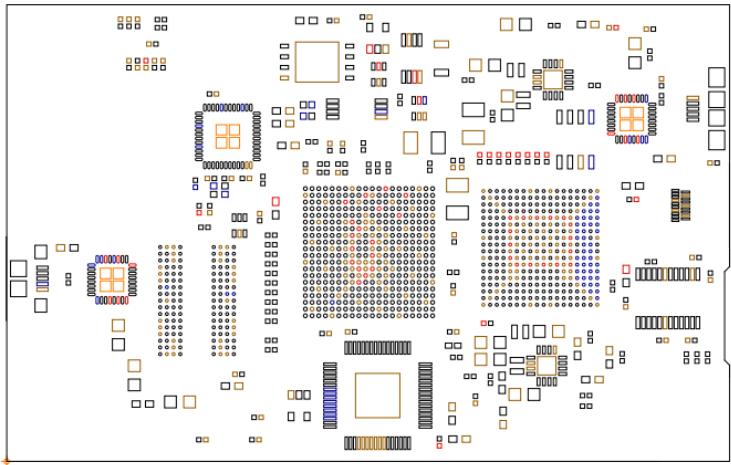
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DRAWN BDS	12/31/13
CHKD	
DESIGN	
ENG	
APPROVED	

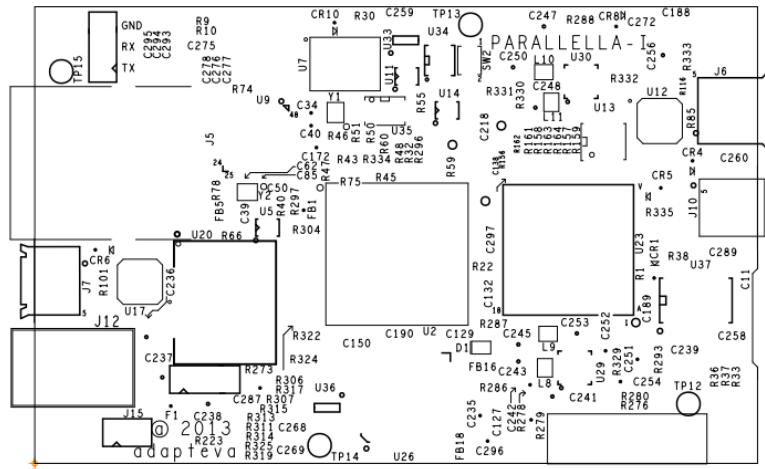
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XXXXXXXXXXXX
XXXXXXXXXXXX
TEL: XXXXXXXXXX

FAB DRAWING
PARALLELLA-I BOARD
SIZE DRAWING NO.
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SCALE NONE DR CODE NONE SHEET 1 OF 1



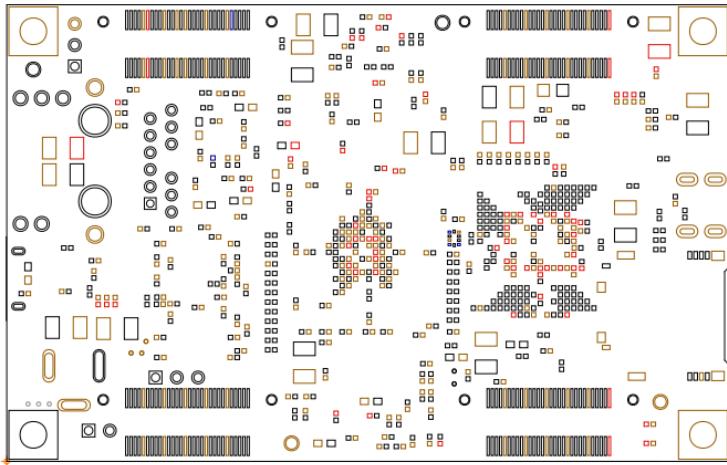
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	LAYER: SOLDER PASTE TOP
	DWG NO: PARALLELLA-I REV: D DATE: 2013.12.31

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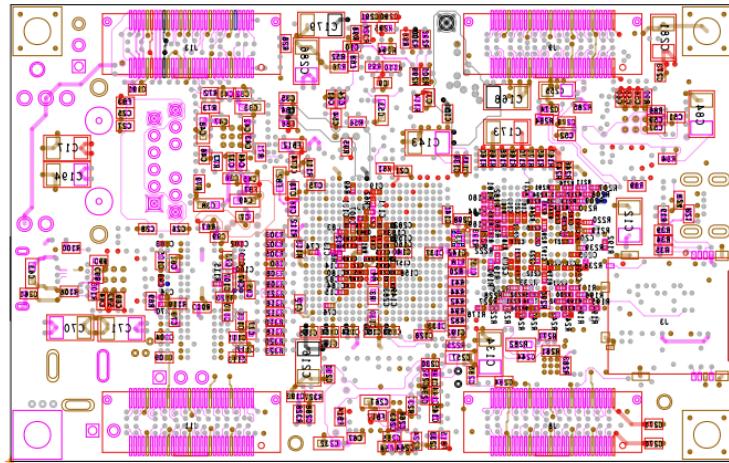


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	LAYER:	SILK SCREEN TOP	
	DWG NO:	REV: D	DATE: 2013.12.31

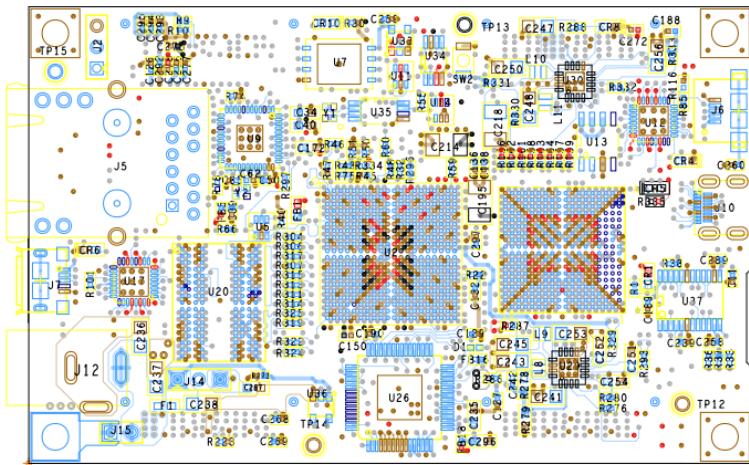
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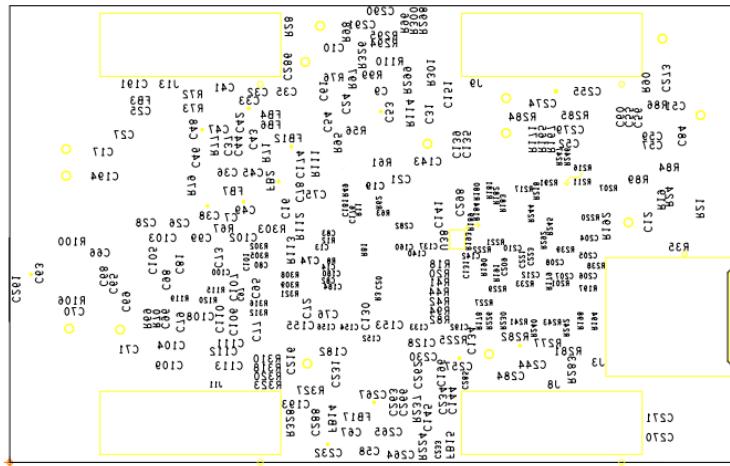
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	DWG NO: PARALLELLA-I REV: D DATE: 2013.12.31



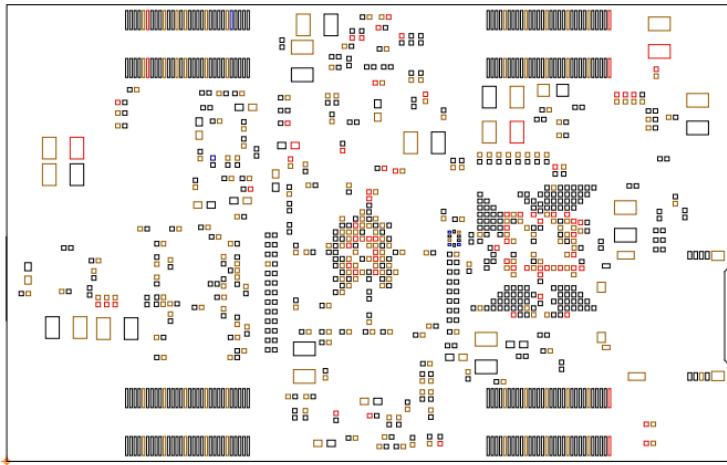
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LAYER: LAYER 12 SOLDER SIDE	
DWG NO: PARALLELLA-I	REV: D DATE: 2013.12.31



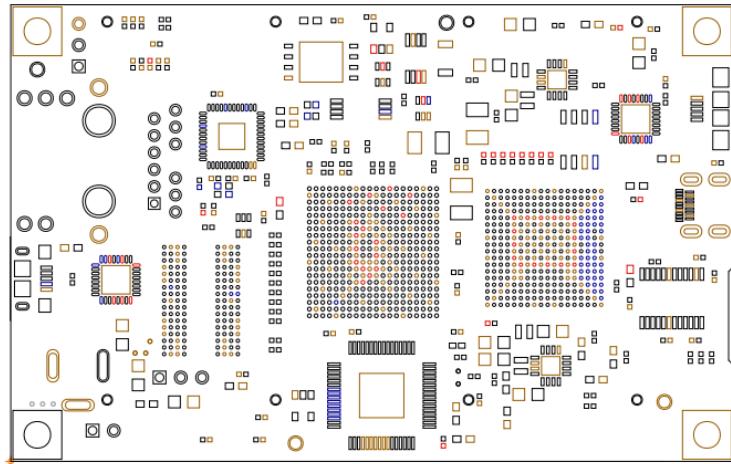
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DRAWN BY:	BDS		
LAYER:	LAYER 1 PRIMARY SIDE		
DWG NO:	PARALLELLA-I	REV: D	DATE: 2013.12.31



PROJECT:		PARALLELLA-I BOARD	
DRAWN BY:		BDS	
LAYER:		STICK SCREEN BOTTOM	
DWG NO:	REV:		DATE:
ADAPTEVA	D		2013.12.31
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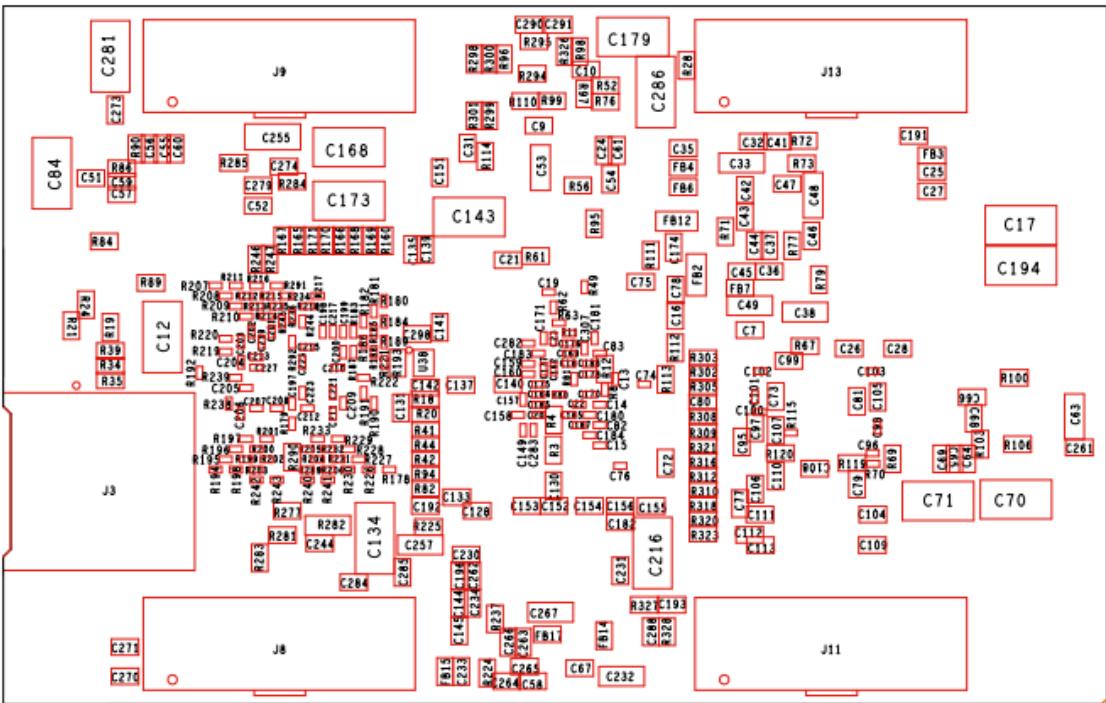


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	LAYER: SOLDER PASTE BOTTOM
	DWG NO: PARALLELLA-I REV: D DATE: 2013.12.31



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	DRAWN BY: BDS
	LAYER: SOLDER MASK TOP
	DWG NO: PARALLELLA-I REV: D DATE: 2013.12.31

ART FILM - assy_bottom



ART FILM - assy_bottom

8

7

6

5

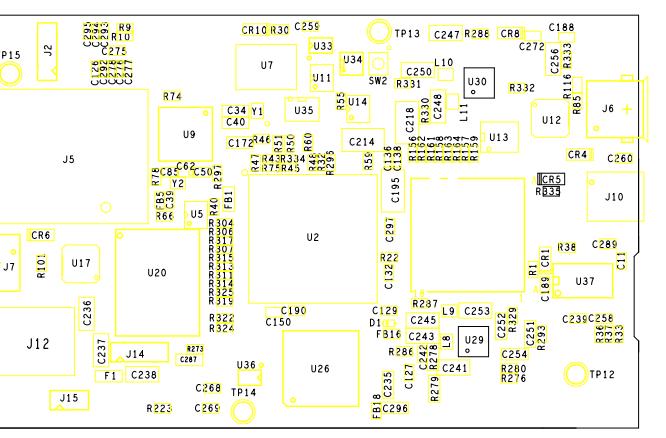
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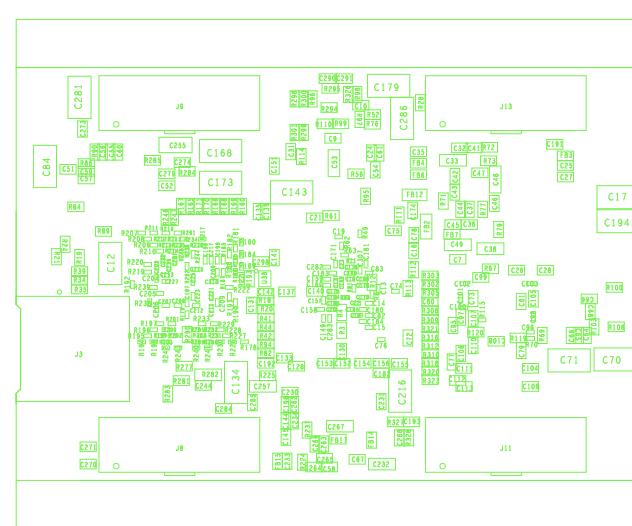
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1

LTR	DESCRIPTION	DATE	APPROVED



VIEWED FROM COMPONENT SIDE



VIEWED FROM SOLDER SIDE

NOTES:

1. WORKMANSHIP TO CONFORM TO IPC-A-610 CLASS 2.
2. FOLLOW SILKSCREEN OUTLINE FOR COMPONENT ORIENTATION.

SI-METRIC THIRD ANGLE PROJECTION	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:		NOTES: UNLESS OTHERWISE SPECIFIED DIMENSIONS AND TOLERANCING PER ANSI Y14.5M MOLD SYSTEM PER Y14.5M REMOVE ALL BURRS BROACHES .005 TO .010 ALL MACHINED SURFACES 125% ALL MACHINED SURFACES		MATERIAL:
	DECIMALS	ANGLES	XX .03	±0° 30'	
	XXX .010				

SI-METRIC THIRD ANGLE PROJECTION	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS TOLERANCES ARE:		NOTES: UNLESS OTHERWISE SPECIFIED DIMENSIONS AND TOLERANCING PER ANSI Y14.5M MOLD SYSTEM PER Y14.5M REMOVE ALL BURRS BROACHES .013 TO .025 ALL MACHINED SURFACES		FINISH:
	DECIMALS	ANGLES	X.X .15	10° 30'	
	XXX .125				

APPROVALS	DATE
DRAWN BDS	12/31/13
CHKD	
DESIGN	
ENG	
APPROVED	

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NEXT ASSY USED ON
FIRST APPLICATION
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ADAPTEVA
XXXXXXXXXXXX
XXXXXXXXXXXX
TEL: XXXXXXXXXX

ASSEMBLY DRAWING
PARALLELLA-I BOARD

SIZE	DRAWING NO.	REV
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SCALE	DR. CODE	NONE
NONE		
SHEET 1 OF 1		

8

7

6

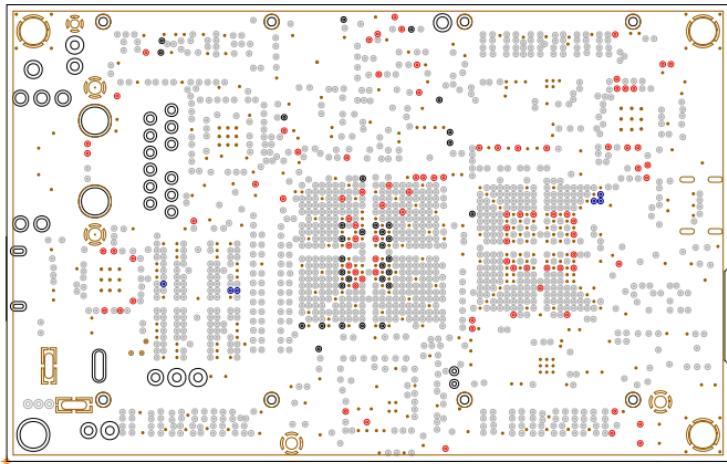
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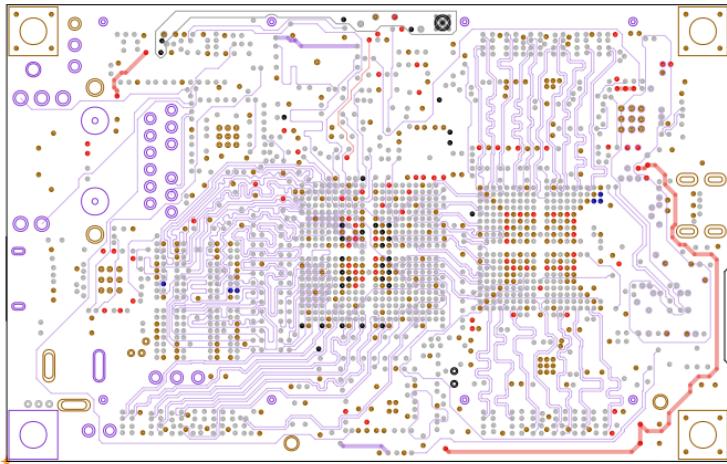
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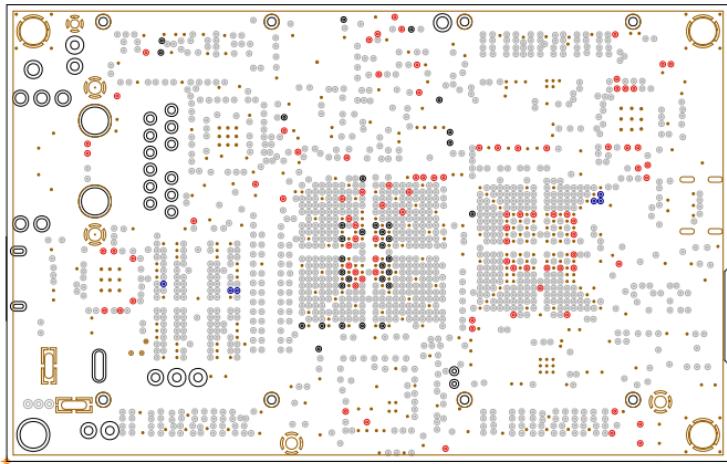
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ADAPTEVA XXXXXXXXXXXX	PROJECT: PARALLELLA-I BOARD
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	LAYER: LAYER 2 GROUND PLANE
	DWG NO: PARALLELLA-I REV: D DATE: 2013.12.31



ADAPTEVA XXXXXXXXXXXX	PROJECT: PARALLELLA-I BOARD
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	LAYER: LAYER 3 SIGNAL
	DWG NO: PARALLELLA-I
	REV: D DATE: 2013.12.31

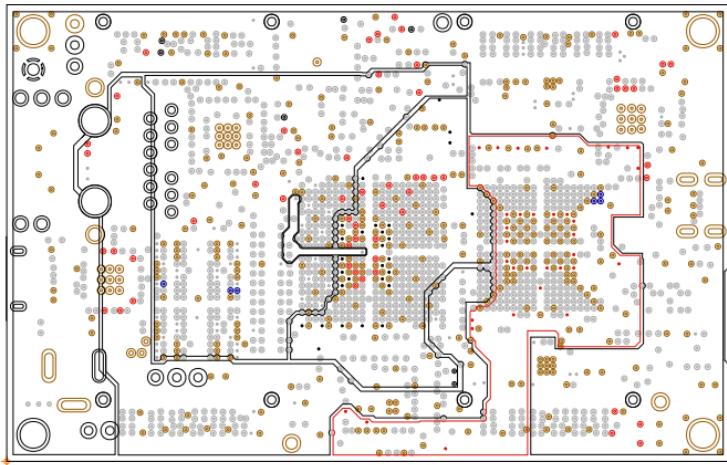


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	DRAWN BY: BDS
	LAYER: LAYER 4 GND
DWG NO: PARALLELLA-I	REV: D DATE: 2013.12.31



ADAPTEVA XXXXXXXXXXXX	PROJECT: PARALLELLA-I BOARD
	DRAWN BY: BDS
	LAYER: LAYER 5 SIGNAL
	DWG NO: PARALLELLA-I

REV: D	DATE: 2013.12.31
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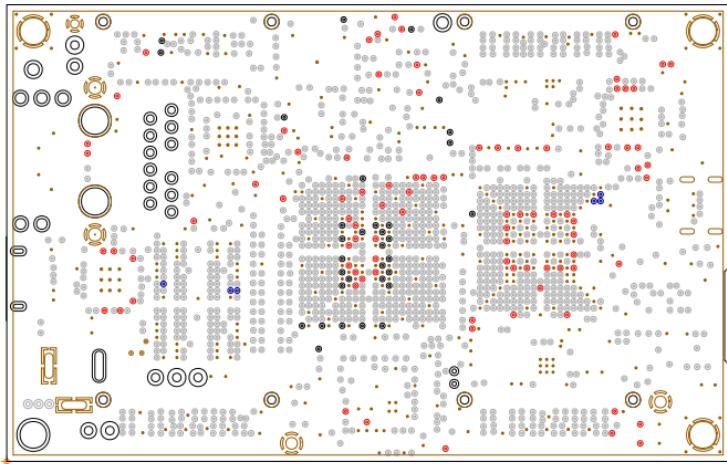
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	LAYER: LAYER 6 PWR
DWG NO: PARALLELLA-I	REV: D DATE: 2013.12.31



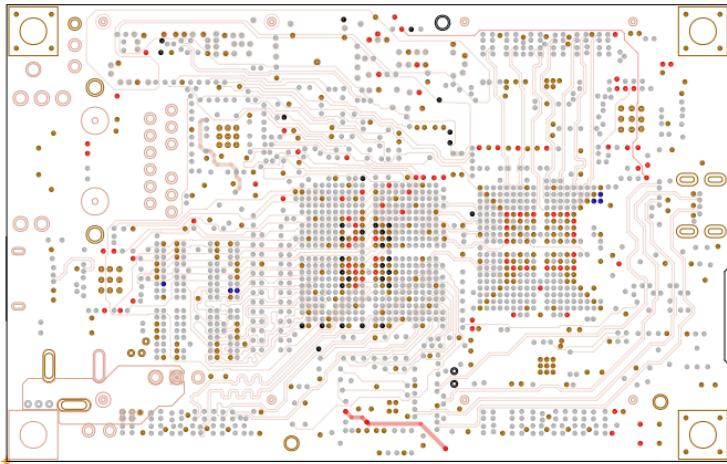
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	DRAWN BY: BDS
	LAYER: LAYER 9 PWR
	DWG NO: PARALLELLA-I REV: D DATE: 2013.12.31



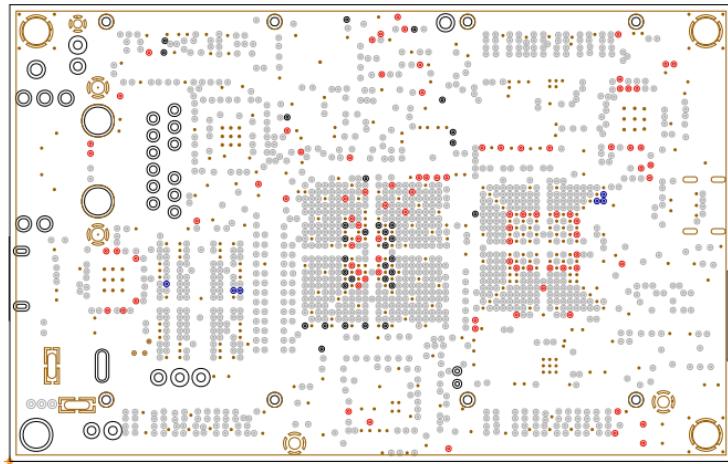
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	LAYER: LAYER 8 SIGNAL
	DWG NO: PARALLELLA-I REV: D DATE: 2013.12.31



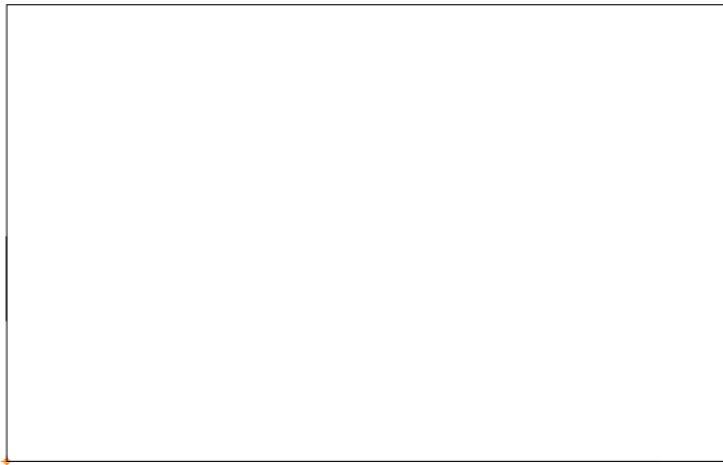
ADAPTEVA XXXXXXXXXXXX	PROJECT: PARALLELLA-I BOARD
	DRAWN BY: BDS
	LAYER: LAYER 9 GND
	DWG NO: PARALLELLA-I REV: D DATE: 2013.12.31



ADAPTEVA XXXXXXXXXXXX	PROJECT: PARALLELLA-I BOARD
	DRAWN BY: BDS
	LAYER: LAYER 10 SIGNAL
	DWG NO: PARALLELLA-I REV: D DATE: 2013.12.31



ADAPTEVA XXXXXXXXXXXX	PROJECT: PARALLELLA-I BOARD
	DRAWN BY: BDS
	LAYER: LAYER 11 GND PLANE
	DWG NO: PARALLELLA-I REV: D DATE: 2013.12.31



ADAPTEVA XXXXXXXXXXXX	PROJECT: PARALLELLA-I BOARD
	DRAWN BY: BDS
	LAYER: BOARD OUTLINE
DWG NO: PARALLELLA-I	REV: D DATE: 2013.12.31