Final Exam - CSc 137

(Include the Test question along with solution)

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1. What is the 16-bit FP number representation of 10.3 in hex with 1-bit sign, 4-bit biased exponent, and 11-bit fraction, where bias = 7? Please identify the key components of FP number representation (20 pts)

Step 1 Convert Decimal to Binary 10.3

Convert Integer: 10

* Successive division by 2*

2⌊10	2⌊5	2⌊2	2⌊1
5	2	1	0
-10	-4	-2	-0
0	1	0	1

$10_{(10)} = 1010_{(2)}$

Convert Fractional: 0.3

* Successive multiplication of remaining products*

$0.3 \times 2 = 0 + 0.6$
$0.6 \times 2 = 1 + 0.2$
$0.2 \times 2 = 0 + 0.4$
$0.4 \times 2 = 0 + 0.8$
$0.6 \times 2 = 1 + 0.6$
$0.2 \times 2 = 1 + 0.2$
$0.2 \times 2 = 0 + 0.4$
$0.4 \times 2 = 0 + 0.8$

Repeated Pattern

Step 2 Converting Binary to Scientific Notation

$10.3_{(10)} = 0101.0100110011\ldots_{(2)}$

Convert $101.0100110011\ldots_{(2)}$ TO Sci. Notation

$101.0100110011\ldots_{(2)}$ —Scientific Notation→ $1.01010011001\ldots_{(2)} \times 2^2$

Step 3 Add Biased Exponent: 1.01010011001...

Biased Offset : 7

Biased Exponent = $1.01010011001\ldots \times 2$

$3_{(10)} + 7_{(10)} = \boxed{10}_{(10)} \rightarrow 1010_{(2)}$ (Convert to Binary)

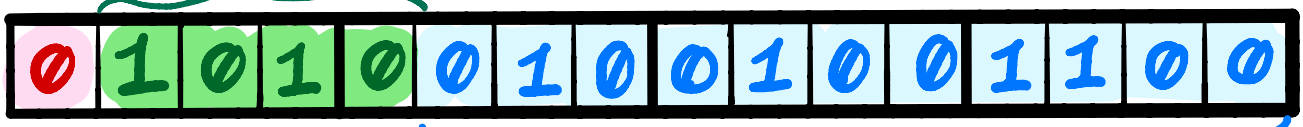
Step4| Fusion of Floating Point

Biased Component

$1.01010001100 \times 2^{10} = 1010_{(2)}$

Signed Component — Fractional Component

Biased Component



Signed Bit

Mantissa/Fraction

* When Signed component is positive set to 0(zero)
* When Signed component is negative set to 1

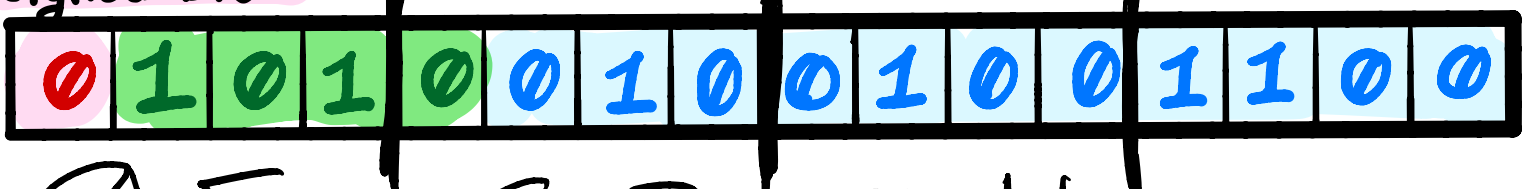
Convert to Hex - Final Step

Number	0	1	2	3	4	5	6	7
Binary	0000	0001	0010	0011	0100	0101	0110	0111
Hexadecimal	0	1	2	3	4	5	6	7

Number	8	9	10	11	12	13	14	15
Binary	1000	1001	1010	1011	1100	1101	1110	1111
Hexadecimal	8	9	A	B	C	D	E	F

Key components

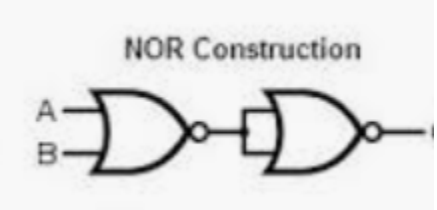
Signed Bit — Biased Exponent — Mantissa/Fraction



0x5 0x2 0x4 0xC

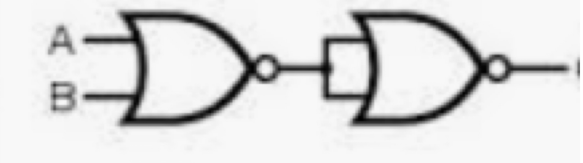
Decimal 10.3 in hex is 0x524C

2. Indicate which single logic gate is represented by the NOR gate construction below? (20 pts)
(Hint: Generate the truth table)

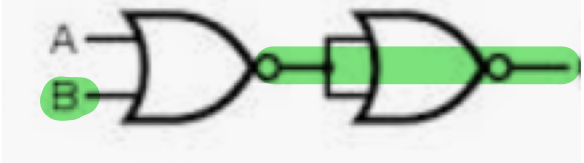


F

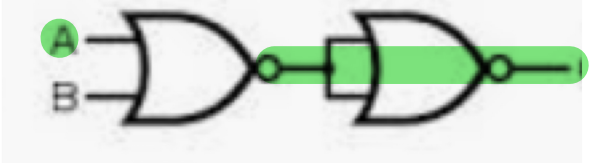
A=0 & B=0



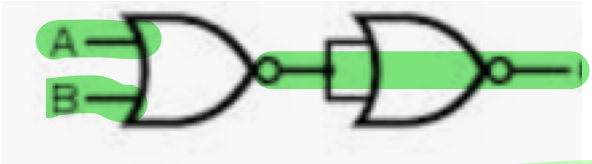
A=0 & B=1



A=1 & B=0



A=1 & B=1

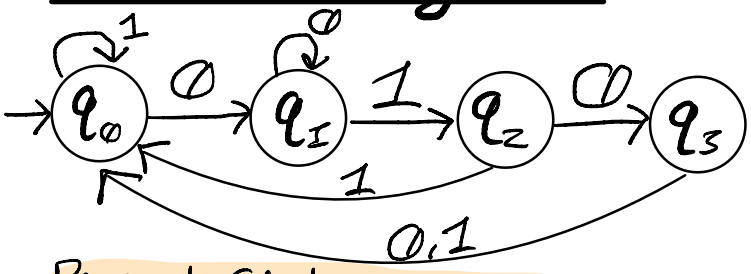


A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

∴ OR Gate

3. Design a Moore sequence recognizer that detects the Non-overlapping sequence "010". Use binary encoded state labels and design and draw the circuit schematic. (i.e. FSD, Next state generator Table (shows transition from current state to next state), Output Generator Table and schematic circuit. Please use output label as Y and input label as Z. Your inputs to D flip-flops will be D0 and D1. (20 pts)

State Diagram



Present State Table

Present State Q_0	Present State Q_1	Input X	Next State Q_0'	Next State Q_1'	Output y
0	0	0	0	1	0
0	0	1	0	0	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	1	1
1	0	1	0	0	0
1	1	0	0	0	0
1	1	1	0	0	0

Flip-Flops

D_0

S_1 \ $S_0 X$	00	01	11	10
0	1	0	0	1
1	1	0	0	0

$$D_0 = \bar{Q}_0\bar{x} + \bar{Q}_1\bar{x}$$

Distributive

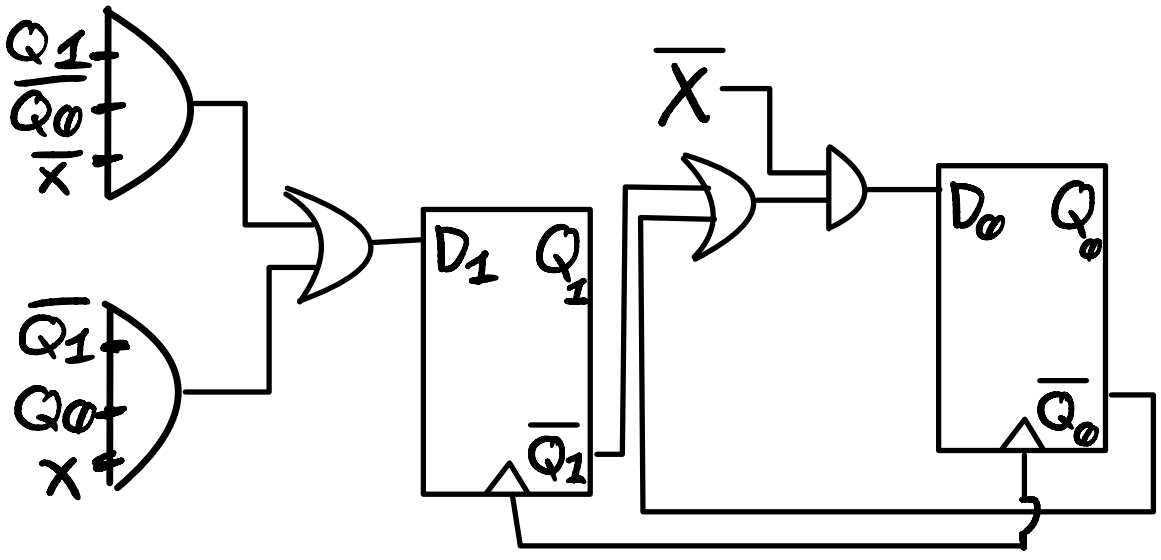
$$= \bar{x}(\bar{Q}_0 + Q_1)$$

D_1

S_1 \ $S_0 X$	00	01	11	10
0	0	0	1	0
1	1	0	0	0

$$D_1 = Q_1\bar{Q}_0\bar{x} + \bar{Q}_1 Q_0 x$$

Circuit Diagram



4. Consider a 8-bit data bus SDRAM. Given that the clock frequency of the bus is 400MHz, what is the peak memory bandwidth in megabyte per second (MBs)? (20 pts)

Clock Frequency
= 400MHz

With of Data Bus
= 8-Bit Data Bus = 1Byte = 8 Bits

Peak Memory Bandwidth
= Clock Frequency · With of Data Bus
= 400MHz · 1Byte
= 400 Megabytes per second

∴ 400 MBs

5. Computation is performed by a RISC ISA. A = B * (C + D). What is the value in R3 after the execution of code line #6: (M[B] = 10; M[C] = 5; M[D] = 15) ie: Code line # 6 has been completed. (20 pts)

R3 has a value of 20

RISC-ISA: Example of assembly program

```
#1. LD    R1,   (C)
#2. LD    R2,   (D)
#3. ADD   R3,   R1, R2
#4. LD    R4,   (B)
#5. MUL   R5,   R3, R4
#6. ST    (A),  R5
```

RISC-ISA: Example of assembly progra

```
#1. LD    R1,   (C)5
#2. LD    R2,   (D)15
#3. ADD   R3,20 R1, R2S,15
#4. LD    R4,   (B)10
#5. MUL   R5,   R3, R420,10
#6. ST    (A),  R5200
```

Line # 6 value 200 is stored in (A)