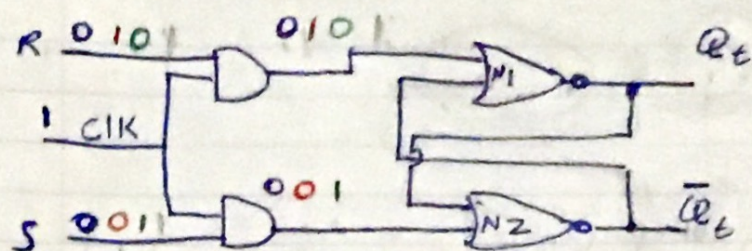


NOR

# S-R Flip-Flop with $\wedge$ Gates



CLK = Clock Signal

	S	R	$Q_t$	$Q_{t+1}$
1	0	0	$Q_t$	$Q_t$ ✓
2	0	1	0	0 ✓
3	1	0	1	1 ✓
4	1	1		Undesired

Case 1:  $S=0$ ;  $R=0$

$$Q_{t+1} = 0 + \overline{Q_t} = \overline{Q_t} = Q_t$$

$$\overline{Q_{t+1}} = 0 + Q_t = Q_t$$

Case 2:  $S=0$ ;  $R=1$

$$Q_{t+1} = 1 + \overline{Q_t} = 1 = 0$$

$$\overline{Q_{t+1}} = 0 + Q_t = \overline{Q_t}$$

Case 3:  $S=1$ ;  $R=0$

$$Q_{t+1} = 0 + \overline{Q_t} = \overline{Q_t} = Q_t = 1$$

$$\overline{Q_{t+1}} = 1 + Q_t = 1 = 0$$



## S-R Flip-Flop with NOR Gates (Cont)

Case 4:  $S = 1$ ;  $R = 1$

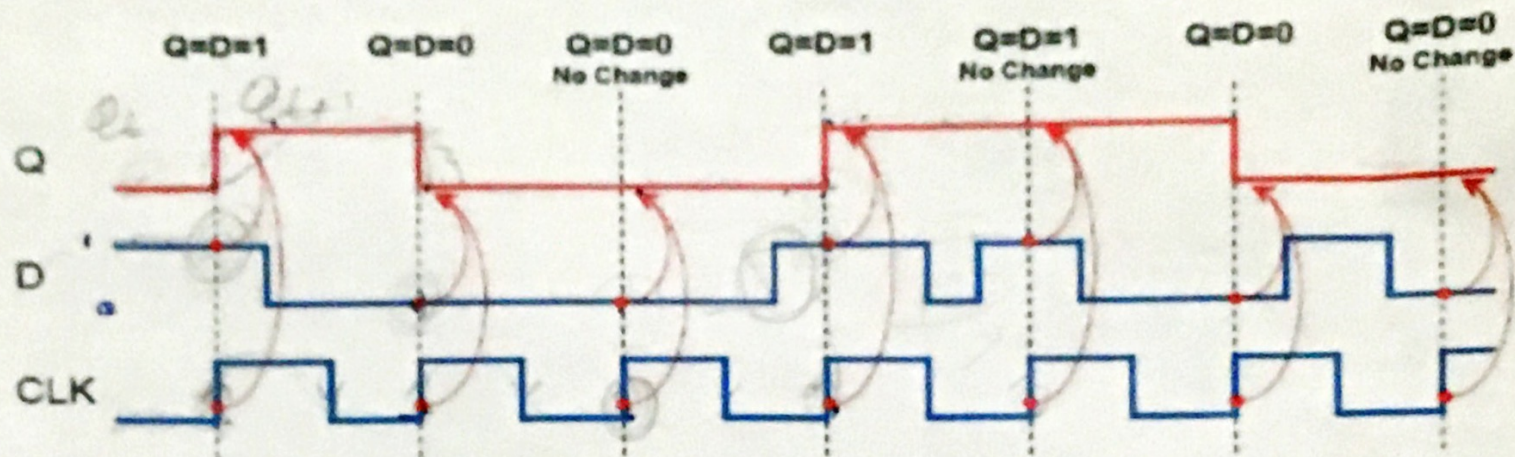
$$Q_{t+1} = \overline{1 + \bar{Q}_t} = \bar{1} = 0$$

$$\bar{Q}_{t+1} = \overline{1 + Q_t} = \bar{1} = 0$$

0 = Not Used!

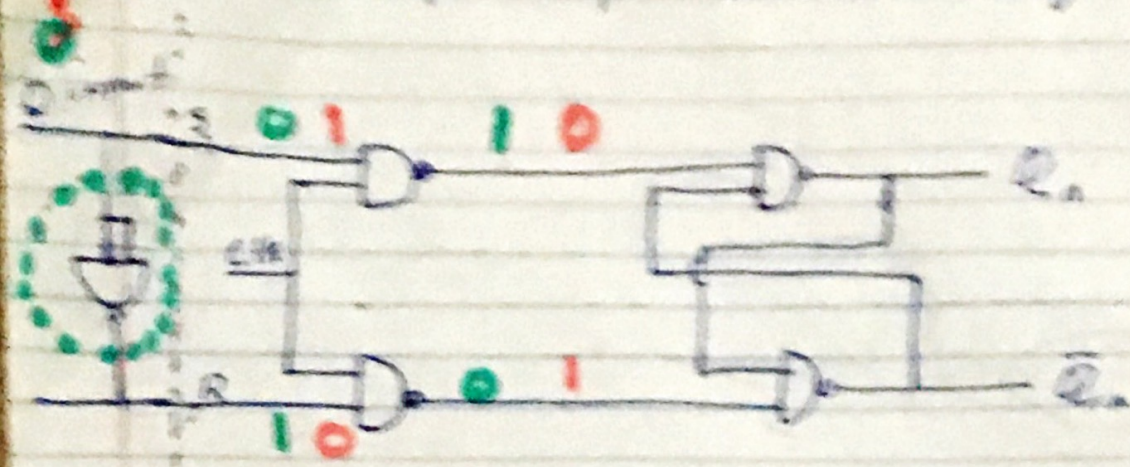


# D Flip-Flop: Example Timing





# D Flip Flop Circuit diagram



Input	Output
D	Q <sub>n+1</sub>
0	0
1	1

set  
reset

Case 1: D = 0

$$Q_{n+1} = 1 \cdot \bar{Q}_n = \bar{Q}_n = Q_n$$

$$\bar{Q}_{n+1} = 0 \cdot Q_n = 0$$

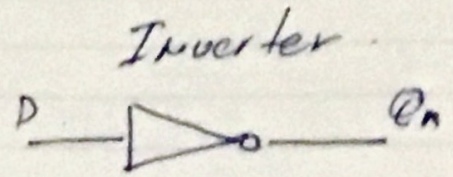
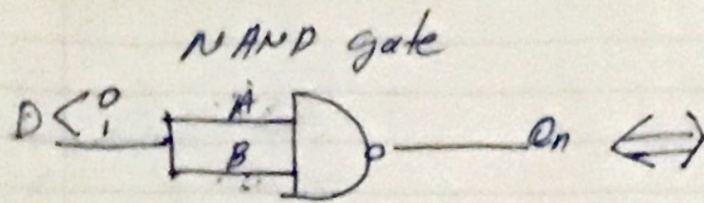
Case 2: D = 1

$$Q_{n+1} = 0 \cdot \bar{Q}_n = 0$$

$$\bar{Q}_{n+1} = 1 \cdot Q_n = Q_n$$



## NAND AS a Inverter



Truth Table

D	A	B	$Q_n$
0	0	0	1
1	1	1	0

A green arrow points to the input D. A green dashed circle highlights the output  $Q_n$  column, which is labeled D.

Truth Table

D	$Q_n$
0	1
1	0

A green arrow points to the input D. A green dashed circle highlights the output  $Q_n$  column.