HW #3

CSc 137, Fall 2020, Harvey

Adder/Mux (12 pts)

1. **Design a Single cell -1 bit Carry propagate (Ripple Carry Adder) full adder. (6 pts)**
   a. **Generate the truth table**
   b. **Using K-map, determine the logical expression for Carry out (C-out) and Sum (S)**
   c. **Based on the logical expression, create the schematic diagram for full adder**

a. X = 0111
Y = 1111

Inputs			Outputs	
X	Y	Z-in	S	Z-out
1	1	0	0	1
1	1	1	1	1
1	1	1	1	1
0	1	1	0	1

Always Zero

S = Sum

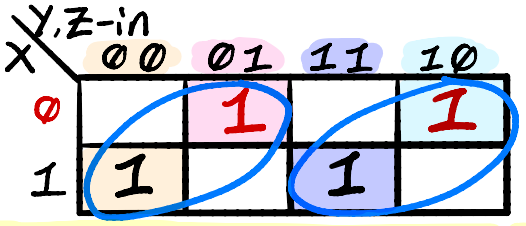
b. Output Logical Expression

$S = \bar{x}\bar{y}z\text{-}in + \bar{x}y\bar{z}\text{-}in + x\bar{y}\bar{z}\text{-}in + xyz\text{-}in$

$Z\text{-}out = \bar{x}yz\text{-}in + x\bar{y}z\text{-}in + xy\bar{z}\text{-}in + xyz\text{-}in$

K-map of the Output Logical Expression

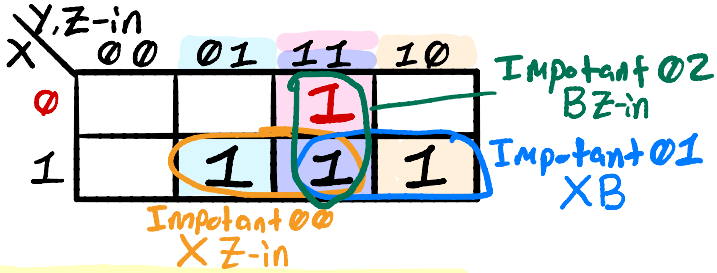
$S = \bar{x}\bar{y}z\text{-}in + \bar{x}y\bar{z}\text{-}in + x\bar{y}\bar{z}\text{-}in + xyz\text{-}in$



See what changes in the impotants *⊕ = XOR*

S-simplified = X ⊕ Y ⊕ Z-in

$Z\text{-}out = \bar{x}yz\text{-}in + x\bar{y}z\text{-}in + xy\bar{z}\text{-}in + xyz\text{-}in$



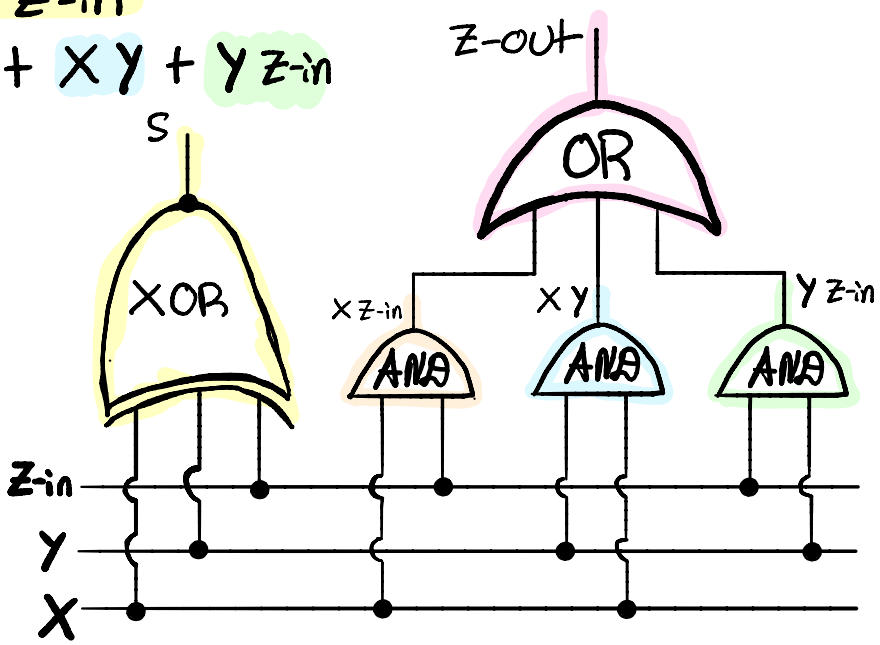
See what changes in the impotants

Z-out simplified = XZ-in + XY + YZ-in

c.

S-simplified = X ⊕ Y ⊕ Z-in

Z-out simplified = XZ-in + XY + YZ-in



HW #3

CSc 137, Fall 2020, Harvey

Adder/Mux (12 pts)

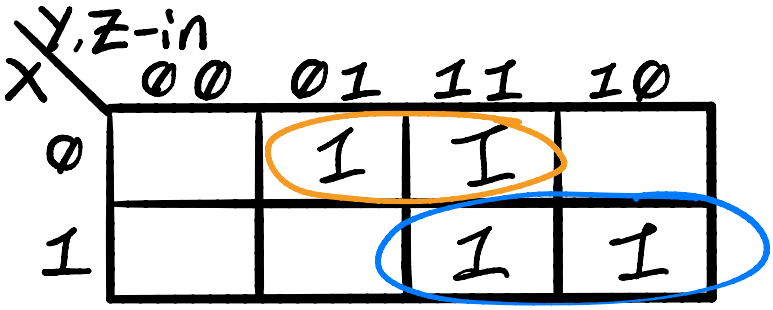
2. **Design a 1 bit, 2 to 1 multiplexer (Mux) (6 pts)**
   a. **Generate the truth table**
   b. **Using K-map, determine the logical expression for output**
   c. **Based on the logical expression, create the schematic diagram for Mux**

a)

ctrl	Input signals		output
S	X	Y	r
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

b)

$$r = \bar{s}\,\bar{x}\,y + \bar{s}\,x\,y + s\,x\,\bar{y}$$



$$S = \bar{s}\,y + s\,x$$

c)