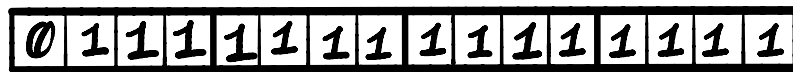


1.6. What is the biggest positive FP number that can be represented in 16-bit format using 1-bit sign, 4-bit biased exponent, and 11-bit fraction, where bias is 7? (4 pts)

Sign  
0 = Positive



Signed Bit

Mantissa/Fraction

Biased Component

$$\text{Biased Exponent} = 1.01011 \times 2^2$$

1.11111  $\times 2^{15} = 1.111_{(2)}$

Signed Component      Fractional Component

Convert to Binary

$$\begin{matrix} 2 \\ (10) \end{matrix} + \begin{matrix} 7 \\ (10) \end{matrix} = \begin{matrix} 15 \\ (10) \end{matrix} \rightarrow \begin{matrix} 15 \\ (10) \end{matrix} = 1111_{(2)}$$

255.3750

1.8 Do the following assuming 16-bit FP numbers with 4-bit bias exponent, bias = 7, and 11-bit fraction: (4 pts)

- a) What real number does an FP number with sign= 0, bias exponent =1 and fraction = 0 represent?

0.015625

Total (16 pts)

2.4 Proof Demorgan's Theorem  $\overline{x + y} = \bar{x} \bar{y}$  by creating truth tables for  $f = \overline{x + y}$  and  $g = \bar{x} \bar{y}$ . Are the two truth tables identical? (4 pts)

## DeMorgan's Theorem

g $A \cdot B$								
Inputs			Outputs					
A	B	A+B	$\overline{A \cdot B}$					
0	0	0	1					
0	1	0	1					
1	0	0	1					
1	1	1	0					

↔

f $\bar{A} + \bar{B}$								
Inputs				Outputs				
A	B	$\bar{A}$	$\bar{B}$	$\bar{A} + \bar{B}$				
0	0	1	1	1				
0	1	1	0	1				
1	0	0	1	1				
1	1	0	0	0				

2.5 Draw the circuit schematic for  $f = x\bar{y} + yz$  and then convert the schematic to NAND gates using the steps illustrated in the textbook. (4 pts)

$$f = x\bar{y} + yz$$

