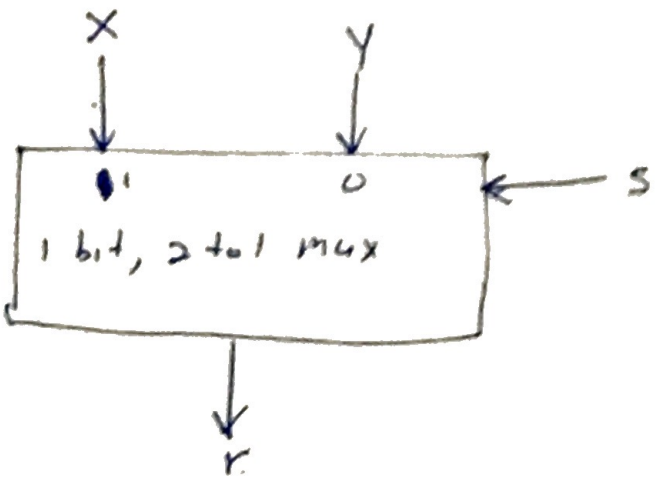
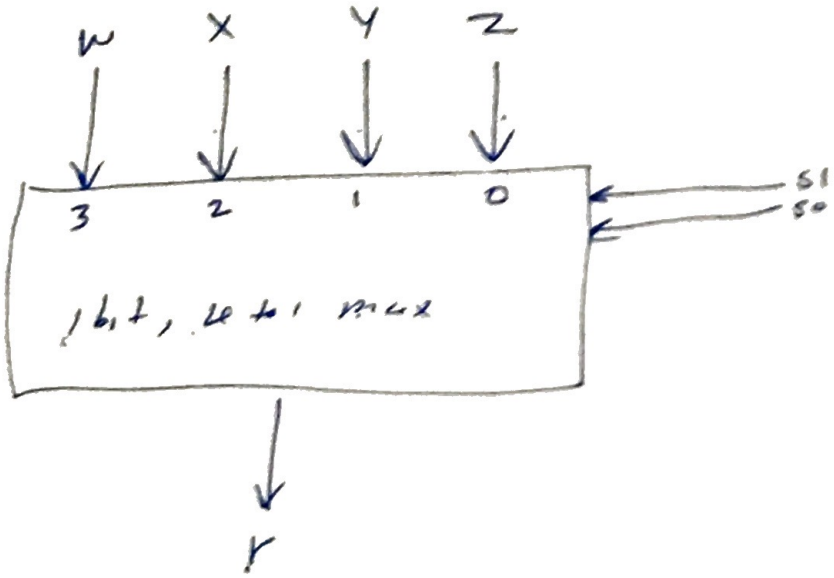
~~Mux~~ Multiplexers (Mux)

a) Block Diagram of 1-bit, 2 to 1 mux

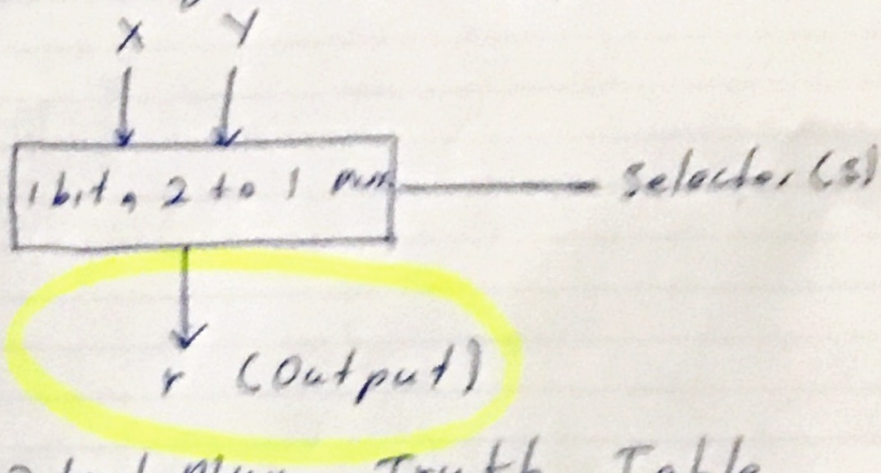


(b) Block Diagram of 1 bit, 4 to 1 mux



Design of 1bit, 2 to 1 Mux

1. Block diagram of 1bit, 2 to 1 Mux



2. 1 bit, 2 to 1 Mux Truth Table

	Ctr	Input Signals		Output
	S	X	Y	r
1	0	0	0	0
2	0	0	1	1
3	0	1	0	0
4	0	1	1	1
5	1	0	0	0
6	1	0	1	0
7	1	1	0	1
8	1	1	1	1

Outputs Y when S=0; Outputs X when S=1.

$$r = \bar{S}\bar{X}Y + \bar{S}XY + S\bar{X}\bar{Y} + SXY$$

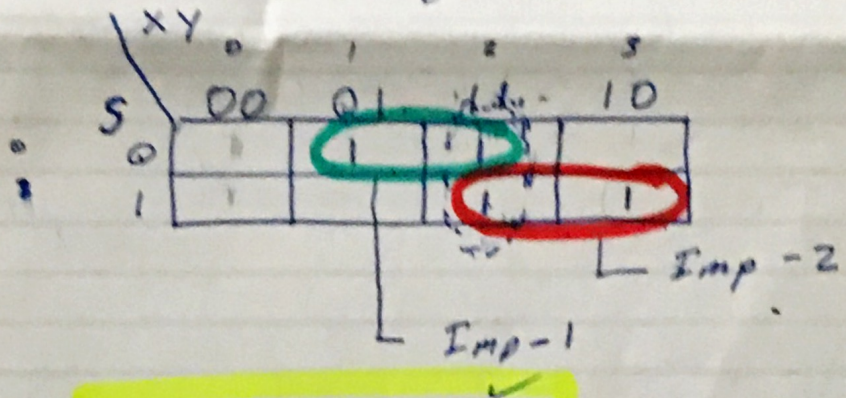
Design of 1 bit, 2 to 1 Mux

3. Simplify the logical Expression:

Minimal SOP Expression: $\bar{S}Y + SX$

$F = \bar{S}\bar{X}Y + \bar{S}XY + SX\bar{Y} + SXY$

Simplify Using K-map:

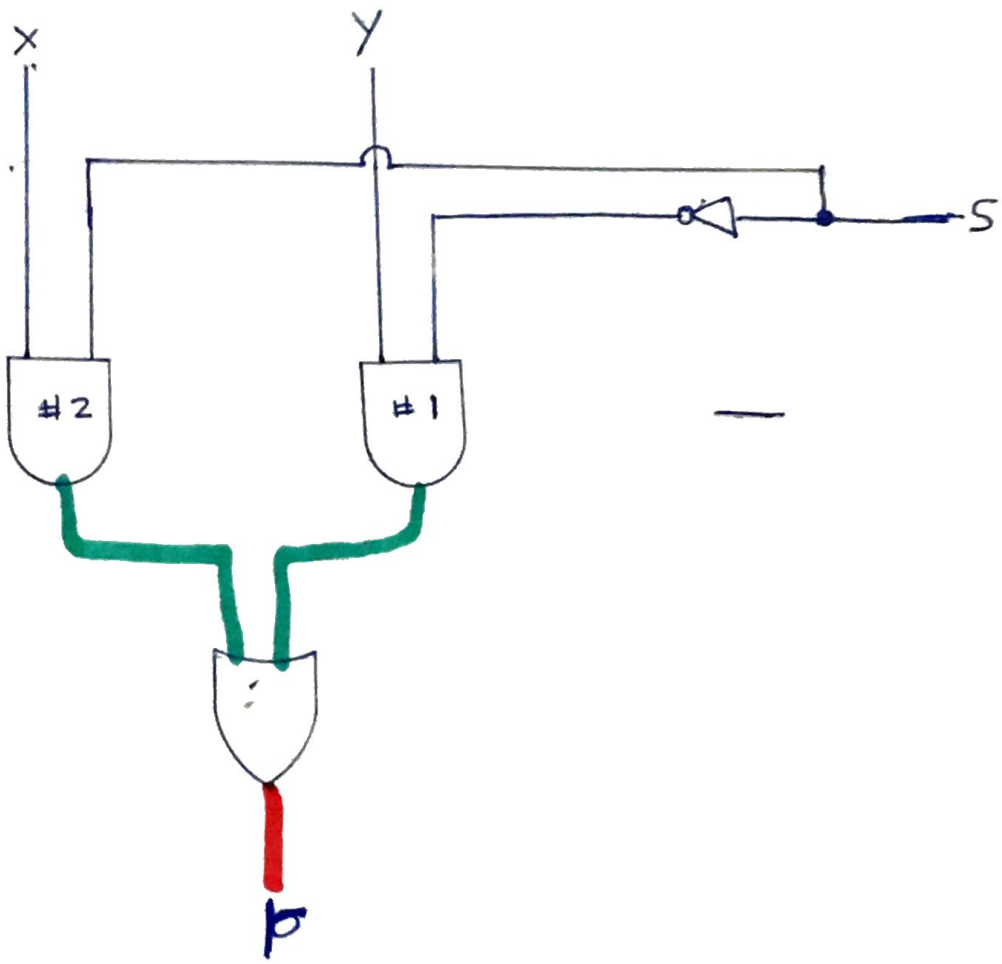


$F = \bar{S}Y + SX$

Design of 1 bit, 2 to 1 mux

4. Design/Circuit diagram for 1 bit, 2 to 1 mux

$$r = \underset{\text{AND \#1}}{\bar{S}Y} + \underset{\text{AND \#2}}{SX}$$



Validation of 1 bit, 2 to 1 Mux

$$r = \bar{S}Y + SX$$

Claimed: Outputs Y when S = 0;
Outputs X when S = 1

$$S = 0$$

$$r = \bar{0}Y + 0X$$

$$= 1 \cdot Y + 0X$$

$$= Y + 0$$

$$\equiv Y$$