CSc 137 - Exam #2

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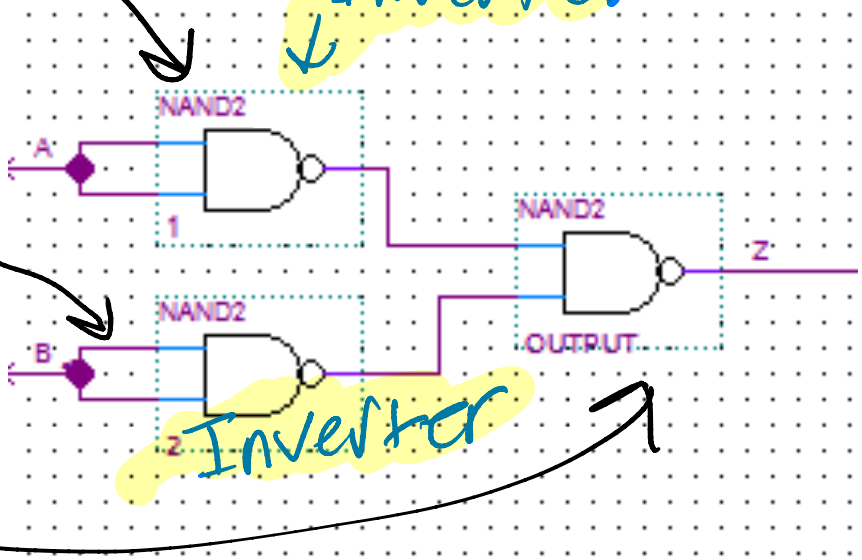
1. Indicate which single logic gate is represented by circuit below? Inputs are A, B and output is Z. (20 pts)

A	Q
1	0
0	1

B	Q
1	0
0	1



A	B	Z
1	1	0
0	0	1

Answer: OR Gate

Three NAND Gates = OR Gate

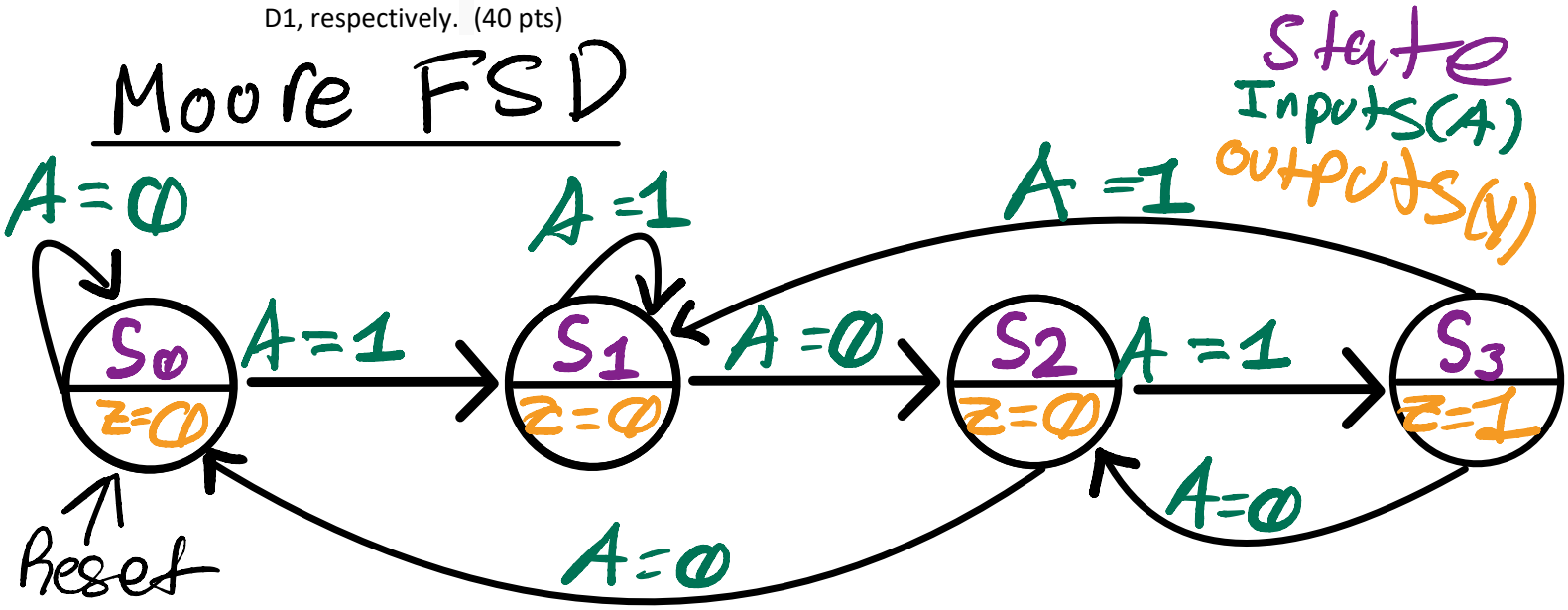
2. Are the following statements True or false? (40 pts)

   (a) The output of a Moore state machine changes synchronously. (Circle the correct answer below)
   True or False ? TRUE

   (b) A NAND gate is the same as a NOR gate with its inputs complemented. (Circle the correct answer below)
   True or False ? False

3. Design a Moore sequence recognizer that detects the overlapping sequence "101". Use binary encoded state labels and design and draw the circuit schematic. (i.e. FSD, Next state generator Table (shows transition from current state to next state), Output Generator Table and schematic circuit. Please use output label as Y and input label as A. Your inputs to D flip-flops will be D0 and D1, respectively. (40 pts)

Moore FSD



NSG

Flip Flop

$S_0 \rightarrow D_0 D_1 = 0\ 0$
$S_1 \rightarrow 0\ 1$
$S_2 \rightarrow 1\ 0$
$S_3 \rightarrow 1\ 1$

	Current State D_0 D_1	Input A	Next state D_0^+ D_1^+	
1	S_0 0 0	0	0 0	S_0
2	0 0	1	0 1	S_1
3	S_1 0 1	0	1 0	S_2
4	0 1	1	0 1	S_1
5	S_2 1 0	0	0 0	S_0
6	1 0	1	1 1	S_3
7	S_3 1 1	0	1 0	S_2
8	1 1	1	0 1	S_1

OG

	Current State D_0	D_1		Output Y
1	0	0	S_0	0
2	0	1	S_1	0
3	1	0	S_2	0
4	1	1	S_3	1

Inputs(4)
outputs(1)

Flip Flop
D_0 D_1

$$D_1^+ = \bar{A} D_0 D_1 + A \bar{D}_0 D_1 + \bar{A} D_0 D_1$$
$$= \bar{A} D_0 D_1 + \bar{A} D_0 D_1 + A \bar{D}_0 D_1$$
$$= \bar{A}(D_0 \bar{D}_1 + D_0 D_1) + A D_0 D_1$$

Complement Law
$D_0(\bar{D}_1 + D_1) = 1$
$D_0 \cdot 1$
$\therefore D_0$

$$= \bar{A}(D_0) + A D_0 D_1$$

$D_0 = X$

$Y = D_0 D_1$