Seq Circuit : Single Cycle

- Equation Estimates min clock period req. to run the data path.

$$T \geq 2\Delta_{Add} + \Delta_{Add|Sub} + \tau_{st} + T_{ca} + T_{cs} \quad (Eq\ 6.1)$$

- Data path that computes either the quantity $A+B+C+D$ or $A+B+C-D$

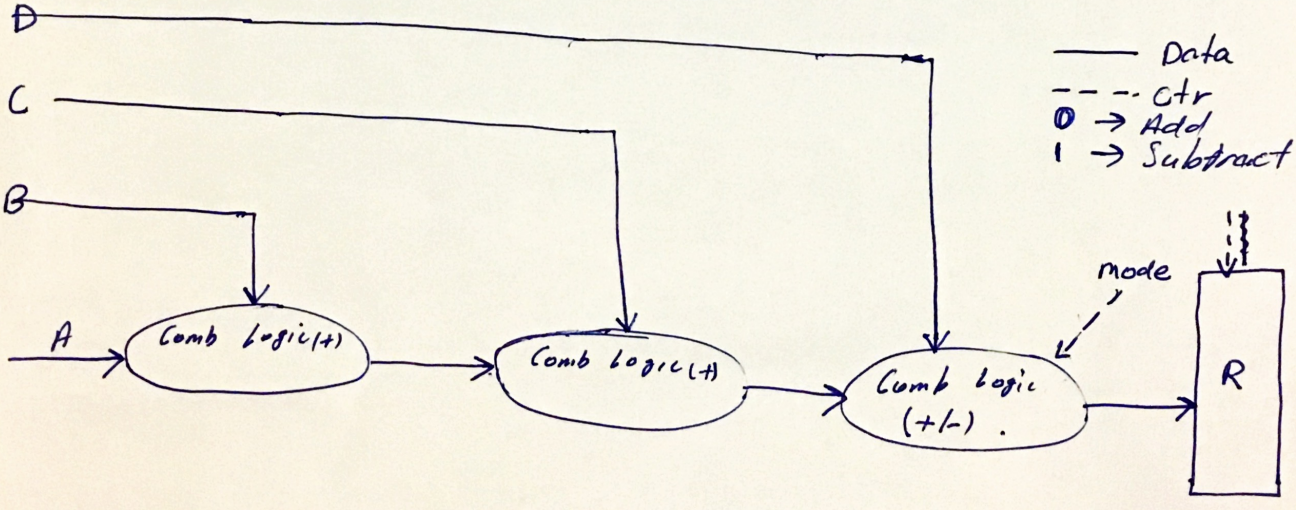

Fig 6.2 ; Single Cycle two function data path - one clock cycle Register

Seq Circuit : Multicycle

- A multicycle data path requires that a computation be divided and computed in steps - simple datapath.

- A multicycle algorithm to implement $R \leftarrow A + B + C \pm D$ (5 possible simple operations)

  Cycle 1 : $R \leftarrow A$

  Cycle 2 : $R \leftarrow R + B$

  Cycle 3 : $R \leftarrow R + C$

  Cycle 4 : if mode == 0 then $R \leftarrow R + D$; otherwise $R \leftarrow R - D$

- Clock period of a multicycle data path is also proportional to longest signal path.

$$T = \Delta_{mux1} + \Delta_{Add/Sub} + \Delta_{mux2} + T_{st} + T_{cq} + T_{cs}$$

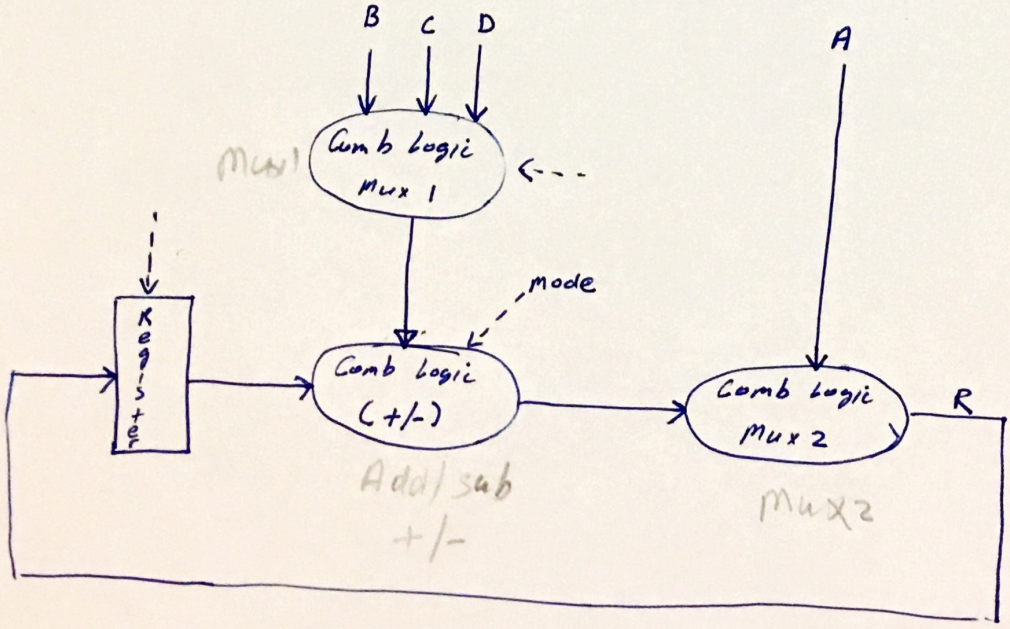

Fig 6.2

Fig 6.3: Multicycle data - Requiring 4 cycles

Seq Circuit: Pipelined Data Path (Cont)

- Computing stream of quantities $A_i + B_i + C_i \pm D_i$

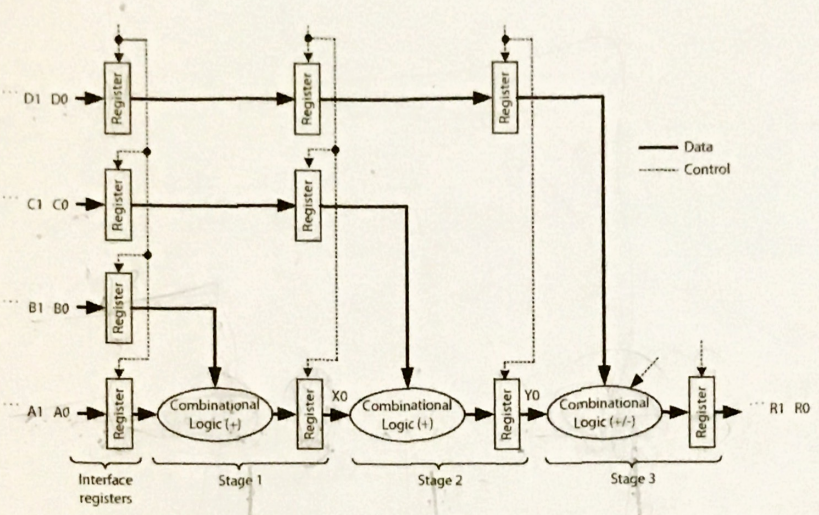

FIGURE 6.4 A two-function pipelined data path computing a stream of quantities $A_i + B_i + C_i \pm D_i$ for $i = 0, 1, 2$, etc.