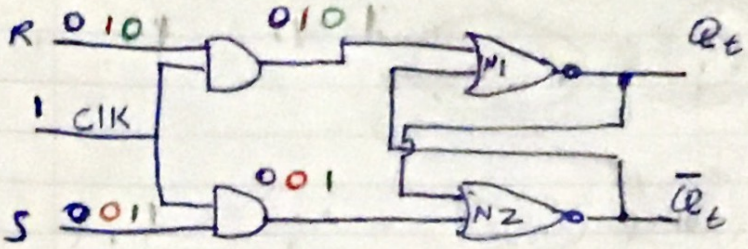
NOR

S-R Flip-Flop with Gates



	S	R	Q_t	Q_{t+1}
1	0	0	Q_t	Q_t
2	0	1	0	0
3	1	0	1	1
4	1	1		Undefined

CLK = Clock Signal

Case1: S = 0; R = 0

$$Q_{t+1} = \overline{0 + \bar{Q}_t} = \bar{\bar{Q}}_t = Q_t$$

$$\bar{Q}_{t+1} = \overline{0 + Q_t} = \bar{Q}_t$$

Case 2: S = 0, R = 1

$$Q_{t+1} = \overline{1 + \bar{Q}_t} = \bar{1} = 0$$

$$\bar{Q}_{t+1} = \overline{0 + Q_t} = \bar{Q}_t$$

Case 3: S = 1; R = 0

$$Q_{t+1} = \overline{0 + \bar{Q}_t} = \bar{\bar{Q}}_t = Q_t = 1$$

$$\bar{Q}_{t+1} = \overline{1 + Q_t} = \bar{1} = 0$$

S-R Flip-Flop with NOR Gates (Cont)

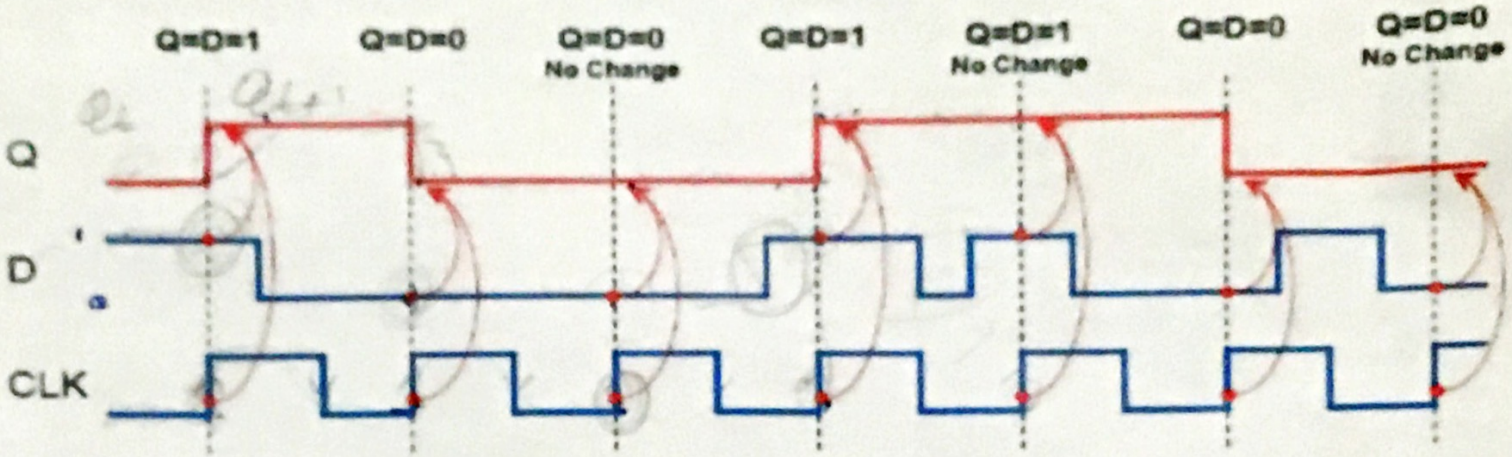
Case 4: $S = 1$; $R = 1$

$$Q_{t+1} = \overline{1 + \bar{Q}_t} = \overline{1} = 0 \quad \emptyset$$

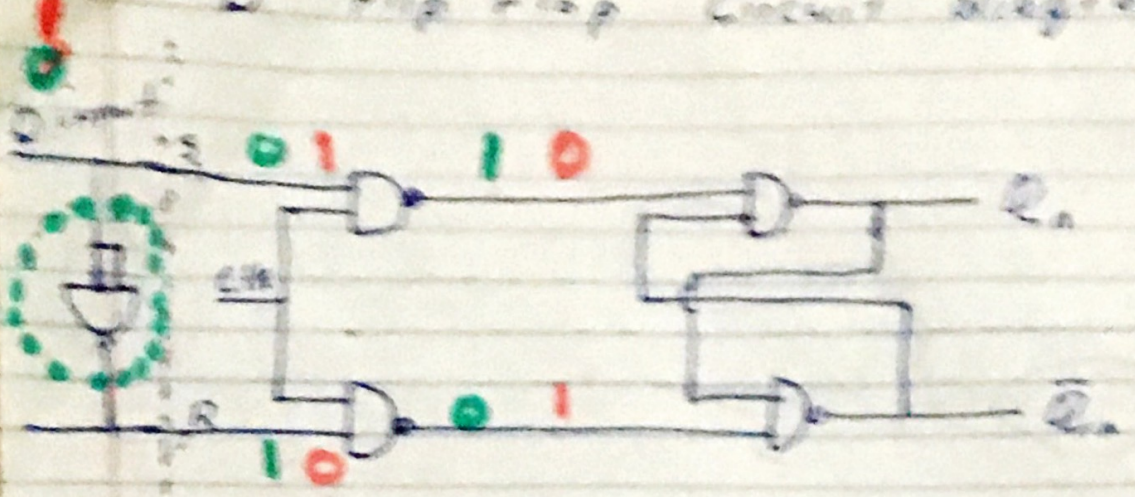
$$\overline{Q_{t+1}} = \overline{1 + Q_t} = \overline{1} = 0 \quad \emptyset$$

$\emptyset$ = Not Used!

D Flip-Flop: Example Timing



D Flip Flop Circuit diagram



Input		Output
D	Q_n	Q_{n+1}
0		0
1	0	1
	1	

Reset

Set

Case 1: D = 0

$$Q_{n+1} = \overline{1 \cdot \bar{Q}_n} = \bar{\bar{Q}}_n = Q_n$$

$$\overline{Q_{n+1}} = \overline{0 \cdot Q_n} = 1$$

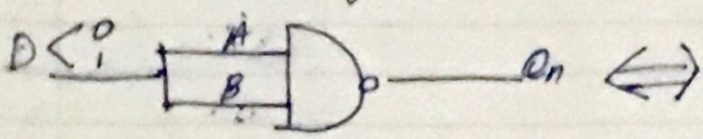
Case 2: D = 1

$$Q_{n+1} = \overline{0 \cdot \bar{Q}_n} = 1$$

$$\overline{Q_{n+1}} = \overline{1 \cdot Q_n} = 0$$

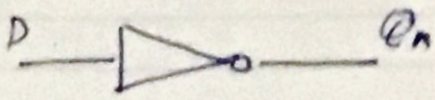
NAND As a Inverter

NAND gate



$\Leftrightarrow$

Inverter



D	A	B	Qn
0	0	0	1
1	1	1	D
			1

Truth Table

D	Qn
0	1
1	0