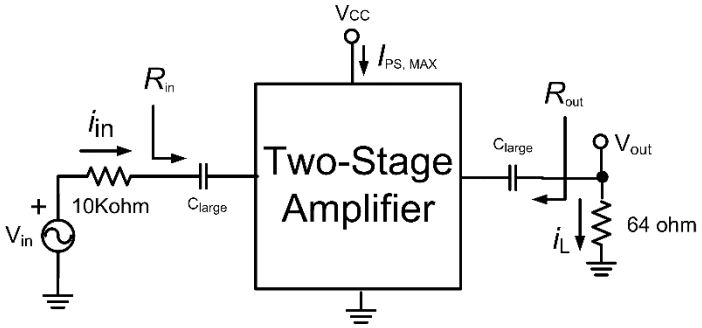
Design a two-stage BJT class-A amplifier to provide the following characteristics.

This project is an individual effort.

DESIGN SPECIFICATIONS:

- Transistors: type 2N2222, nominal β = 200 with β_{min} = 100 and β_{max} =300
  (For OrCAD, select Q2N2222 in "Eval" library and edit the "PSpice Model" to change the value for β_f - right mouse click on transistor)
- Power Supply: V_{CC} from Project #1
- Source frequency = 1kHz
- Load Impedance: 64Ω (impedance of speaker)



Performance Requirements

1. Primary Goal: Output load current peak swing, $i_{L,PEAK} \geq 70mA$ before clipping (140mA peak-to-peak) over the range $100 \leq \beta \leq 300$. Extra points for $i_{L,PEAK} > 70mA$.
2. Primary Goal, the total (2-stage) small signal current gain, $A_i = \left|\frac{i_L}{i_s}\right| = 140$ at $\beta = 200$. Simulated gain should be within 10% of this value.
3. Primary Goal: Do not exceed maximum power dissipation for any 2N2222 of 0.6 watts.
4. Primary Goal: Do not exceed maximum power dissipation for any resistor of 3 watts.
5. Secondary goal, total power supply current, $\boldsymbol{I_{PS}}$, should not exceed 185mA. Extra points for $\boldsymbol{I_{PS}}$<125mA.
6. Secondary goal, $\boldsymbol{R_{in}}$ of complete amplifier = 10kΩ +/- 10%.
7. Extra Points if your small signal gain, $A_i = \left|\frac{i_L}{i_s}\right|$, is stable with changes in β over the range $100 \leq \beta \leq 300$. A stable gain is $A_i \pm 15\%$ over this range in β using your β=200 value as nominal.

Notes:

- Resistors can have any value during the initial design. You don't need to adhere to industry standard values unless you want to (could be helpful later). If you calculate a resistor of 2 ohms or less, then you probably don't need this one.
- When calculating the DC operation of your "driver" circuit, it could be helpful to use the typical approximation for VBEQ = 0.7V.

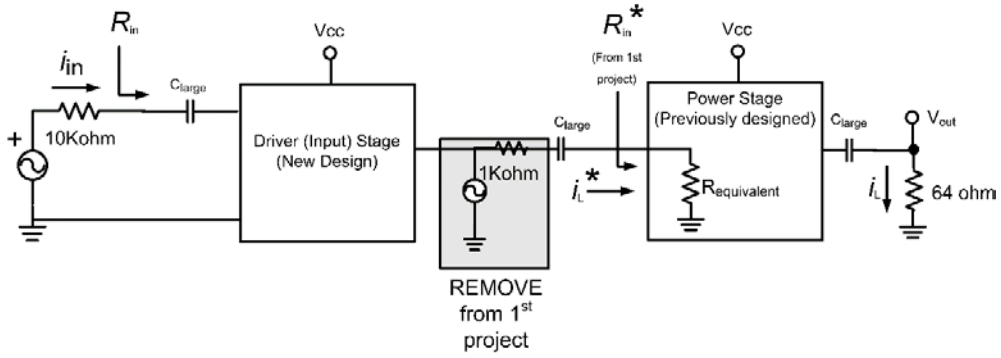
- There will be differences between your hand calculations and the PSpice results. You will start the PSpice simulation using your hand calculated values then you will slightly adjust the resistor(s) of the "driver" circuit until you achieve the required specifications in PSpice.
- Assume r_o = infinite (transistor small signal model)

Submission Requirements:

DESIGN: You will need the following parameters from Project #1:

1. V_{CC}
2. R_{in}^* (PSpice simulated input resistance)
3. A_i^* (PSpice simulated small signal gain)
4. I_{PS}, I_{CQ}, V_{BEQ}, V_{CEQ}, and P_D (PSpice simulated)

Design the input "driver" stage to your two-stage amplifier by using the equivalent input resistance, R_{in}, of your Project 1 as the "load" to this new amplifier as shown in the figure below. You will need to translate the current gain and maximum swing specs to the equivalent circuit using the small signal gain from Project #1, A_i*. Also remove the voltage source and 100Ω source resistor used during the design of the Project 1 as shown below.



When designing the driver amp circuit, translate the specs using the following:

- Current gain of Driver Amp = 140 / (A_i^*)
- Max. current swing of Driver Amp = 70mA / (A_i^*)

After you are confident that your design meets the specifications, answer the following questions.

1) HAND CALCULATIONS:

a. From project #1, list the selected V_{CC}, the PSpice equivalent input resistance, R_{in}^*, and PSpice small signal current gain, A_i^*. List these parameters on a **table**.
b. What are your calculated DC transistor bias parameters? Make a **table** showing I_{CQ}, V_{BEQ}, V_{CEQ}, and P_D for the driver transistor.
c. What are the power rating for each of your resistors? Make a **table** of the resistor values and expected power dissipation.
d. What is your total DC current, I_{PS}, supplied from the DC voltage source (both stages for a total; use PSpice value, I_{PS}, for project #1)?
e. What is your calculated small signal current gain, A_i? Make a **table** of the gain for the driver (input) stage, the power amp stage (PSpice), and the combined two-stage design.

f. What is your calculated small-signal Input Resistance, R_{in}, of the complete two-stage amplifier? Did you achieve a calculated input resistance of 10kΩ?
g. Submit the complete schematic of your two-stage design.
h. Submit a copy of your hand calculations showing important calculations and selection of all resistor values.

2) PSPICE SCHEMATIC: **Submit your PSpice schematic** for the complete two stage amplifier (driver and power amp connected together). On this schematic, show all values for DC voltage, DC current and DC Power for each circuit element (for OrCAD, select V, I and P from the menu). On the schematic, make sure the DC parameters are positioned to allow the display of each resistor value (no display overlaps).
3) SIMLATED DC BIAS: What are the simulated DC bias parameters, I_{CQ}, V_{CEQ}, V_{BEQ} and transistor Power Dissipation, P_D? Submit a table showing the simulated values for I_{CQ}, V_{CEQ}, V_{BEQ}, and P_D for each transistor. As a comparison and on this same table, include the values that you calculated in (b) above.
4) SIMLATED POWER SUPPLY BIAS: What is the total current delivered from the supply, I_{PS}? Does your circuit operate below the specification for maximum current, I_{PS} < 185mA. Extra points for I_{PS}<125mA.
5) SIMULATED CURRENT SWING: Simulate your two-stage design in PSpice using a 1kHz sinusoidal input. Place a current probe on the wire leading into your circuit (on the left side of the capacitor). What is the largest peak-to-peak swing in the output current, i_L, through the 64 ohm load resistance? To find the maximum swing, you should slowly increase the source current amplitude until the output current waveform begins to clip at the top or the bottom. Unless you have a design optimized for maximum symmetrical swing in I_{CQ}, it's most likely that the clipping will not be symmetrical. In other words, the point of clipping in the positive peak current will be different from the negative peak current. **Submit a plot** showing i_L with clipping using a β = 200. When clipping occurs, chose the smaller of the two values and double this value, this is the peak-to-peak swing in the output current, i_L. **Report** the peak-to-peak swing in the output current, i_L. Did your design achieve the 70mA peak swing (140mA peak-to-peak)?
6) Repeat (E) for β = 100 and 300. **Submit a table** showing the maximum peak-to-peak swing in i_L for β = 100, 200 and 300. Did you meet the peak-to-peak swing under all conditions?
7) SIMULATED EFFICIENCY: Using the peak swing in load current, i_L, and load resistance, 64 ohms, **calculate the simulated power conversion efficiency, η**? You will need the simulated I_{PS} in this calculation. Show all your calculations using data recorded from your simulated plots, no points for just an answer.
8) SIMULATED SMALL SIGNAL OPERATION: Using PSpice, reduce the input source amplitude until both transistors are operating in the small signal region. This current should be small enough to operate your transistor in the small signal region. Verify that the peak AC voltage across the Base-Emitter junction, v_{be}, is less than 2.6mV peak (<<26mV) for both transistors. In OrCAD, you can verify the voltage using the "Differential Voltage Probe" measurement. If v_{be} is greater than 2.6mV, decrease the source current until the voltage is in the small signal range for both transistors. **Record** the amplitude value of the source for small signal operation. **Submit plots** showing of v_{BE} for β = 200 for both transistors. Use a scale so the voltage waveforms can easily be observed.

9) SIMULATED TWO-STAGE CURRENT GAIN: Using the input source amplitude found in part (8), what is the small signal gain, $A_i = \left|\frac{i_L}{i_s}\right|$, at β = 200? **Submit two plots** showing i_S and i_L under small signal conditions using a β = 200. Did you achieve a current gain, $|i_L/i_S|$, of 140 ?
10) SIMULATED GAIN VARIATION WITH β: Continue with Step (9), what is the current gain, i_L/i_S, when β =100 and β =300 (plots are not required here)? **Submit a table** showing current gain, $A_i = \left|\frac{i_L}{i_s}\right|$, for β = 100, 200 and 300. What is the % variation in your gain across this range in β (relative to β = 200)? Do you achieve a current gain variation ± 15% about the nominal value of β = 200?
11) SIMULATED INPUT RESISTANCE: Using the source amplitude found in part (8), what is the simulated input resistance, ***Rin***, to your amplifier? Using current and voltage test probes at the amplifier input to calculate the input resistance using PSpice by placing cursors at the peak of each sinusoidal waveform and dividing the voltage peak by the current peak (absolute values are acceptable if required). Note that the placement of V/I probes on the schematic in circuit areas where there is DC voltage and/or DC current will result in a DC offset in the simulated measurements, if so, either move the probe or subtract the DC offset from the results. **Submit a plot** showing ***v***s and ***i***s on two separate graphs for β = 200. **Submit a table** showing ***Rin*** for β = 100, 200 and 300. Did you achieve an input resistance of 10 kΩ+/−10%?
12) SIMULATED FREQUENCY RESPONSE: Perform a small signal "AC" analysis of the small signal current gain over the frequency range of 100Hz to 10MHz for β=200 (note: in OrCAD, you will need to change the source to VAC component). **Record** the 3dB bandwidth of the current gain, $|i_L/i_S|$ (use 20*log10($|i_L/i_S|$))? You may need to increase the upper end of the frequency range (>10MHz) if the gain has not fallen by 3dB. **Submit a plot** showing the current gain as a function of frequency using a "log" scale in the x-axis and calculated "dB' in the y-axis. What does this frequency range tell you about your amplifier?
13) SIMULATION USING STANDARD RESISTOR VALUES: Using your PSPICE design, substitute the standard resistors into your model. Using β=200, simulate the peak-peak current swing and small signal current gain. **Submit a plot** showing i_L with clipping at both the positive and negative peaks using a β = 200. **Submit plots** of i_s and i_L under small signal conditions. Did your amplifier achieve the peak-peak and nominal gain specifications when the resistors are changed? **Submit a table** comparing the simulated peak swing, the simulated small signal gain and input resistance with the original and standard resistors.
14) COMPONENT BILL OF MATERIALS (BOM) FOR LAB EXPERIMENT: Create the BOM, with standard resistor values (ohms), the quantities for each type of resistor and the required power spec (1/4 watt, ½ watt, 1 watt or 3 watt). Include the BOM in your project submission and also s**ubmit your BOM by email to Robert Rivera, rwrivera@nyu.edu. In the email subject - include class and lab section (for example, EE3124 BOM Lab Section A1). The BOM must be received by Friday, April 6 at 9:00am.**