



Ultra Low Power Stereo Audio Codec

GENERAL DESCRIPTION

The MAX98090 is a fully integrated audio codec whose high performance, ultra low power consumption and small footprint make it ideal for portable applications.

Stereo Class D speaker amplifiers provide efficient amplification. Low radiated emissions enable completely filterless operation.

The Class H headphone amplifiers provide a ground referenced output eliminating the need for large DC blocking capacitors. Class H operation power by a 1.8V supply ensures low power consumption and high efficiency. Also included is a differential receiver (earpiece) amplifier that can reconfigured as stereo line outputs.

The MAX98090 features a highly flexible input scheme that includes six analog input pins that can be configured as microphone inputs or single ended line or differential inputs.

The digital audio interface can accept standard PCM formats such as I²S, left-justified, right-justified, and TDM as well as supporting sample rates from 8-96 kHz.

The integrated FLEXSOUND™ digital signal processing includes an Automatic level control and a seven band equalizer that can improve loudspeaker performance by optimizing the frequency response.

FEATURES

- ◆ 102dB DR Stereo DAC (8kHz < Fs < 96kHz)
- ◆ < 4 mW Playback Power Consumption
- ◆ 95dB DR Stereo ADC (8kHz < Fs < 96kHz)
- ◆ < 4.5 mW Record Playback Power Consumption
- ◆ Stereo Low EMI Class D Amplifier, 950mW / Channel (8Ω, SPK_VDD = 4.2V)
- ◆ Stereo Ground Referenced Class H Headphone Amplifier
- ◆ Differential Earpiece Amplifier / Stereo Line Output
- ◆ 3 Stereo Single-Ended / Mono Differential Inputs (WLP version)
- ◆ FLEXSOUND™ Technology Signal Processing
 - 7-Band Parametric EQ
 - ALC
- ◆ I²S / LJ / RJ / TDM Digital Audio Interface
- ◆ Supports Master Clock Frequencies from 256 x Fs to 60MHz
- ◆ RF Immune Analog Inputs and Outputs
- ◆ Extensive Click-and-Pop Reduction Circuitry
- ◆ I²C Programmable Control Interface
- ◆ Jack Detection
- ◆ 49-Bump 0.4mm WLP and 40-Pin TQFN

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
MAX98090AEWJ+T	-40°C to +85°C	49 - WLP
MAX98090AETL+T	-40°C to +85°C	40 - TQFN
MAX98090BEWJ+T	-40°C to +85°C	49 - WLP
MAX98090BETL+T	-40°C to +85°C	40 - TQFN

SIMPLIFIED BLOCK DIAGRAM

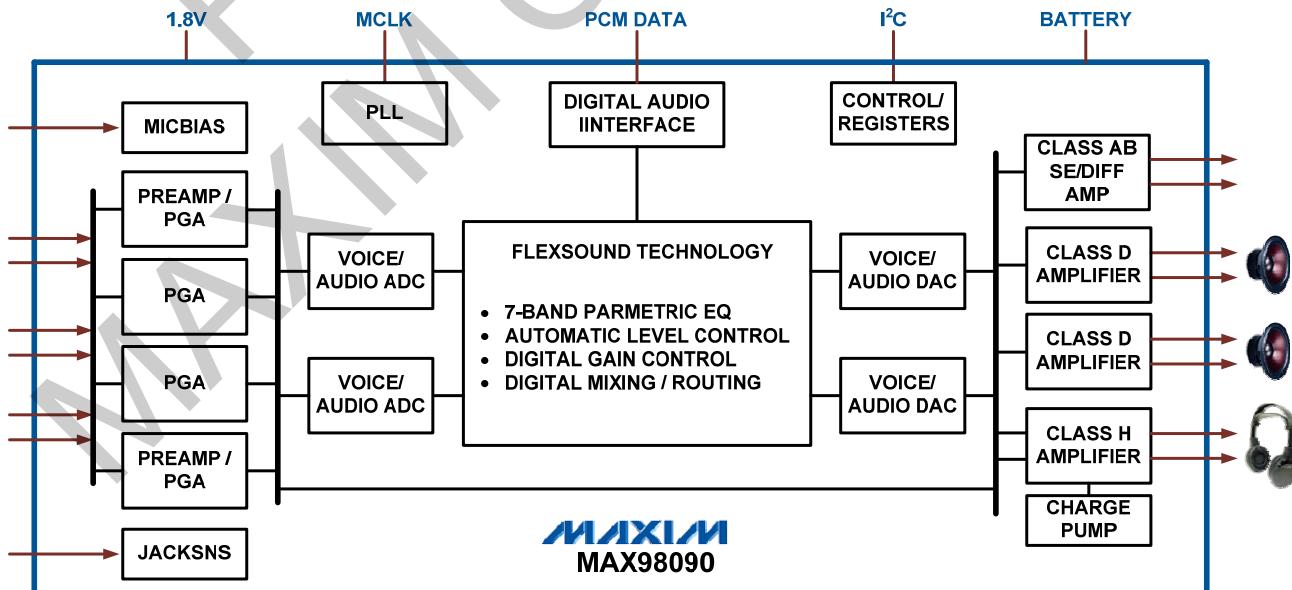
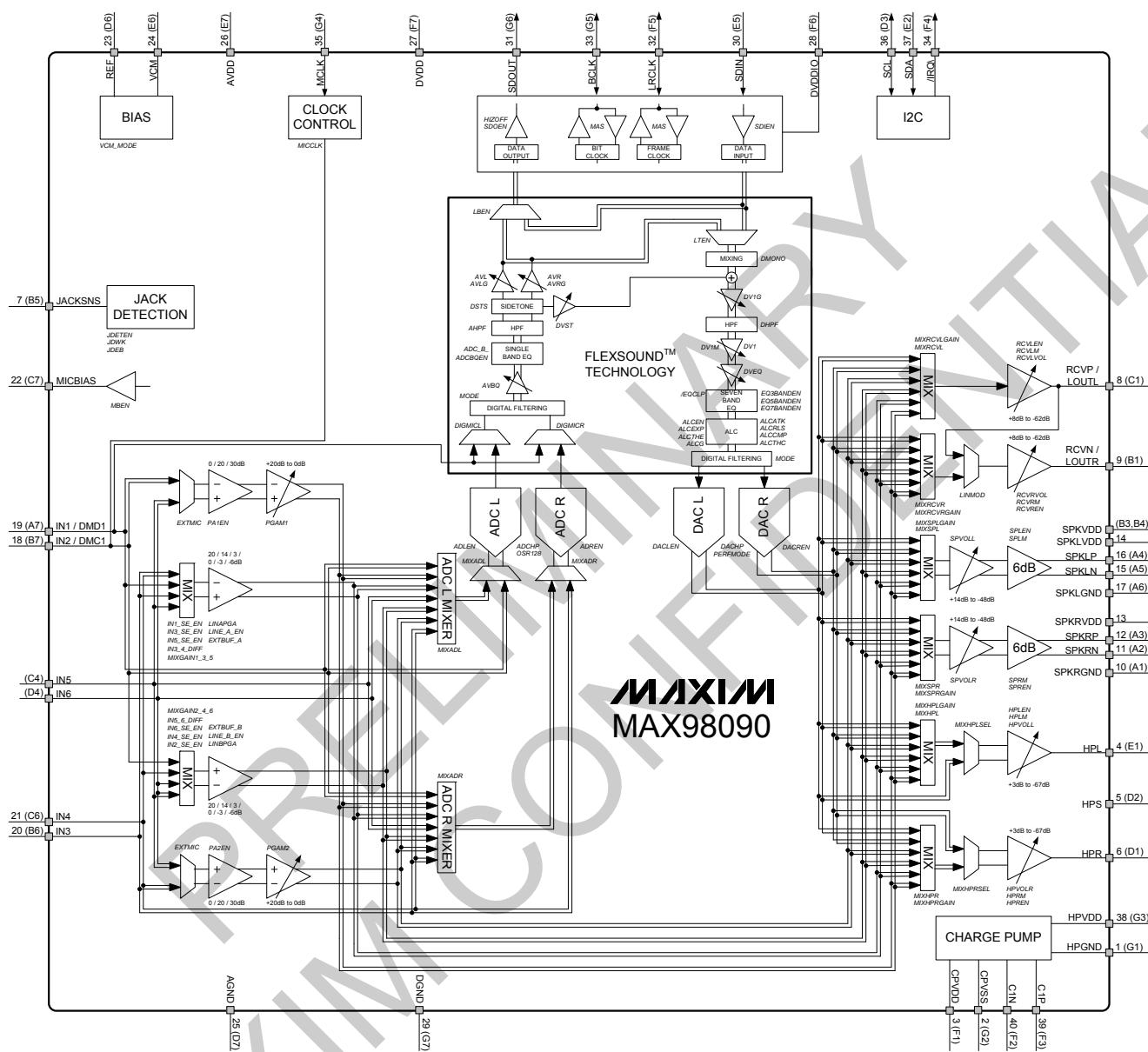


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ABSOLUTE MAXIMUM RATINGS

(Voltages with respect to AGND)

AVDD, CPVDD, HPVDD	-0.3V to +2.2V
SPKLVDD, SPKRVDD, DVDDIO	-0.3V to +6.0V
DGND, HPGND, SPKLGND, SPKRGND	-0.1V to +0.1V
CPVSS	(HPGND - 2.2V) to (HPGND + 0.3V)
C1N	(HPVSS - 0.3V) to (HPGND + 0.3V)
C1P	(HPGND - 0.3V) to (HPVDD + 0.3V)
MICBIAS	-0.3V to (SPKLVDD+0.3V)
REF, VCM	-0.3V to (AVDD+0.3V)
MCLK, SDIN, SDA, SCL, /IRQ\	-0.3V to +6.0V
LRCLK, BCLK, SDOUT	-0.3V to (DVDDIO+0.3V)
IN1, IN2, IN3, IN4, IN5, IN6	-0.3V to +2.2V

HPSNS	(HPGND - 0.3V) to (HPGND+0.3V)
HPL, HPR	(HPVSS - 0.3V) to (HPVDD+0.3V)
RCVP, RCVN	(SPKLGND - 0.3V) to (SPKLVDD+0.3V)
SPKLP, SPKLN	(SPKLGND - 0.3V) to (SPKLVDD+0.3V)
SPKRP, SPKRN	(SPKRGND - 0.3V) to (SPKRVDD+0.3V)
JACKSNS	-0.3V to +6.0V
Continuous Power Dissipation ($T_A=+70^\circ C$)	
49-Bump WLP (derate 23.8mW/ $^\circ C$ above $+70^\circ C$)	TBDW
40-Pin TQFN (derate 35.7mW/ $^\circ C$ above $+70^\circ C$)	2.86W
Operating Temp Range	-40C to +85C
Storage Temp Range	-65C to +150C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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PACKAGE THERMAL CHARACTERISTICS

49-Bump WLP

Junction-to-Ambient Thermal Resistance (θ_{JA})	42 $^\circ C/W$
Junction-to-Case Thermal Resistance (θ_{JC})	1 $^\circ C/W$

40-Pin TQFN

Junction-to-Ambient Thermal Resistance (θ_{JA})	28 $^\circ C/W$
Junction-to-Case Thermal Resistance (θ_{JC})	2 $^\circ C/W$

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, see www.maxim-ic.com/thermal-tutorial.

ELECTRICAL CHARACTERISTICS

($V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = +1.8V$, $V_{DVDD} = 1.2V$, $V_{SPKLVDD} = V_{SPKRVDD} = V_{SPKVDD} = 3.7V$). Receiver load (R_{REC}) connected between RECP/LOUTL and RECN/LOUTR (LINMOD=0). Line Output loads (R_{LOUT}) connected between RECP/LOUTL and RECN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. $R_{REC} = \infty$, $R_{LOUT} = \infty$, $R_{HP} = \infty$, $Z_{SPK} = \infty$. $C_{REF} = 2.2\mu F$, $C_{VCM} = C_{MICBIAS} = 1\mu F$, $C_{CIN-C1P} = C_{CPVDD} = C_{CPVSS} = 1\mu F$. $A_{V_MICPRE} = A_{V_MICPGA} = A_{V_LINEPGA} = 0dB$, $A_{V_ADCLVL} = A_{V_ADCAGAIN} = 0dB$, $A_{V_DACLVL} = A_{V_DAGAIN} = 0dB$, $A_{V_MIXGAIN} = 0dB$, $A_{V_REC} = A_{V_LOUT}$, $A_{V_HP} = A_{V_SPK} = 0dB$. $f_{MCLK} = 12.288MHz$, $f_{RCLK} = 48kHz$, MAS = 0, 20-bit source data. $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage Range		Guaranteed by PSRR (Note 12)	$V_{SPKLVDD}, V_{SPKRVDD}$	2.8	3.7	5.5
			V_{AVDD}, V_{HPVDD}	1.65	1.8	2
			V_{DVDD}	1.08	1.2	1.98
			V_{DVDDIO}	1.65	1.8	3.6
Total Supply Current (Note 2)	I_{VDD}	Full Duplex 8kHz Mono, Receiver Output	Analog	1.97	3.5	mA
			Speaker	0.70	2	
			Digital	0.71	1.2	
		DAC Playback 48kHz Stereo, Headphone Outputs	Analog	1.45	2	
			Speaker	0	0.005	
			Digital	0.79	1.2	
		DAC Playback 48kHz Stereo, Speaker Outputs	Analog	0.91	2	
			Speaker	2.21	3	
			Digital	0.80	1.2	
REF Voltage					1.25	V
VCM Voltage		VCM from Resistive Division (VCM_MODE = 0)			0.90	V
		VCM from Bandgap (VCM_MODE = 1)			0.78	
Shutdown Supply Current (Note 2)		$T_A = +25^\circ C$	Analog	1	10	μA
			Speaker	1	5	
			Digital	2.1	20	
Shutdown to Full Operation					10	ms
DIFFERENTIAL INPUT (MICROPHONE) TO ADC PATH						
Dynamic Range (Note 4)	DR	$A_{V_MICPRE} = 0dB$, $f_s = 48kHz$, MODE = 1 (FIR Audio), A-weighting filter applied.			97	dB
		$A_{V_MICPRE} = 0dB$, $f_s = 8kHz$, MODE = 0 (IIR Voice), A-weighting filter applied.			90	dB
Total Harmonic Distortion + Noise	THD+N	$A_{V_MICPRE} = 20dB$, $V_{IN} = 90mV_{RMS}$, $f = 1kHz$,			-82	-75
		$A_{V_MICPRE} = 0dB$, $V_{IN} = 900mV_{RMS}$, $f = 1kHz$			-91	dB
		$A_{V_MICPRE} = 30dB$, $V_{IN} = 28.5mV_{RMS}$, $f = 1kHz$			-73	
Common-Mode Rejection Ratio	CMRR	$f = 217Hz$, $V_{IN_CM} = 100mV_{P-P}$			59	dB
Power Supply Rejection Ratio (Note 12)	PSRR	$V_{AVDD} = 1.65V$ to $2.0V$, input referred			40	TBD
		$V_{RIPPLE} = 100mV_{P-P}$, input referred, $A_{V_MIC} = A_{V_ADC} = 0dB$	$f = 217Hz$		78	dB
			$f = 1kHz$		78	
			$f = 10kHz$		77	
Path Phase Delay		1kHz, 0dB input, High pass filter disabled measured from analog input to digital output	MODE = 0 (IIR Voice); 8kHz		2.2	ms
			MODE = 0 (IIR Voice); 16kHz		1.1	
			MODE = 1 (FIR Audio) 8kHz		4.5	
			MODE = 1 (FIR Audio) 48kHz		0.8	
Gain Error		DC Accuracy			1	5
						%

($V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = +1.8V$, $V_{DVDD} = 1.2V$, $V_{SPKLVDD} = V_{SPKRVDD} = V_{SPKVDD} = 3.7V$). Receiver load (R_{REC}) connected between RECP/LOUTL and RECN/LOUTR (LINMOD=0). Line Output loads (R_{LOUT}) connected between RECP/LOUTL and RECN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. $R_{REC} = \infty$, $R_{LOUT} = \infty$, $R_{HP} = \infty$, $Z_{SPK} = \infty$. $C_{REF} = 2.2\mu F$, $C_{VCM} = C_{MICBIAS} = 1\mu F$, $C_{CIN-CIP} = C_{CPVDD} = C_{CPVSS} = 1\mu F$. $A_{V_MICPRE_} = A_{V_MICPGA_} = A_{V_LINEPGA_} = 0dB$, $A_{V_ADCLVL} = A_{V_ADCGAIN} = 0dB$, $A_{V_DACLVL} = A_{V_DAGAIN} = 0dB$, $A_{V_MIXGAIN} = 0dB$, $A_{V_REC} = A_{V_LOUT}$, $A_{V_HP} = A_{V_SPK} = 0dB$. $f_{MCLK} = 12.288MHz$, $f_{LRCLK} = 48kHz$, MAS = 0, 20-bit source data. $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIFFERENTIAL (MICROPHONE) PREAMP & PGA						
Full Scale Input		$A_{V_MICPRE_} = 0dB$		1		V_{RMS}
Microphone Pre-Amplifier Gain	$A_{V_MICPRE_}$	Note 5	$PA_EN[1:0] = 01$	0		dB
			$PA_EN[1:0] = 10$	19.5	20	20.5
			$PA_EN[1:0] = 11$	29.5	30	30.5
Microphone Level Adjust Gain (PGA)	$A_{V_MICPGA_}$	Note 5	$PGAM_ [4:0] = 0x00$	19.5	20	20.5
			$PGAM_ [4:0] = 0x14$	0		dB
MIC Input Resistance	R_{IN_MIC}	All Gain Settings, measured at IN_ (measured single-ended).	30	50		$k\Omega$
MICROPHONE BIAS						
MICBIAS Output Voltage	$V_{MICBIAS}$	$I_{LOAD} = 1mA$, $MBVSEL[1:0] = 00$	TBD	2.2	TBD	V
		$I_{LOAD} = 1mA$, $MBVSEL[1:0] = 01$	TBD	2.4	TBD	
		$I_{LOAD} = 1mA$, $MBVSEL[1:0] = 10$	TBD	2.57	TBD	
		$I_{LOAD} = 1mA$, $MBVSEL[1:0] = 11$	TBD	2.8	TBD	
Load Regulation		$I_{LOAD} = 1mA$ to $2mA$, $MBVSEL[1:0] = 00$		0.085	0.28	mV
Line Regulation		$V_{SPKLVDD} = 2.8V$ to $5.5V$, $MBVSEL[1:0] = 00$		9.7	96	μV
Ripple Rejection		$f = 217Hz$, $V_{RIPPLE} (SPKLVDD) = 100mV_{P-P}$		70		dB
		$f = 10kHz$, $V_{RIPPLE} (SPKLVDD) = 100mV_{P-P}$		75		
Noise Voltage		A-weighted, $f = 20Hz - 20kHz$		7.4		μV_{RMS}
		$f = 1kHz$		52.3		nV/\sqrt{Hz}
SINGLE-ENDED (LINE) INPUT TO ADC PATH						
Dynamic Range (Note 4)	DR	$f_s = 48kHz$, $f_{MCLK} = 12.288MHz$, MODE = 1 (FIR Audio)		98		dB
Total Harmonic Distortion + Noise	THD+N	$V_{IN} = 0.222V_{RMS}$, $f = 1kHz$		-85	-80	dB
SINGLE ENDED (LINE) INPUT PGA						
Full Scale Input	V_{IN}	$A_{V_LINEPGA_} = 0dB$		0.5		V_{RMS}
		$A_{V_EXTERNAL} = -6dB$, $EXTBUF = 1$		1		
Line Input Level Adjust Gain (PGA)	$A_{V_LINEPGA}$	Note 5	$PGALIN = 0x0$	19	20	21
			$PGALIN = 0x1$	13	14	15
			$PGALIN = 0x2$	2	3	4
			$PGALIN = 0x3$	-1	0	1
			$PGALIN = 0x4$	-4	-3	-2
			$PGALIN = 0x5, 0x6, 0x7$	-7	-6	-5
Line Input Amplifier Gain	$A_{V_LINEAMP}$	Single Ended Only		6		dB
Input Resistance	R_{IN}	$A_{V_LINEPGA_} = 0dB$		14	20	$k\Omega$
Feedback Resistance	R_{IN_FB}	$T_A = +25^\circ C$		19	20	21
ADC LEVEL CONTROL						
ADC Level Adjust Range	A_{V_ADCLVL}	AVL/AVR = 0xF to 0x0 (Note 5)		-12	3	dB
ADC Level Adjust Step Size				1		dB
ADC Gain Adjust Range	$A_{V_ADCGAIN}$	AVLG/AVRG = 0x0 to 0x3 (Note 5)		0	18	dB
ADC Gain Adjust Step Size				6		dB

($V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = +1.8V$, $V_{DVDD} = 1.2V$, $V_{SPKLVDD} = V_{SPKRVDD} = V_{SPKVDD} = 3.7V$). Receiver load (R_{REC}) connected between RECP/LOUTL and RECN/LOUTR (LINMOD=0). Line Output loads (R_{LOUT}) connected between RECP/LOUTL and RECN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. $R_{REC} = \infty$, $R_{LOUT} = \infty$, $R_{HP} = \infty$, $Z_{SPK} = \infty$. $C_{REF} = 2.2\mu F$, $C_{VCM} = C_{MICBIAS} = 1\mu F$, $C_{CIN-CIP} = C_{CPVDD} = C_{CPVSS} = 1\mu F$. $A_{V_MICPRE_} = A_{V_MICPGA_} = A_{V_LINEPGA_} = 0dB$, $A_{V_ADCLVL} = A_{V_ADCAGAIN} = 0dB$, $A_{V_DACLVL} = A_{V_DAGAIN} = 0dB$, $A_{V_MIXGAIN} = 0dB$, $A_{V_REC} = A_{V_LOUT}$, $A_{V_HP} = A_{V_SPK} = 0dB$. $f_{MCLK} = 12.288MHz$, $f_{LRCLK} = 48kHz$, MAS = 0, 20-bit source data. $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC DIGITAL FILTERS						
VOICE MODE IIR LOWPASS FILTER (MODE = 0)						
Pass band Cutoff	f_{PLP}	Ripple Limit Cutoff	0.445 $\times f_s$	Hz		
		-3dB Cutoff	0.449 $\times f_s$			
Pass band Ripple		$f < f_{PLP}$	-0.1	0.1		dB
Stop band Cutoff	f_{SLP}			0.47 $\times f_s$		Hz
Stop band Attenuation (Note 6)		$f > f_{SLP}$	74			dB
PROGRAMMABLE BIQUAD FILTER						
Pre-Attenuator Gain Range			-15	0		dB
Pre-Attenuator Step Size				1		dB
Minimum Cutoff Frequency		High Pass Filter	0.0008 $\times f_s$	Hz		
		High Frequency Shelving Filter	0.02 $\times f_s$			
		Low Pass Filter	0.002 $\times f_s$			
		Low Frequency Shelving Filter	0.0008 $\times f_s$			
		Peak Filter	0.0008 $\times f_s$			
Maximum Q		Peak Filter		10		
STEREO AUDIO MODE FIR LOWPASS FILTER (MODE = 1, DHF = 0, $f_{LRCLK} < 50kHz$)						
Pass band Cutoff	f_{PLP}	Ripple Limit Cutoff	0.43 $\times f_s$	Hz		
		-3dB Cutoff	0.48 $\times f_s$			
		-6.02dB Cutoff	0.5 $\times f_s$			
Pass band Ripple		$f < f_{PLP}$	-0.1	0.1		dB
Stop band Cutoff	f_{SLP}			0.58 $\times f_s$		Hz
Stop band Attenuation (Note 6)		$f < f_{SLP}$	60			dB
ADC STEREO AUDIO MODE FIR LOWPASS FILTER (MODE = 1, DHF = 1, $f_{LRCLK} > 50kHz$)						
Pass band Cutoff	f_{PLP}	Ripple Limit Cutoff	0.208 $\times f_s$	Hz		
		-3dB Cutoff	0.28 $\times f_s$			
Pass band Ripple		$f < f_{PLP}$	-0.1	0.1		dB
Stop band Cutoff	f_{SLP}			0.45 $\times f_s$		Hz
Stop band Attenuation		$f < f_{SLP}$	60			dB
ADC DC BLOCKING HIGHPASS FILTER						
DC Attenuation	A_{V_ADCHPF}	$A_{HPPF} = 1$		90		dB
ADC TO DAC DIGITAL SIDETONE (MODE = 0)						
Sidetone Level Adjust Range	A_{V_STLVL}	DVST = 0x1F to 0x01	-60.5	-0.5		dB
Sidetone Level Adjust Step Size				2		dB
Sidetone Path Phase Delay		1kHz, 0dB input, High pass filter disabled	8kHz	1.8	ms	
			16kHz	0.9		

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC TO DAC DIGITAL LOOP-THROUGH PATH						
Dynamic Range (Note 4)	DR	$f_S = 48kHz$, $f_{MCLK} = 12.288MHz$, MODE = 1 (FIR Audio)	97			dB
Total Harmonic Distortion + Noise	THD+N	$f_{IN} = 1kHz$, $f_S = 48kHz$, $f_{MCLK} = 12.288MHz$, MODE = 1 (FIR Audio)	-83	-75		dB
DAC LEVEL CONTROL						
DAC Attenuation Range	A_{V_DACLVL}	$DV1 = 0xF$ to $0x0$ (Note 5)	-15	0		dB
DAC Attenuation Step Size				1		dB
DAC Gain Adjust Range	A_{V_DAGAIN}	$DV1G = 00$ to 11 (Note 5)	0	18		dB
DAC Gain Adjust Step Size				6		dB
DAC DIGITAL FILTERS						
VOICE MODE IIR LOWPASS FILTER (MODE = 0)						
Pass band Cutoff	f_{PLP}	Ripple Limit Cutoff	0.448			Hz
		-3dB Cutoff	$0.451 \times f_S$			
Pass band Ripple		$f < f_{PLP}$	-0.1	0.1		dB
Stop band Cutoff	f_{SLP}			0.476		Hz
Stop band Attenuation (Note 6)		$f > f_{SLP}$	75			dB
STEREO AUDIO MODE FIR LOWPASS FILTER (MODE = 1, DHF = 0, $f_{LRCLK} < 50kHz$)						
Pass band Cutoff	f_{PLP}	Ripple Limit Cutoff	0.43			Hz
		-3dB Cutoff	0.47			
		-6.02dB Cutoff	0.5			
Pass band Ripple		$f < f_{PLP}$	-0.1	0.1		dB
Stop band Cutoff	f_{SLP}			0.58		Hz
Stop band Attenuation (Note 6)		$f > f_{SLP}$	60			dB
STEREO AUDIO MODE FIR LOWPASS FILTER (MODE1 = 1, DHF = 1 for $f_{LRCLK} > 50kHz$)						
Pass band Cutoff	f_{PLP}	Ripple Limit Cutoff	0.24			Hz
		-3dB Cutoff	0.31			
Pass band Ripple		$f < f_{PLP}$	-0.1	0.1		dB
Stop band Cutoff	f_{SLP}			0.477		Hz
Stop band Attenuation (Note 6)		$f > f_{SLP}$	60			dB
DAC DC BLOCKING HIGHPASS FILTER						
DC Attenuation	A_{V_DACHPF}	$DHPF = 1$		89		dB
AUTOMATIC LEVEL CONTROL						
Gain Range			0	12		dB
Compression Threshold		Verify – EC table master states -35 but description doesn't match	-31	0		dBFS
Expansion Threshold			-66	-35		dBFS
Attack Time		Discuss – EV-kit does not match Austin - faster	0.0005	0.2		s
Release Time			0.0625	8		s

($V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = +1.8V$, $V_{DVDD} = 1.2V$, $V_{SPKLVDD} = V_{SPKRVDD} = 3.7V$). Receiver load (R_{REC}) connected between RECP/LOUTL and RECN/LOUTR (LINMOD=0). Line Output loads (R_{LOUT}) connected between RECP/LOUTL and RECN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. $R_{REC} = \infty$, $R_{LOUT} = \infty$, $R_{HP} = \infty$, $Z_{SPK} = \infty$. $C_{REF} = 2.2\mu F$, $C_{VCM} = C_{MICBIAS} = 1\mu F$, $C_{CIN-CIP} = C_{CPVDD} = C_{CPVSS} = 1\mu F$. $A_{V_MICPRE_} = A_{V_MCPGA_} = A_{V_LINEPGA_} = 0dB$, $A_{V_ADCLVL} = A_{V_ADCGAIN} = 0dB$, $A_{V_DACLVL} = A_{V_DAGAIN} = 0dB$, $A_{V_MIXGAIN} = 0dB$, $A_{V_REC} = A_{V_LOUT}$, $A_{V_HP} = A_{V_SPK} = 0dB$. $f_{MCLK} = 12.288MHz$, $f_{LRCLK} = 48kHz$, MAS = 0, 20-bit source data. $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
PARAMETRIC EQUALIZER							
Number of Bands			7			Bands	
Per Band Gain Range			-12	12		dB	
Pre-Attenuator Gain Range			-15	0		dB	
Pre-Attenuator Step Size			1			dB	
Minimum Cutoff Frequency		High Pass Filter	0.0008 $\times f_s$	Hz			
		High Frequency Shelving Filter	0.02 $\times f_s$				
		Low Pass Filter	0.002 $\times f_s$				
		Low Frequency Shelving Filter	0.0008 $\times f_s$				
		Peak Filter	0.0008 $\times f_s$				
Maximum Q		Peak Filter	10				
DAC TO RECEIVER AMPLIFIER PATH							
Dynamic Range (Note 4)	DR	$f_s = 48kHz$, $f_{MCLK} = 12.288MHz$	100			dB	
Total Harmonic Distortion + Noise	THD+N	$f = 1kHz$, $P_{OUT} = 20mW$, $R_{REC} = 32\Omega$	-68	-58		dB	
ANALOG INPUT TO RECEIVER AMPLIFIER PATH							
Dynamic Range (Note 4)	DR		93	96		dB	
Total Harmonic Distortion + Noise	THD+N		-71			dB	
Power Supply Rejection Ratio (Note 12)	PSRR	$SPKLVDD = 2.8V$ to $5.5V$	72	80	dB		
		$V_{RIPPLE} = 100mV_{P-P}$	$f = 217Hz$	77			
			$f = 1kHz$	77			
			$f = 10kHz$	69			
RECEIVER AMPLIFIER (Note 7)							
Output Power	P_{OUT}	$R_{REC} = 32\Omega$, $f = 1kHz$, THD < 1%, VCM_MODE = 0	97		mW		
		$R_{REC} = 32\Omega$, $f = 1kHz$, THD < 1%, VCM_MODE = 1	74				
Full Scale Output		$A_{V_RECPGA} = 0dB$ (Note 8)	1			V_{RMS}	
Receiver Volume Control (PGA)	A_{V_RECPGA}	Note 5 and Note 13	$RCVLVOL = 0x00$	-63	-61	-59	dB
			$RCVLVOL = 0x1F$	+7.5	+8	+8.5	
Volume Control Step Size (Note 13)		+8dB to +6dB	0.5	dB			
		+6dB to +0dB	1				
		0dB to -14dB	2				
		-14dB to -38dB	3				
		-38dB to -62dB	4				
Mute Attenuation		$f = 1kHz$	88	97		dB	
Output Offset Voltage	V_{OS}	$A_{V_REC} = -62dB$, $T_A = 25^\circ C$		± 1		mV	
Click and Pop Level	K_{CP}	Peak Voltage, A-weighted, 32 samples per second, $A_{V_REC} = 0dB$	Into shutdown	-67		dBV	
			Out of shutdown	-68			
Capacitive Drive Capability		No sustained oscillations	$R_L = 32\Omega$	500		pF	
			$R_L = \infty$	100			

($V_{AVDD} = V_{HPVDD} = V_{DVDD} = +1.8V$, $V_{DVDD} = 1.2V$, $V_{SPKLVDD} = V_{SPKVDD} = 3.7V$). Receiver load (R_{REC}) connected between RECP/LOUTL and RECN/LOUTR (LINMOD=0). Line Output loads (R_{LOUT}) connected between RECP/LOUTL and RECN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. $R_{REC} = \infty$, $R_{LOUT} = \infty$, $R_{HP} = \infty$, $Z_{SPK} = \infty$. $C_{REF} = 2.2\mu F$, $C_{VCM} = C_{MICBIAS} = 1\mu F$, $C_{CIN-CIP} = C_{CPVDD} = C_{CPVSS} = 1\mu F$. $A_{V_MICPRE_} = A_{V_MICPGA_} = A_{V_LINEPGA_} = 0dB$, $A_{V_ADCLVL} = A_{V_ADCGAIN} = 0dB$, $A_{V_DACLVL} = A_{V_DAGAIN} = 0dB$, $A_{V_MIXGAIN} = 0dB$, $A_{V_REC} = A_{V_LOUT}$, $A_{V_HP} = A_{V_SPK} = 0dB$. $f_{MCLK} = 12.288MHz$, $f_{RCLK} = 48kHz$, MAS = 0, 20-bit source data. $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
DAC TO LINEOUT AMPLIFIER PATH							
Dynamic Range (Note 4)	DR	$f_s = 48kHz$, $f_{MCLK} = 12.288MHz$	100			dB	
Total Harmonic Distortion + Noise	THD+N	$f = 1kHz$, $R_{LOUT} = 10k\Omega$ (0.707V _{RMS} Output Level)	-86	-70		dB	
ANALOG INPUT TO LINE OUT AMPLIFIER PATH							
Dynamic Range (Note 4)	DR		98			dB	
Total Harmonic Distortion + Noise	THD+N	$f = 1kHz$, $R_{LOUT} = 10k\Omega$ (0.707V _{RMS} Output Level)	-86			dB	
Power Supply Rejection Ratio (Note 12)	PSRR	$V_{SPK_VDD} = 2.8V$ to $5.5V$	60	74		dB	
		$V_{RIPPLE} = 100mV_{P-P}$	$f = 217Hz$	74			
			$f = 1kHz$	74			
			$f = 10kHz$	73			
LINE OUT AMPLIFIER (Note 7)							
Full Scale Output		$A_{V_LOUT} = 0dB$ (Note 8)	0.707			V _{RMS}	
Line Output Amplifier Gain	$A_{V_LOUTAMP}$			-3		dB	
Line Output Volume Control (PGA)	$A_{V_LOUTPGA}$	Note 5 and Note 13	$RCV_VOL = 0x00$	-63	-61	-59	dB
			$RCV_VOL = 0x1F$	+7.5	+8	+8.5	
Volume Control Step Size (Note 13)		$+8dB$ to $+6dB$		0.5		dB	
		$+6dB$ to $+0dB$		1			
		$0dB$ to $-14dB$		2			
		$-14dB$ to $-38dB$		3			
		$-38dB$ to $-62dB$		4			
Mute Attenuation		$f = 1kHz$	88	97		dB	
Capacitive Drive Capability		No sustained oscillations	$R_{LOUT} = 1k\Omega$	500		pF	
			$R_{LOUT} = \infty$	100			
DAC TO SPEAKER AMPLIFIER PATH							
Dynamic Range (Note 4)	DR	$A_{V_SPK} = 0 dB$	96			dB	
Total Harmonic Distortion + Noise	THD+N	$f = 1kHz$, $P_{OUT} = 200mW$, $Z_{SPK} = 8\Omega + 68\mu H$, $f_{MCLK} = 12.288MHz$	-73			dB	
Crosstalk		SPL to SPR and SPR to SPL, $P_{OUT} = 640mW$, $f = 1kHz$	-108				
Output Noise		$A_{V_SPK} = 0dB$	27			μV_{RMS}	
ANALOG INPUT TO SPEAKER AMPLIFIER PATH							
Dynamic Range (Note 4)	DR	$A_{V_MIC} = 0dB$ $A_{V_SPK} = 0 dB$ (Output referenced to 2Vrms)	94			dB	
Total Harmonic Distortion + Noise	THD+N	$f = 1kHz$, $P_{OUT} = 200mW$, $Z_{SPK} = 8\Omega + 8\mu H$	-73			dB	
Output Noise			28			μV_{RMS}	
Power Supply Rejection Ratio (Note 12)	PSRR	$V_{SPK_VDD} = 2.8V$ to $5.5V$	60	80		dB	
		$V_{RIPPLE} = 100mV_{P-P}$	$f = 217Hz$	68			
			$f = 1kHz$	67			
			$f = 10kHz$	61			

($V_{AVDD} = V_{HPVDD} = V_{DVDD} = +1.8V$, $V_{DVDD} = 1.2V$, $V_{SPKLVDD} = V_{SPKRVDD} = V_{SPKVDD} = 3.7V$). Receiver load (R_{REC}) connected between RECP/LOUTL and RECN/LOUTR (LINMOD=0). Line Output loads (R_{LOUT}) connected between from RECP/LOUTL and RECN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. $R_{REC} = \infty$, $R_{LOUT} = \infty$, $R_{HP} = \infty$, $Z_{SPK} = \infty$. $C_{REF} = 2.2\mu F$, $C_{VCM} = C_{MICBIAS} = 1\mu F$, $C_{CIN-CIP} = C_{CPVDD} = C_{CPVSS} = 1\mu F$. $A_{V_MICPRE_} = A_{V_MICPGA_} = A_{V_LINEPGA_} = 0dB$, $A_{V_ADCLVL} = A_{V_ADCGAIN} = 0dB$, $A_{V_DACLVL} = A_{V_DAGAIN} = 0dB$, $A_{V_MIXGAIN} = 0dB$, $A_{V_REC} = A_{V_LOUT}$, $A_{V_HP} = A_{V_SPK} = 0dB$. $f_{MCLK} = 12.288MHz$, $f_{RCLK} = 48kHz$, MAS = 0, 20-bit source data. $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
SPEAKER AMPLIFIER (Note 7)							
Output Power	P_{OUT}	$f = 1kHz$, THD < 1%, $Z_{SPK} = 8\Omega + 68\mu H$	SPK_VDD = 4.2V	950		mW	
			SPK_VDD = 3.7V	730			
			SPK_VDD = 3.3V	580			
			SPK_VDD = 3.0V	400			
Full Scale Output		$A_{V_SPK} = +6dB$ (Note 8)		2		V_{RMS}	
Speaker Output Amplifier Gain	A_{V_SPKAMP}			+6		dB	
Speaker Volume Control (PGA)	A_{V_SPKPGA}	Note 5 and Note 13	SPVOL_ = 0x00	-50	-48	-46	dB
			SPVOL_ = 0x1F	+13.5	+14	+14.5	
Volume Control Step Size (Note 13)		+14dB to +9dB		0.5		dB	
		+9dB to -6dB		1			
		-6dB to -14dB		2			
		-14dB to -32dB		3			
		-32dB to -48dB		4			
Mute Attenuation		$f = 1kHz$		84		dB	
Output Offset Voltage	V_{OS}	$A_{V_SPKPGA} = -62dB$		± 0.5	± 3	mV	
Click and Pop Level	K_{CP}	Peak Voltage, A-weighted, 32 samples per second, $A_{V_SPK} = 0dB$	Into shutdown	-65		dBV	
			Out of shutdown	-65			
DAC TO HEADPHONE AMPLIFIER PATH							
Dynamic Range (Note 4)	DR	$f_s = 48kHz$, $f_{MCLK} = 12.288MHz$	Master or Slave Mode	102		dB	
			Slave Mode	96			
Total Harmonic Distortion + Noise	THD+N	$f = 1kHz$, $P_{OUT} = 10mW$	$R_{HP} = 16\Omega$	-88	-80	dB	
			$R_{HP} = 32\Omega$	-86			
		$f = 1kHz$, $V_{OUT} = 1V_{RMS}$, $R_{HP} = 10k\Omega$		-88			
Crosstalk		$f = 1kHz$, $V_{IN} = -1dBFS$, $R_{HP} = 10k\Omega$		TBD		dB	
		HPL to HPR and HPR to HPL, $P_{OUT} = 5mW$, $f = 1kHz$, $R_{HP} = 32\Omega$		TBD		dB	
Power Supply Rejection Ratio (Note 12)	PSRR	$V_{AVDD} = V_{HPVDD} = 1.65V$ to $2.0V$		70	85	dB	
		$V_{RIPPLE} = 100mV_{P-P}$, $A_{V_HP} = 0dB$	$f = 217Hz$	79			
			$f = 1kHz$	79			
			$f = 10kHz$	74			
DAC Path Phase Delay		1kHz, 0dB input, High pass filter disabled measured from digital input to analog output	MODE = 0 (IIR Voice); 8kHz	2.2		ms	
			MODE = 0 (IIR Voice); 16kHz	1.1			
			MODE = 1 (FIR Audio) 8kHz	2.5			
			MODE = 1 (FIR Audio) 48kHz	0.76			
Gain Error				1	5	%	
Channel Gain Mismatch				1		%	

($V_{AVDD} = V_{HPVDD} = V_{DVDD} = +1.8V$, $V_{DVDD} = 1.2V$, $V_{SPKLVDD} = V_{SPKRVDD} = V_{SPKVDD} = 3.7V$). Receiver load (R_{REC}) connected between RECP/LOUTL and RECN/LOUTR (LINMOD=0). Line Output loads (R_{LOUT}) connected between from RECP/LOUTL and RECN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. $R_{REC} = \infty$, $R_{LOUT} = \infty$, $R_{HP} = \infty$, $Z_{SPK} = \infty$. $C_{REF} = 2.2\mu F$, $C_{VCM} = C_{MICBIAS} = 1\mu F$, $C_{CIN-CIP} = C_{CPVDD} = C_{CPVSS} = 1\mu F$. $A_{V_MICPRE_} = A_{V_MICPGA_} = A_{V_LINEPGA_} = 0dB$, $A_{V_ADCLVL} = A_{V_ADCGAIN} = 0dB$, $A_{V_DACLVL} = A_{V_DAGAIN} = 0dB$, $A_{V_MIXGAIN} = 0dB$, $A_{V_REC} = A_{V_LOUT}$, $A_{V_HP} = A_{V_SPK} = 0dB$. $f_{MCLK} = 12.288MHz$, $f_{LRCLK} = 48kHz$, MAS = 0, 20-bit source data. $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
ANALOG INPUT TO HEADPHONE AMPLIFIER PATH							
Dynamic Range (Note 4)		$A_{V_LINE} = 0dB$ $A_{V_HPPGA} = 0dB$	101				
Total Harmonic Distortion + Noise	THD+N	$V_{IN} = 250mV_{RMS}$, $f = 1kHz$	-80			dB	
Power Supply Rejection Ratio (Note 12)	PSRR	$V_{AVDD} = V_{HPVDD} = 1.65V$ to $2.0V$	40	60		dB	
		$V_{RIPPLE} = 100mV_{P-P}$, $A_{V_TOTAL} = 0dB$	$f = 217Hz$	61			
			$f = 1kHz$	61			
			$f = 10kHz$	60			
HEADPHONE AMPLIFIER (Note 7)							
Output Power	P_{OUT}	$f = 1kHz$, THD < 1%	$R_L = 16\Omega$	20	40	mW	
			$R_L = 32\Omega$	30			
Total Harmonic Distortion + Noise	THD +N	$R_{HP} = 16\Omega$, $P_{OUT} = 10mW$, $f = 1kHz$	-88	-80		dB	
		$R_{HP} = 10k\Omega$, $V_{OUT} = 1V_{rms}$, $f = 1kHz$	-88				
Full Scale Output		$AV_{HP} = 0dB$ (Note 8)	1			V_{RMS}	
Headphone Volume Control (PGA)	A_{V_HPPGA}		$HPVOL_ = 0x00$	-69	-67	-65	dB
			$HPVOL_ = 0x1F$	2.5	3	3.5	
Volume Control Step Size (Note 13)		+3dB to +1dB	0.5			dB	
		+1dB to -5dB	1				
		-5dB to -19dB	2				
		-19dB to -43dB	3				
		-43dB to -67dB	4				
Mute Attenuation		$f = 1kHz$	110			dB	
Output Offset Voltage	V_{OS}	$A_{V_HP} = -67dB$	$T_A = +25^\circ C$	± 0.5	± 1	mV	
			$T_A = T_{MIN}$ to T_{MAX}		± 3		
Crosstalk		HPL to HPR and HPR to HPL, $P_{OUT} = 5mW$, $f = 1kHz$, $R_{HP} = 32\Omega$	TBD			dB	
Capacitive Drive Capability		No sustained oscillations	$R_{HP} = 32\Omega$	500		pF	
			$R_{HP} = \infty$	100			
Click and Pop Level	K_{CP}	Peak Voltage, A-weighted, 32 samples per second, $A_{V_HP} = -67dB$	Into shutdown	-73		dBV	
			Out of shutdown	-73			
JACK DETECTION							
JACKSNS High Threshold	V_{TH_HIGH}	MICBIAS Enabled	$0.92 \times V_{MICBIAS}$	$0.95 \times V_{MICBIAS}$	$0.98 \times V_{MICBIAS}$	V	
		MICBIAS Disabled	$0.92 \times V_{SPKLVDD}$	$0.95 \times V_{SPKLVDD}$	$0.98 \times V_{SPKLVDD}$		
JACKSNS Low Threshold	V_{TH_LOW}	MICBIAS Enabled	$0.06 \times V_{MICBIAS}$	$0.10 \times V_{MICBIAS}$	$0.17 \times V_{MICBIAS}$	V	
		MICBIAS Disabled	$0.06 \times V_{SPKLVDD}$	$0.10 \times V_{SPKLVDD}$	$0.17 \times V_{SPKLVDD}$		
JACKSNS Sense Voltage	V_{SENSE}	MICBIAS Disabled			$V_{SPKLVDD}$	V	
JACKSNS Strong Pull-up Resistance	R_{SPU}	MICBIAS Disabled, JDWK = 0	TBD	2.3	TBD	k Ω	
JACKSNS Weak Pull-up Current	I_{WPu}	MICBIAS Disabled, JDWK = 1	2.5	5	12	μA	
JACKSNS Glitch Debounce Period	t_{GLITCH}	JDEB = 00		25		ms	
		JDEB = 11		200			

DIGITAL INPUT/OUTPUT CHARACTERISTICS

($V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = +1.8V$, $V_{DVDD} = 1.2V$, $V_{SPKLVDD} = V_{SPKRVDD} = V_{SPKVDD} = 3.7V$. Receiver load (R_{REC}) connected between RECP/LOUTL and RECN/LOUTR (LINMOD=0). Line Output loads (R_{LOUT}) connected between from RECP/LOUTL and RECN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. $R_{REC} = \infty$, $R_{LOUT} = \infty$, $R_{HP} = \infty$, $Z_{SPK} = \infty$. $C_{REF} = 2.2\mu F$, $C_{VCM} = C_{MICBIAS} = 1\mu F$, $C_{C1N-C1P} = C_{CPVDD} = C_{CPVSS} = 1\mu F$. $A_{V_MICPRE} = A_{V_MICPGA} = A_{V_LINEPGA} = 0dB$, $A_{V_ADCLVL} = A_{V_ADCGAIN} = 0dB$, $A_{V_DACLVL} = A_{V_DAGAIN} = 0dB$, $A_{V_MIXGAIN} = 0dB$, $A_{V_REC} = A_{V_LOUT}$, $A_{V_HP} = A_{V_SPK} = 0dB$. $f_{MCLK} = 12.288MHz$, $f_{RCLK} = 48kHz$, MAS = 0, 20-bit source data. $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MCLK						
Input High Voltage	V_{IH}		1.2			V
Input Low Voltage	V_{IL}			0.6		V
Input Leakage Current	I_{IH}, I_{IL}	$V_{DVDDIO} = 2.0V$, $V_{IN} = 0V, 5.5V$, $T_A = +25^\circ C$	-1	1		μA
Input Capacitance				10		pF
SDIN, BCLK, LRCLK - INPUT						
Input High Voltage	V_{IH}	$V_{DVDDIO} = 1.65V$	$0.7 \times V_{DVDDIO}$			V
Input Low Voltage	V_{IL}	$V_{DVDDIO} = 1.65V$		$0.3 \times V_{DVDDIO}$		V
Input Hysteresis				125		mV
Input Leakage Current	I_{IH}, I_{IL}	$V_{DVDDIO} = 3.6V$, $V_{IN} = 0V, 3.6V$, $T_A = +25^\circ C$	-1	1		μA
Input Capacitance				10		pF
BCLK, LRCLK, SDOUT - OUTPUT						
Output High Voltage	V_{OH}	$V_{DVDDIO} = 1.65V$, $I_{OH} = 3mA$	$V_{DVDDIO} - 0.4$			V
Output Low Voltage	V_{OL}	$V_{DVDDIO} = 1.65V$, $I_{OL} = 3mA$		0.4		V
Input Leakage Current	I_{IH}, I_{IL}	$V_{DVDDIO} = 2.0V$, $V_{IN} = 0V, 5.5V$, $T_A = +25^\circ C$, High-Z State	-1	1		μA
SDA, SCL - INPUT						
Input High Voltage	V_{IH}	$V_{DVDDIO} = 1.65V$	$0.7 \times V_{DVDDIO}$			V
Input Low Voltage	V_{IL}	$V_{DVDDIO} = 1.65V$		$0.3 \times V_{DVDDIO}$		V
Input Hysteresis				100		mV
Input Leakage Current	I_{IH}, I_{IL}	$V_{DVDDIO} = 2.0V$, $V_{IN} = 0V, 5.5V$, $T_A = +25^\circ C$	-1	1		μA
Input Capacitance				10		pF
SDA, /IRQ1 - OUTPUT						
Output Low Voltage	V_{OL}	$V_{DVDDIO} = 1.65V$, $I_{OH} = 3mA$		$0.2 \times V_{DVDDIO}$		V
Output High Current	I_{OH}	$V_{DVDDIO} = 1.65V$, $I_{OL} = 3mA$		1		μA
DIGMICDATA - INPUT						
Input High Voltage	V_{IH}	$V_{DVDDIO} = 1.65V$	$0.65 \times V_{DVDDIO}$			V
Input Low Voltage	V_{IL}	$V_{DVDDIO} = 1.65V$		$0.35 \times V_{DVDDIO}$		V
Input Hysteresis				100		mV
Input Leakage Current	I_{IH}, I_{IL}	$V_{DVDDIO} = 2.0V$, $V_{IN} = 0V, 5.5V$, $T_A = +25^\circ C$	-25	25		μA
Input Capacitance				10		pF

($V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = +1.8V$, $V_{DVDD} = 1.2V$, $V_{SPKLVDD} = V_{SPKRVDD} = V_{SPKVDD} = 3.7V$. Receiver load (R_{REC}) connected between RECP/LOUTL and RECN/LOUTR (LINMOD=0). Line Output loads (R_{LOUT}) connected between RECP/LOUTL and RECN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. $R_{REC} = \infty$, $R_{LOUT} = \infty$, $R_{HP} = \infty$, $Z_{SPK} = \infty$. $C_{REF} = 2.2\mu F$, $C_{VCM} = C_{MICBIAS} = 1\mu F$, $C_{C1N-C1P} = C_{CPVDD} = C_{CPVSS} = 1\mu F$. $A_{V_MICPRE_} = A_{V_MICPGA_} = A_{V_LINEPGA_} = 0dB$, $A_{V_ADCLVL} = A_{V_ADCAGAIN} = 0dB$, $A_{V_DACLVL} = A_{V_DACAGAIN} = 0dB$, $A_{V_MIXGAIN} = 0dB$, $A_{V_REC} = A_{V_LOUT}$, $A_{V_HP} = A_{V_SPK} = 0dB$. $f_{MCLK} = 12.288MHz$, $f_{LRCLK} = 48kHz$, MAS = 0, 20-bit source data. $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGMICCLK - INPUT						
Input High Voltage	V_{IH}	$V_{DVDDIO} = 1.65V$	$0.65 \times V_{DVDDIO}$			V
Input Low Voltage	V_{IL}	$V_{DVDDIO} = 1.65V$		$0.35 \times V_{DVDDIO}$		V
Input Hysteresis				100		mV
Input Capacitance				10		pF
DIGMICCLK - OUTPUT						
Output High Voltage	V_{OH}	$V_{DVDDIO} = 1.65V$, $I_{OH} = 3mA$	$V_{DVDDIO} - 0.4$			V
Output Low Voltage	V_{OL}	$V_{DVDDIO} = 1.65V$, $I_{OL} = 3mA$			0.4	V

INPUT CLOCK CHARACTERISTICS

($V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = +1.8V$, $V_{DVDD} = 1.2V$, $V_{SPKLVDD} = V_{SPKRVDD} = V_{SPKVDD} = 3.7V$. Receiver load (R_{REC}) connected between RECP/LOUTL and RECN/LOUTR (LINMOD=0). Line Output loads (R_{LOUT}) connected between RECP/LOUTL and RECN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. $R_{REC} = \infty$, $R_{LOUT} = \infty$, $R_{HP} = \infty$, $Z_{SPK} = \infty$. $C_{REF} = 2.2\mu F$, $C_{VCM} = C_{MICBIAS} = 1\mu F$, $C_{C1N-C1P} = C_{CPVDD} = C_{CPVSS} = 1\mu F$. $A_{V_MICPRE_} = A_{V_MICPGA_} = A_{V_LINEPGA_} = 0dB$, $A_{V_ADCLVL} = A_{V_ADCAGAIN} = 0dB$, $A_{V_DACLVL} = A_{V_DACAGAIN} = 0dB$, $A_{V_MIXGAIN} = 0dB$, $A_{V_REC} = A_{V_LOUT}$, $A_{V_HP} = A_{V_SPK} = 0dB$. $f_{MCLK} = 12.288MHz$, $f_{LRCLK} = 48kHz$, MAS = 0, 20-bit source data. $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

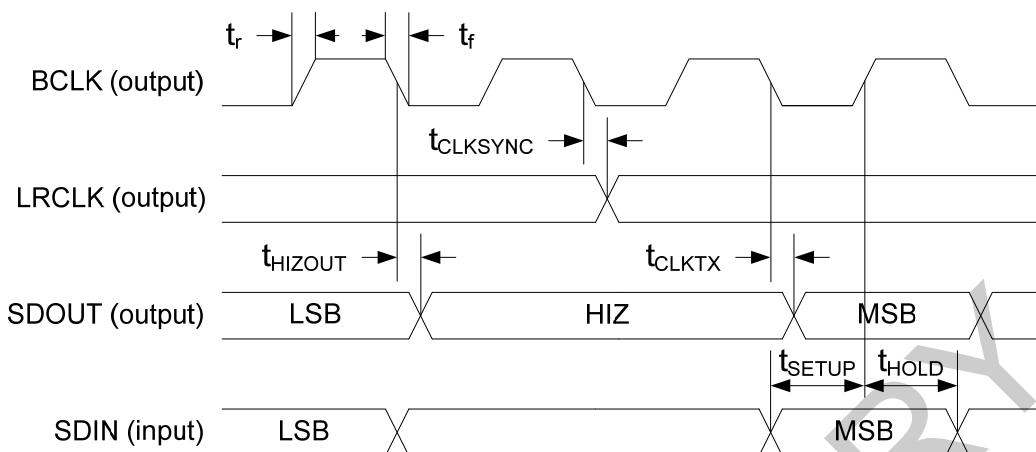
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CLOCK CHARACTERISTICS						
MCLK Input Frequency	f_{MCLK}		2.048		60	MHz
MCLK Input Duty Cycle		PSCLK = 01	40	50	60	%
		PSCLK = 10 or 11	30		70	
Maximum MCLK Input Jitter				1		ns
LRCLK Sample Rate (Note 9)	f_{LRCLK}	DHF = 0	8	48		kHz
		DHF = 1	48	96		
DAI LRCLK average frequency error (Note 10)		FREQ = 0x8 to 0xF	0	0		%
		FREQ = 0x0	-0.025	0.025		
PLL Lock Time			Rapid Lock Mode	2	7	ms
			Non-Rapid Lock Mode	12	25	
Maximum LRCLK input jitter to maintain PLL lock					± 100	ns
Soft Start / Stop Time				10		ms

DIGITAL AUDIO INTERFACE TIMING CHARACTERISTICS

($V_{AVDD} = V_{HPVDD} = V_{DVDD} = +1.8V$, $V_{SPKLVDD} = V_{SPKRVDD} = V_{SPKVDD} = 3.7V$). Receiver load (R_{REC}) connected between RECP/LOUTL and RECN/LOUTR (LINMOD=0). Line Output loads (R_{LOUT}) connected between RECP/LOUTL and RECN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. $R_{REC} = \infty$, $R_{LOUT} = \infty$, $R_{HP} = \infty$, $Z_{SPK} = \infty$. $C_{REF} = 2.2\mu F$, $C_{VCM} = C_{MICBIAS} = 1\mu F$, $C_{C1N-C1P} = C_{CPVDD} = C_{CPVSS} = 1\mu F$. $A_{V_MICPRE} = A_{V_MICPGA} = A_{V_LINEPGA} = 0dB$, $A_{V_ADCLVL} = A_{V_ADCAGAIN} = 0dB$, $A_{V_DACLVL} = A_{V_DACGAIN} = 0dB$, $A_{V_MIXGAIN} = 0dB$, $A_{V_REC} = A_{V_LOUT}$, $A_{V_HP} = A_{V_SPK} = 0dB$. $f_{MCLK} = 12.288MHz$, $f_{RCLK} = 48kHz$, MAS = 0, 20-bit source data. $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL AUDIO INTERFACE TIMING CHARACTERISTICS						
BCLK Cycle Time	t_{BCLK}	Slave Mode	80			ns
BCLK High Time	t_{BCLKH}	Slave Mode	20			ns
BCLK Low Time	t_{BCLKL}	Slave Mode	20			ns
BCLK or LRCLK Rise and Fall Time	t_r, t_f	Master Mode, $C_L = 15pF$		5		ns
SDIN to BCLK Set-Up Time	t_{SETUP}		20			ns
LRCLK to BCLK Set-Up Time	$t_{SYNCSET}$	Slave Mode	20			ns
SDIN to BCLK Hold Time	t_{HOLD}		20			ns
LRCLK to BCLK Hold Time	$t_{SYNCHOLD}$	Slave Mode	20			ns
Minimum delay time from LSB BCLK falling edge to Hi-Z state	t_{HIZOUT}	Master Mode	TDM = 1	20		ns
			TDM = 1, FSW = 1	20		
			TDM = 1, FSW = 0	20		
			TDM = 0, DLY = 1	20		
LRCLK rising edge to SDOUT MSB Delay	t_{SYNCTX}	$C = 30pF$, TDM = 1, FSW = 1			TBD	ns
BCLK to SDOUT Delay	t_{CLKTX}	$C = 30pF$	TDM = 1, BCLK rising edge		TBD	ns
			TDM = 0		TBD	
SDOUT valid time before opposite BCLK edge	$t_{VALIDPRE}$			20		ns
SDOUT valid time after opposite BCLK edge	$t_{VALIDPOST}$			20	150	ns
Delay Time from BCLK to LRCLK	$t_{CLKSYNC}$	Master Mode	TDM = 1	-15	15	ns
			TDM = 0		$0.8 \times t_{BCLK}$	

Master Mode



Slave Mode

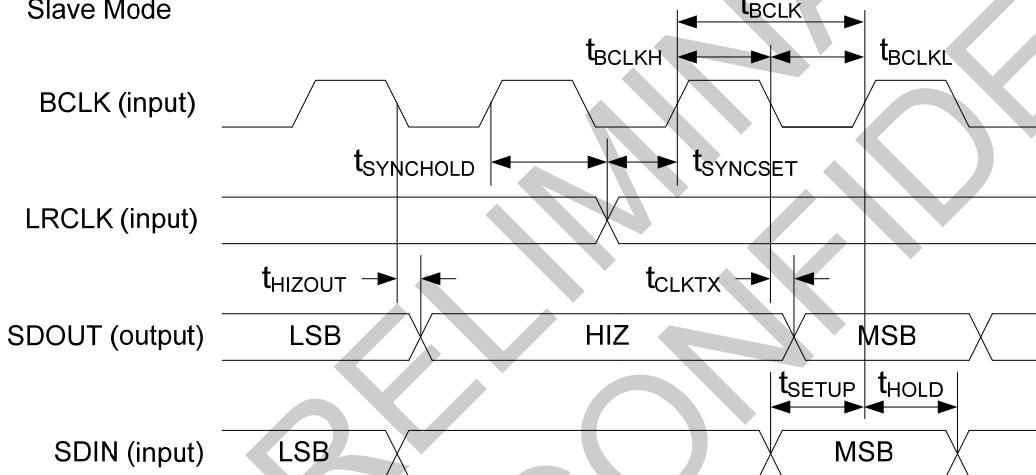


Figure 1: I2S Audio Interface Timing Diagrams (TDM = 0)

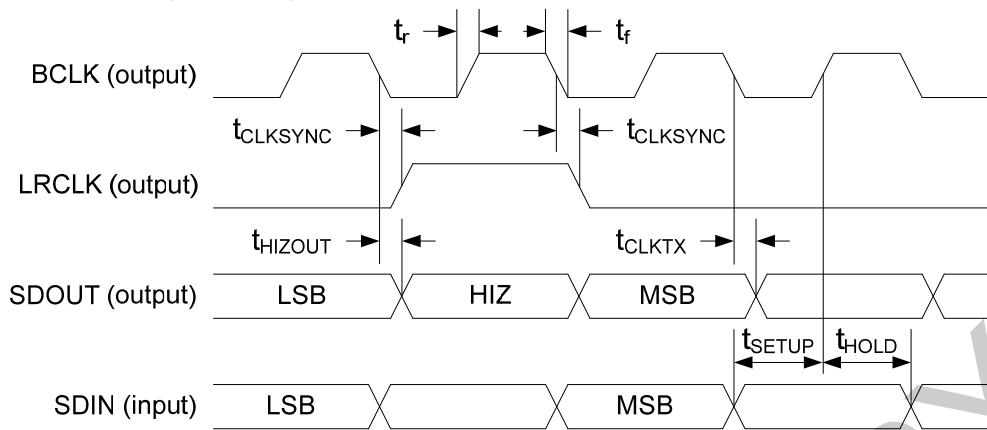
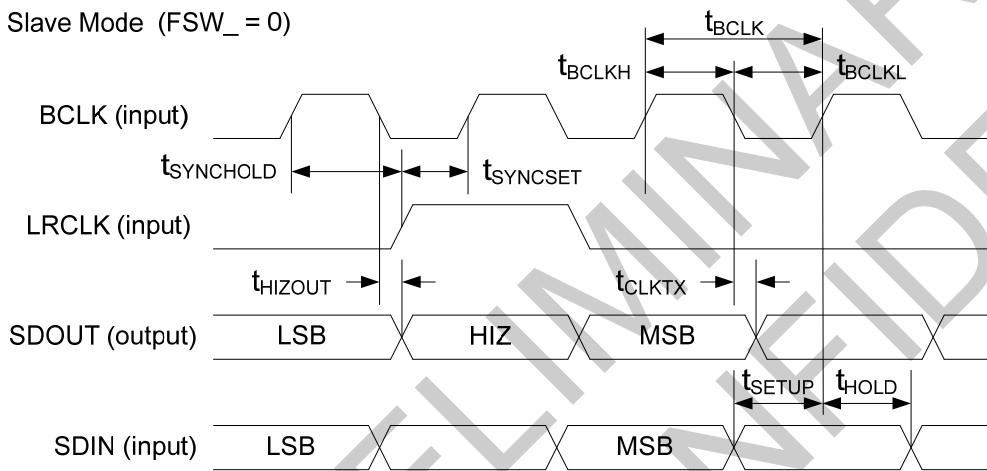
Master Mode ($\text{FSW}_- = 0$)Slave Mode ($\text{FSW}_- = 0$)

Figure 2: TDM Audio Interface Short Mode Timing Diagram (TDM = 1)

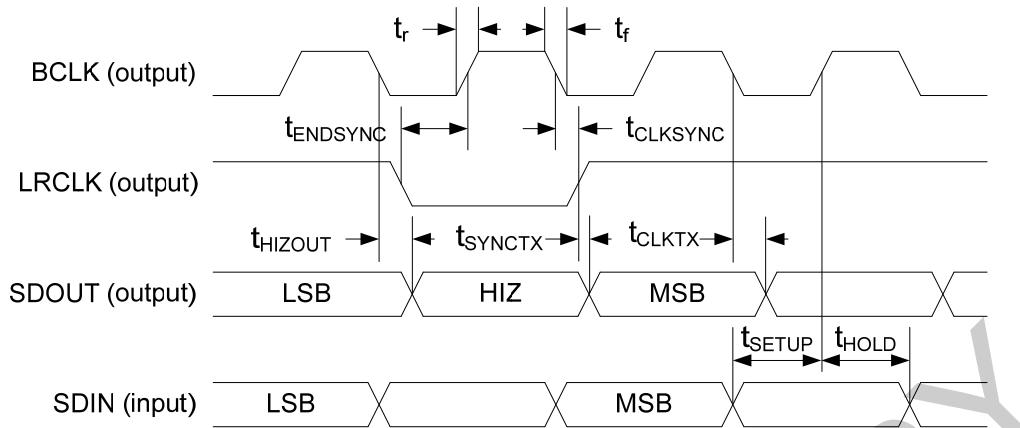
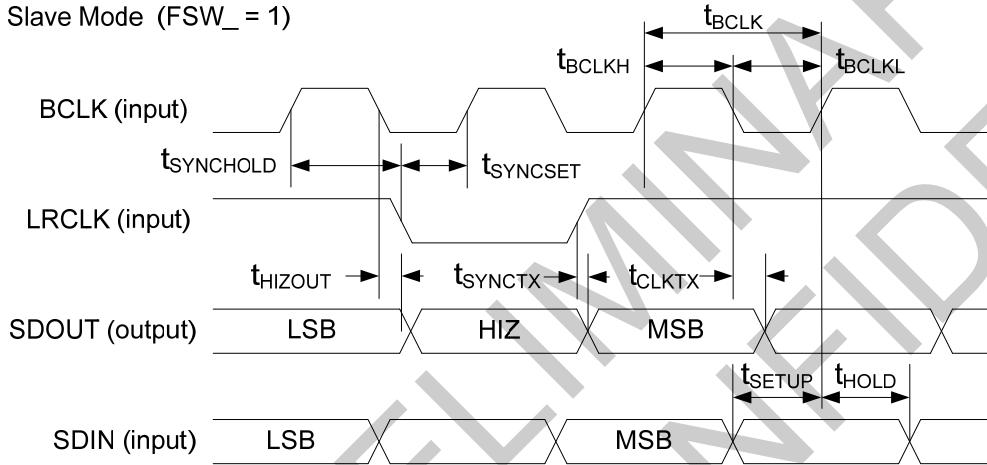
Master Mode ($\text{FSW}_- = 1$)Slave Mode ($\text{FSW}_- = 1$)

Figure 3: TDM Long Mode Timing Diagram (TDM = 1)

I²C TIMING CHARACTERISTICS

($V_{AVDD} = V_{HPVDD} = V_{DVDDIO} = +1.8V$, $V_{DVDD} = 1.2V$, $V_{SPKLVDD} = V_{SPKVDD} = 3.7V$). Receiver load (R_{REC}) connected between RECP/LOUTL and RECN/LOUTR (LINMOD=0). Line Output loads (R_{LOUT}) connected between RECP/LOUTL and RECN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. $R_{REC} = \infty$, $R_{LOUT} = \infty$, $R_{HP} = \infty$, $Z_{SPK} = \infty$. $C_{REF} = 2.2\mu F$, $C_{VCM} = C_{MICBIAS} = 1\mu F$, $C_{C1N-C1P} = C_{CPVDD} = C_{CPVSS} = 1\mu F$. $A_{V_MICPRE_} = A_{V_MICPGA_} = A_{V_LINEPGA_} = 0dB$, $A_{V_ADCLVL} = A_{V_ADCGAIN} = 0dB$, $A_{V_DACLVL} = A_{V_DAGAIN} = 0dB$, $A_{V_MIXGAIN} = 0dB$, $A_{V_REC} = A_{V_LOUT}$, $A_{V_HP} = A_{V_SPK} = 0dB$. $f_{MCLK} = 12.288MHz$, $f_{LRCLK} = 48kHz$, MAS = 0, 20-bit source data. $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C TIMING CHARACTERISTICS						
Serial Clock Frequency	f_{SCL}	Guaranteed by SCL Pulse-Width Low and High	0	400	400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			μs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			μs
SCL Pulse-Width Low	t_{LOW}		1.3			μs
SCL Pulse-Width High	t_{HIGH}		0.6			μs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			μs
Data Hold Time	$t_{HD,DAT}$	$R_{PU} = 475\Omega$, $C_B = 100pF$, $400pF$	0	900		ns
		Transmitting	0	900		
		Receiving		0		
Data Setup Time	$t_{SU,STA}$		100			ns
SDA and SCL Receiving Rise Time	t_R	Note 11	$20 + 0.1 \times C_B$	300		ns
SDA and SCL Receiving Fall Time	t_F	Note 11	$20 + 0.1 \times C_B$	300		ns
SDA Transmitting Fall Time	t_F	$R_{PU} = 475\Omega$, $C_B = 100pF$ to $400pF$, Note 11	$20 + 0.1 \times C_B$	250		ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			μs
Bus Capacitance	C_B	Guaranteed by SDA Transmitting Fall Time		400		pF
Pulse Width of Suppressed Spike	t_{SP}		0	50		ns

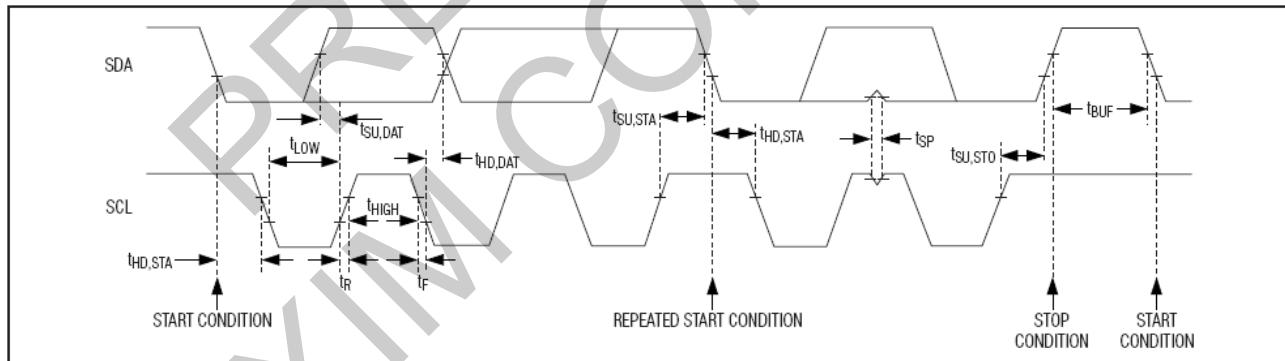


Figure 4: I²C Interface Timing Diagram

DIGITAL MICROPHONE TIMING CHARACTERISTICS

($V_{AVDD} = V_{HPVDD} = V_{DVDD} = +1.8V$, $V_{SPKVDD} = V_{SPKLVDD} = 1.2V$, $V_{SPKRVDD} = V_{SPKVDD} = 3.7V$). Receiver load (R_{REC}) connected between RECP/LOUTL and RECN/LOUTR (LINMOD=0). Line Output loads (R_{LOUT}) connected between RECP/LOUTL and RECN/LOUTR to GND (LINMOD = 1). Headphone loads (R_{HP}) connected from HPL or HPR to GND. Speaker loads (Z_{SPK}) connected between SPK_P and SPK_N. $R_{REC} = \infty$, $R_{LOUT} = \infty$, $R_{HP} = \infty$, $Z_{SPK} = \infty$. $C_{REF} = 2.2\mu F$, $C_{VCM} = C_{MICBIAS} = 1\mu F$, $C_{C1N-C1P} = C_{CPVDD} = C_{CPVSS} = 1\mu F$. $A_{V_MICPRE} = A_{V_MICPGA} = A_{V_LINEPGA} = 0dB$, $A_{V_ADCLVL} = A_{V_ADCAGAIN} = 0dB$, $A_{V_DACLVL} = A_{V_DACGAIN} = 0dB$, $A_{V_MIXGAIN} = 0dB$, $A_{V_REC} = A_{V_LOUT}$, $A_{V_HP} = A_{V_SPK} = 0dB$. $f_{MCLK} = 12.288MHz$, $f_{LRCLK} = 48kHz$, MAS = 0, 20-bit source data. $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL MICROPHONE TIMING CHARACTERISTICS						
DIGMICCLK Frequency	$f_{DIGMICCLK}$	$f_{MCLK} = 12.288MHz$	$MICCLK = 000$	$f_{PCLK}/2$	MHz	
			$MICCLK = 001$	$f_{PCLK}/3$		
			$MICCLK = 010$	$f_{PCLK}/4$		
			$MICCLK = 011$	$f_{PCLK}/5$		
			$MICCLK = 100$	$f_{PCLK}/6$		
			$MICCLK = 101$	$f_{PCLK}/8$		
			$MICCLK = 110$	$f_{PCLK}/10$		
DIGMICDATA to DIGMICCLK Set-Up Time	$t_{SU,MIC}$	Either clock edge	20		ns	
DIGMICDATA to DIGMICCLK Hold Time	$t_{HD,MIC}$	Either clock edge	0		ns	

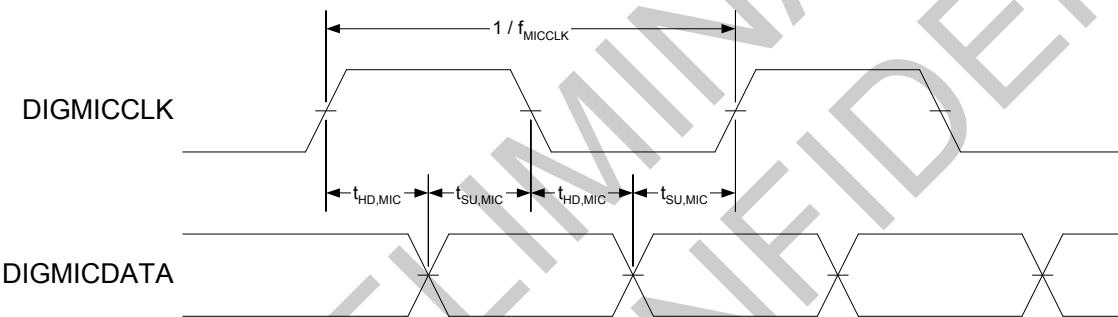


Figure 5: Digital Microphone Timing Diagram

Note 1: The MAX98090 is 100% production tested at $T_A = +25^\circ C$. Specifications over temperature limits are guaranteed by design.

Note 2: Analog Supply Current = $AVDD + HPVDD$, Speaker Supply Current = $SPKLVDD + SPKRVDD$, and Digital Supply Current = $DVDD + DVDDIO$

Note 3: Performance measured at Headphone Outputs, unless otherwise stated.

Note 4: Dynamic range measured with the EIAJ method. -60dBFS, 1kHz output signal, A-weighted and normalized to 0dBFS. $f = 20Hz - 20kHz$

Note 5: Gain measured relative to the 0dB setting.

Note 6: Accurate for synchronous clocking modes where NI is a multiple of 0x1000.

Note 7: Performance measured using DAC Inputs, unless otherwise stated.

Note 8: Full scale analog output with 0dB of programmable gain, and a 0dBFS DAC input amplitude, a $1V_{RMS}$ differential analog input amplitude, or a $0.5V_{RMS}$ single-ended analog input amplitude.

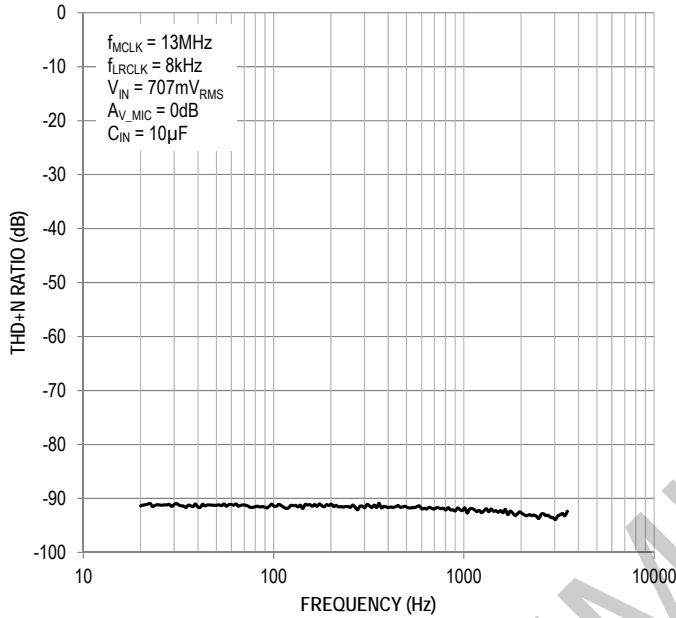
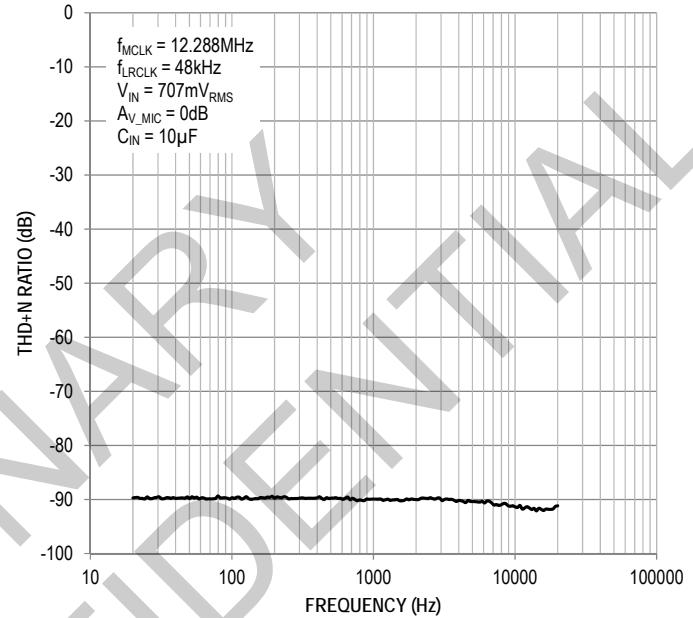
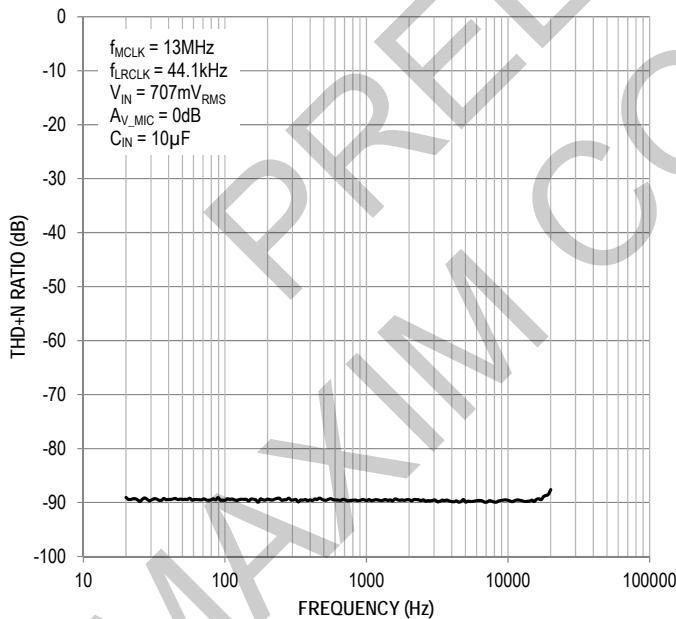
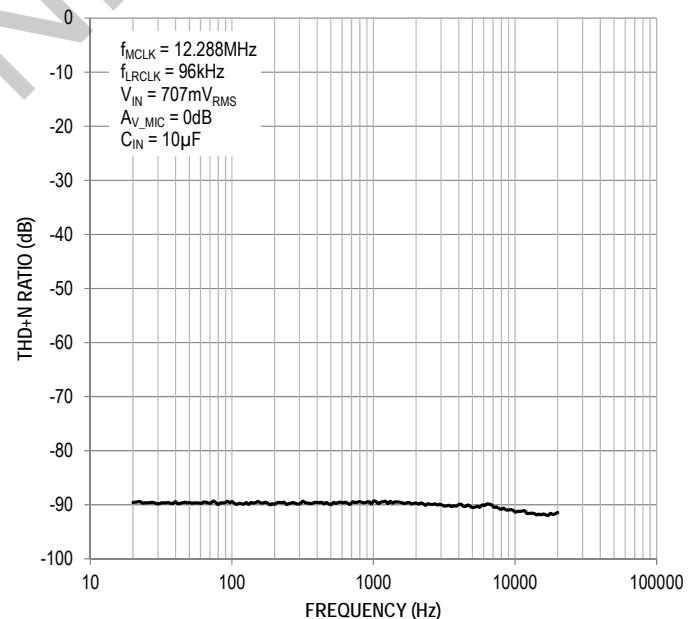
Note 9: f_{LRCLK} may be any rate in the indicated range. Asynchronous and non-integer f_{MCLK}/f_{LRCLK} ratios may exhibit some full scale performance degradation compared to Synchronous integer ratios.

Note 10: In master-mode operation, the accuracy of the MCLK input proportionally determines the accuracy of the sample clock rate.

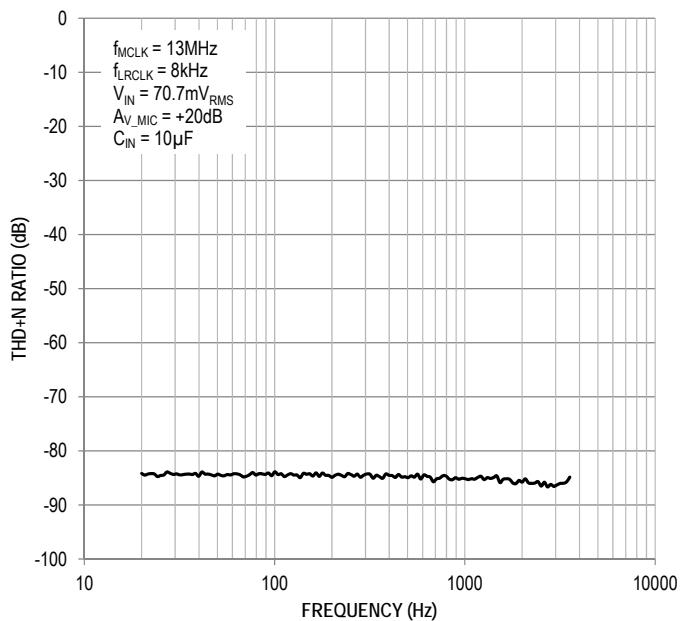
Note 11: C_B is in pF.

Note 12: VCM will be derived from a bandgap reference (VCM_MODE = 1) to allow the DC PSRR measurement to test the supply voltage range.

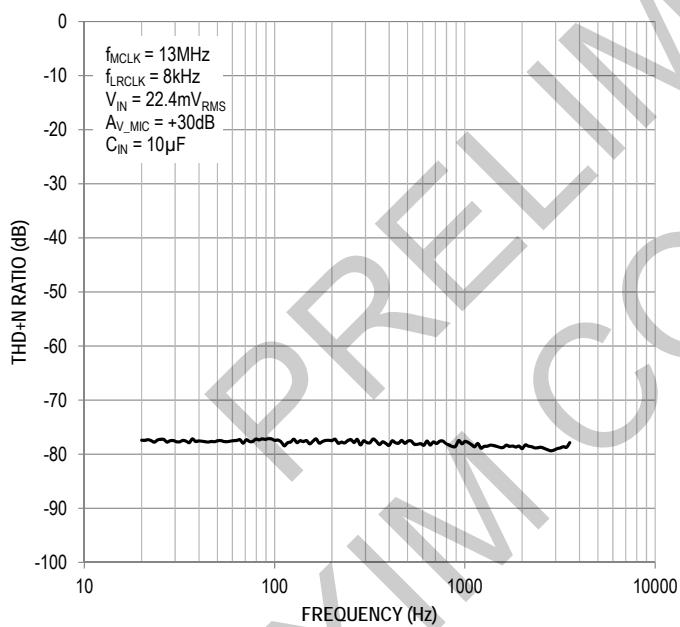
Note 13: Performance measured using an analog input to amplifier output path.

POWER CONSUMPTION**TYPICAL OPERATING CHARACTERISTICS**TOTAL HARMONIC DISTORTION PLUS NOISE
VS FREQUENCY (MIC TO ADC)TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (MIC TO ADC)TOTAL HARMONIC DISTORTION PLUS NOISE
VS FREQUENCY (MIC TO ADC)TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (MIC TO ADC)

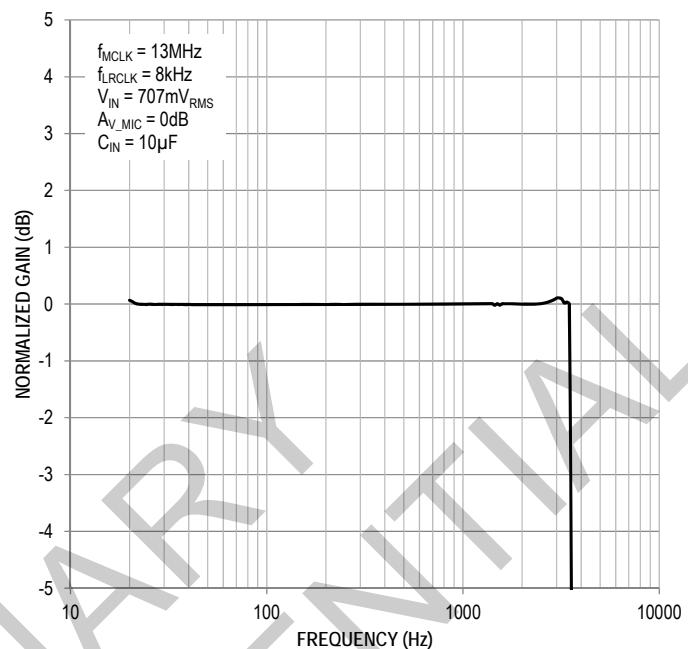
TOTAL HARMONIC DISTORTION PLUS NOISE
VS FREQUENCY (MIC TO ADC)



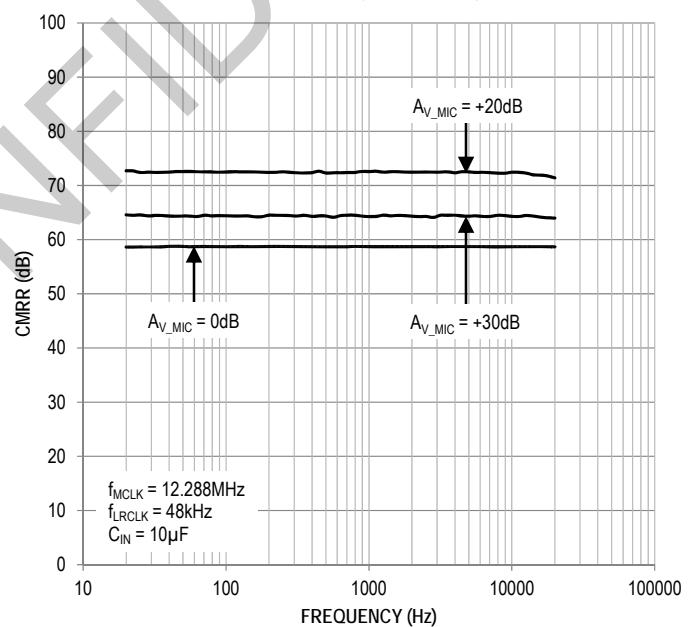
TOTAL HARMONIC DISTORTION PLUS NOISE
VS FREQUENCY (MIC TO ADC)



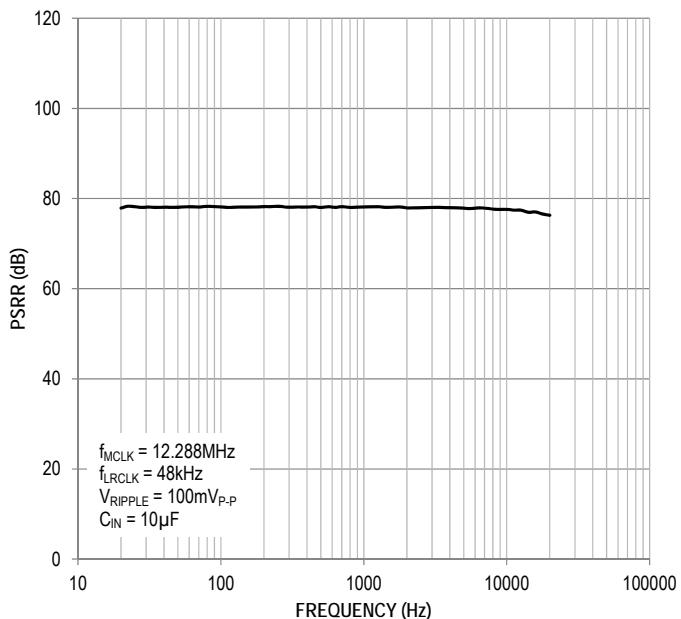
GAIN vs FREQUENCY (MIC TO ADC)



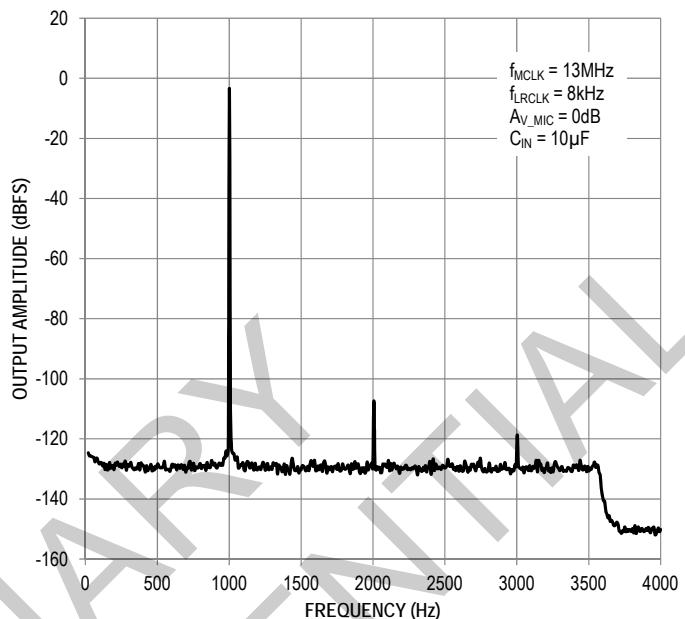
COMMON MODE REJECTION RATIO
VS FREQUENCY (MIC TO ADC)



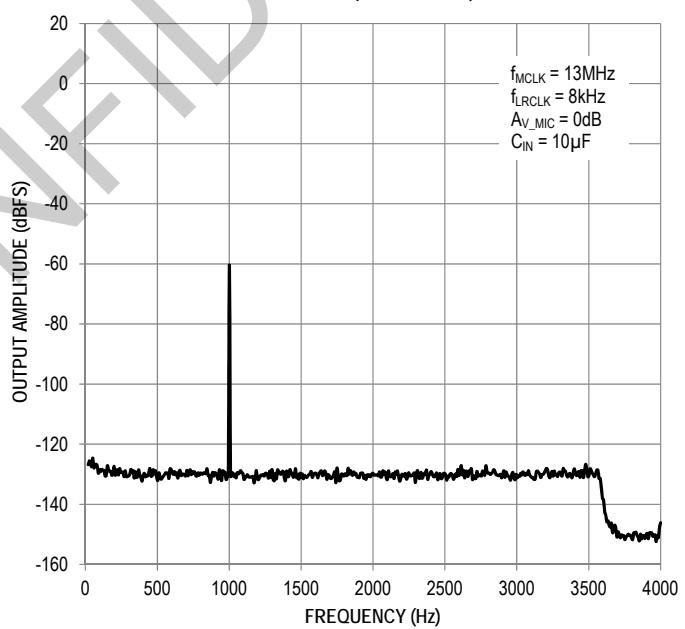
POWER SUPPLY REJECTION RATIO
vs FREQUENCY (MIC to ADC)

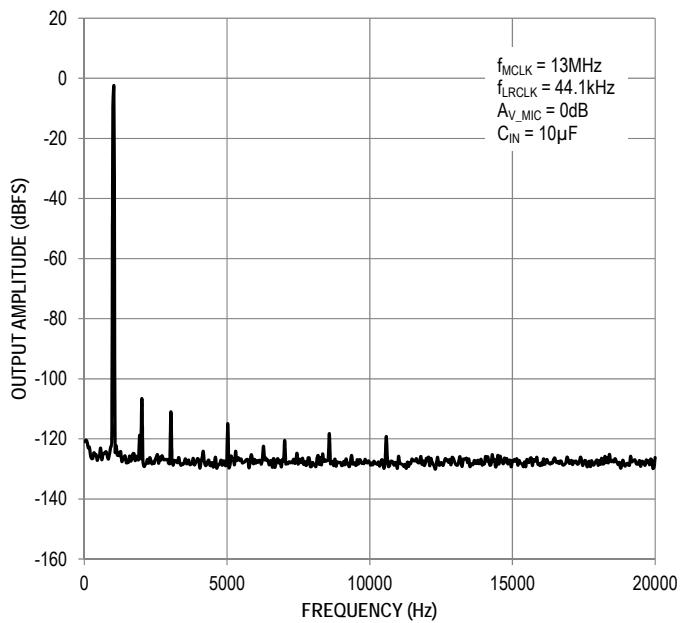
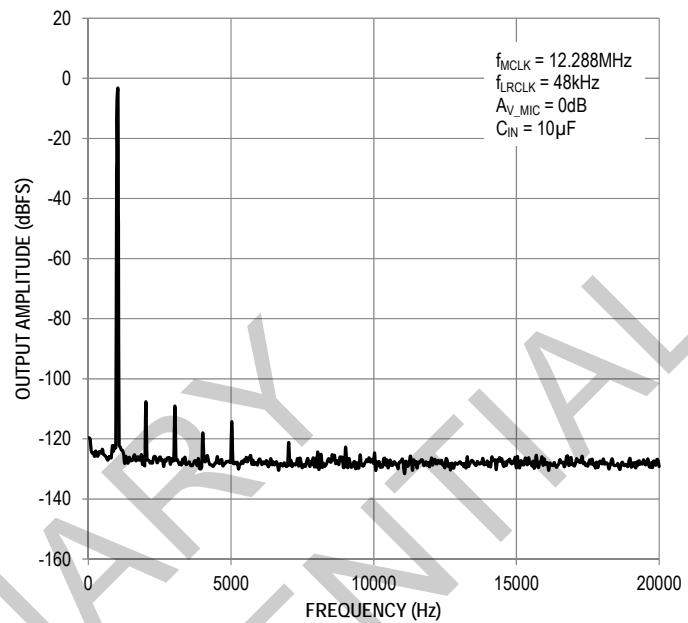
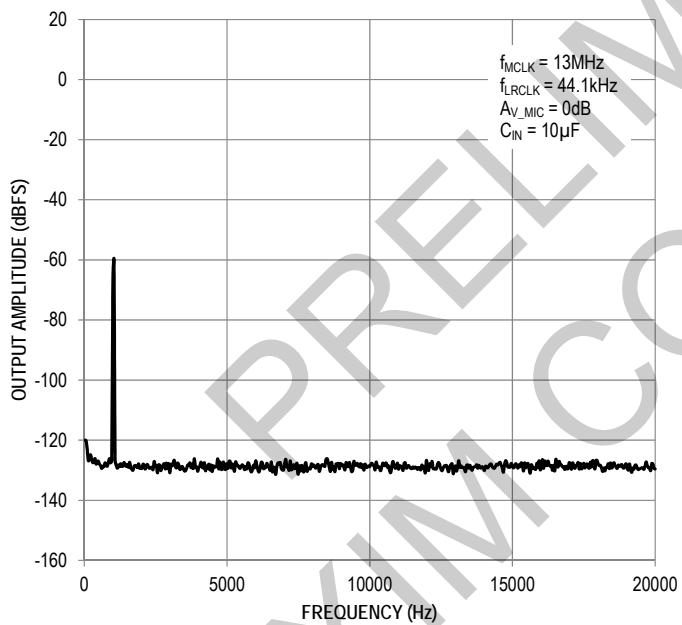
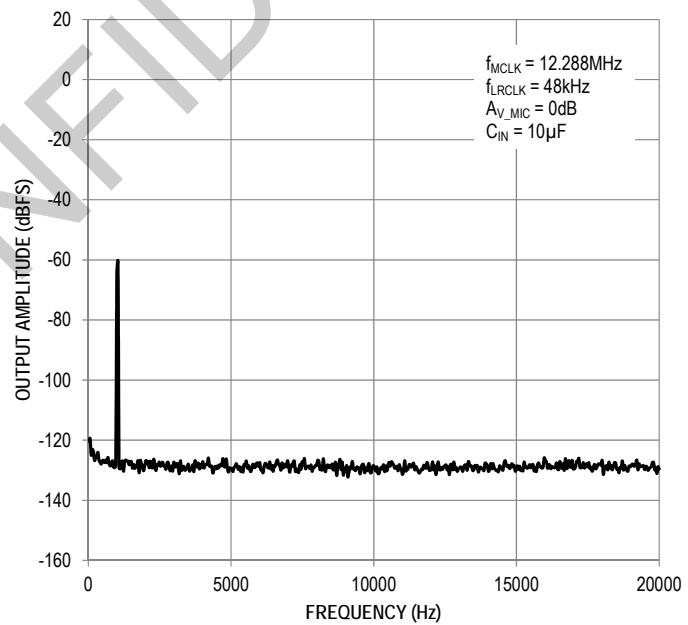


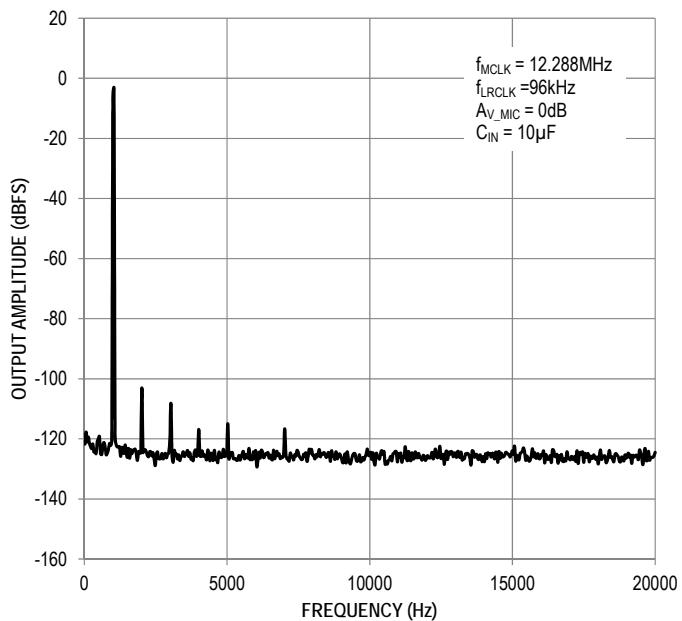
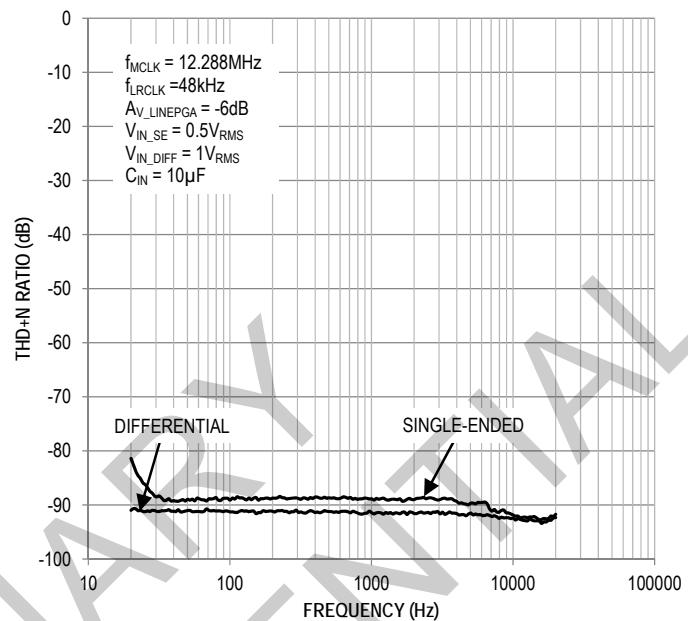
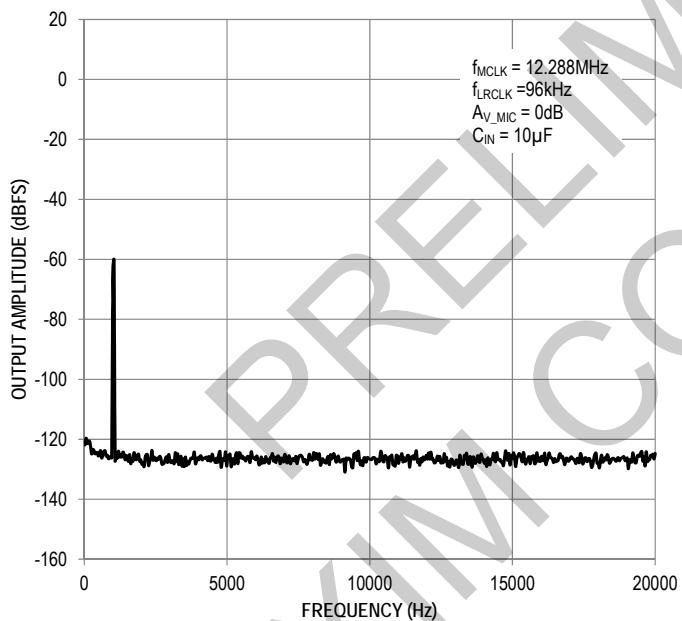
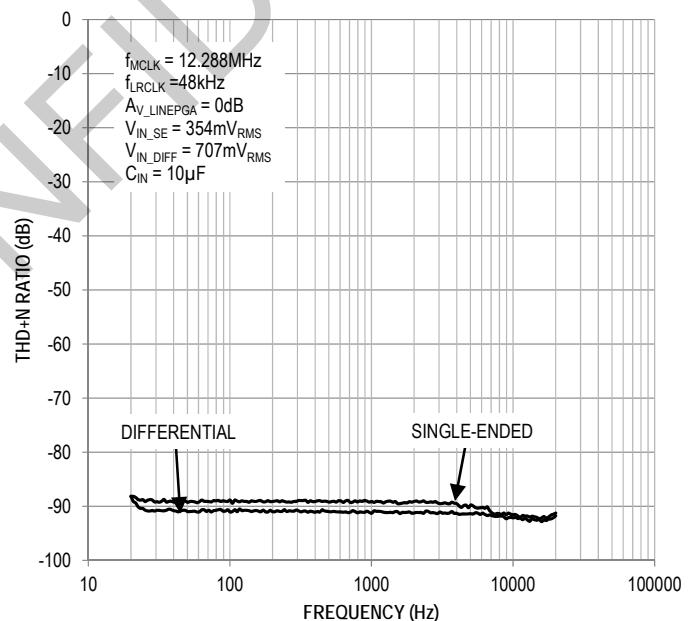
INBAND OUTPUT SPECTRUM,
-3dBFS INPUT (MIC TO ADC)



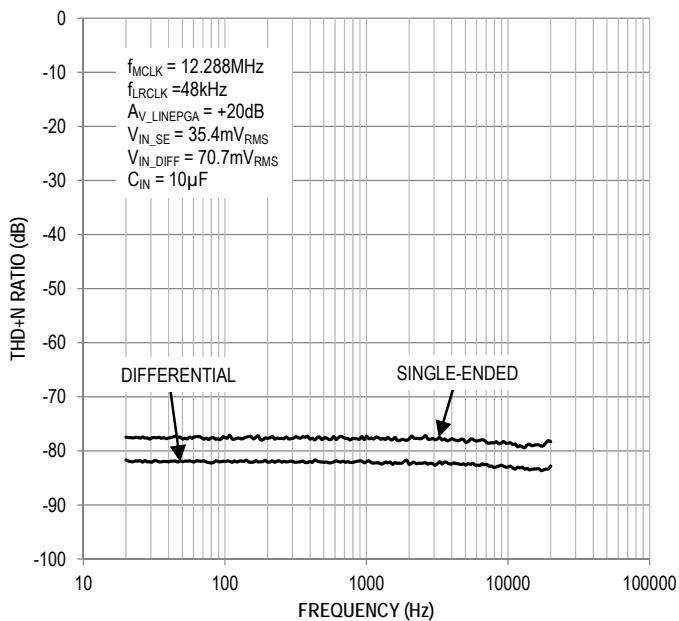
INBAND OUTPUT SPECTRUM,
-60dBFS INPUT (MIC TO ADC)



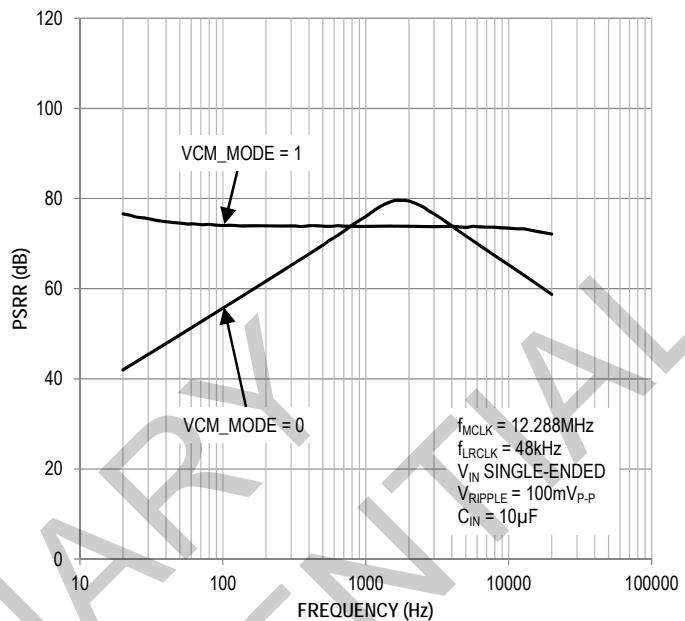
INBAND OUTPUT SPECTRUM,
-3dBFS INPUT (MIC TO ADC)INBAND OUTPUT SPECTRUM,
-3dBFS INPUT (MIC TO ADC)INBAND OUTPUT SPECTRUM,
-60dBFS INPUT (MIC TO ADC)INBAND OUTPUT SPECTRUM,
-60dBFS INPUT (MIC TO ADC)

INBAND OUTPUT SPECTRUM,
-3dBFS INPUT (MIC TO ADC)TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (LINE TO ADC)INBAND OUTPUT SPECTRUM,
-60dBFS INPUT (MIC TO ADC)TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (LINE TO ADC)

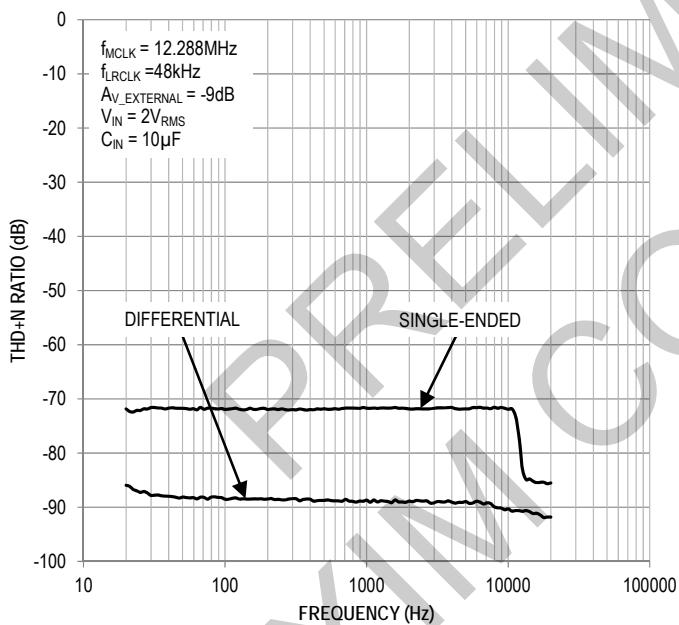
TOTAL HARMONIC DISTORTION PLUS NOISE
VS FREQUENCY (LINE TO ADC)



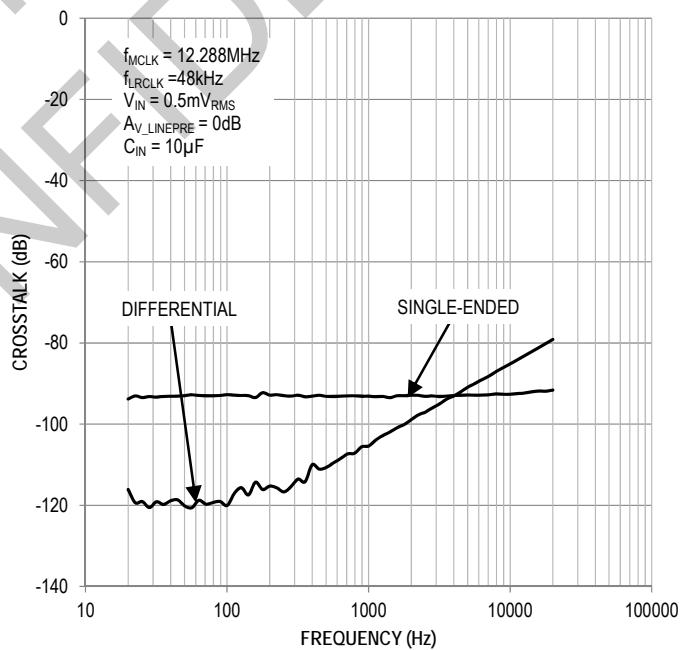
POWER SUPPLY REJECTION RATIO
vs FREQUENCY (LINE to ADC)

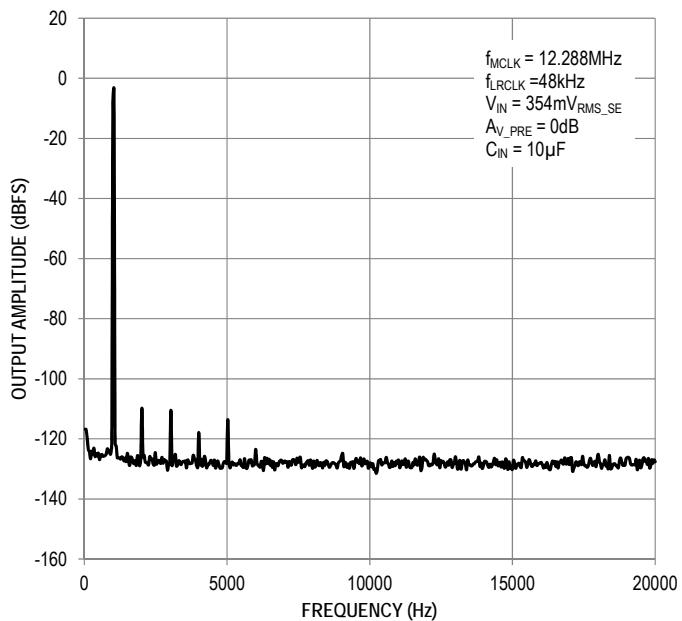
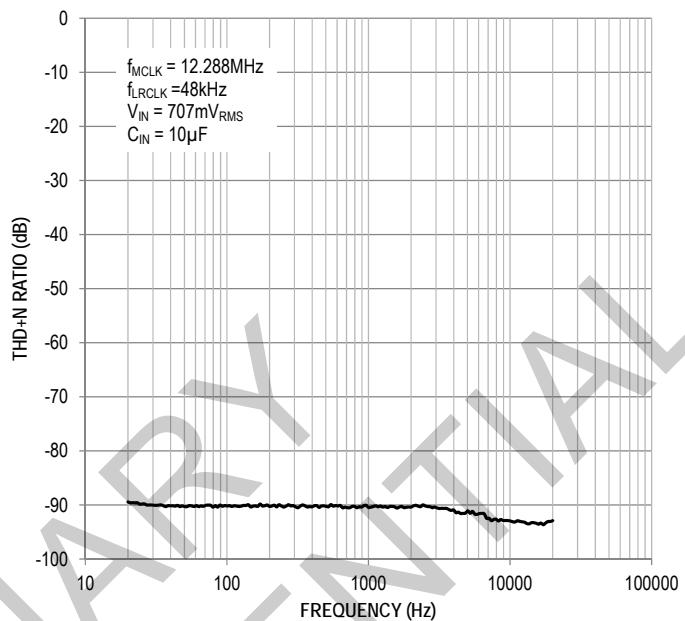
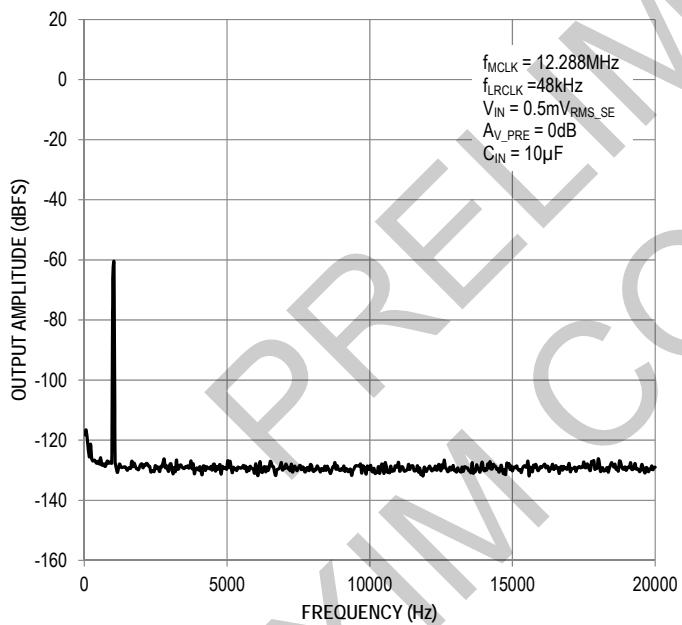
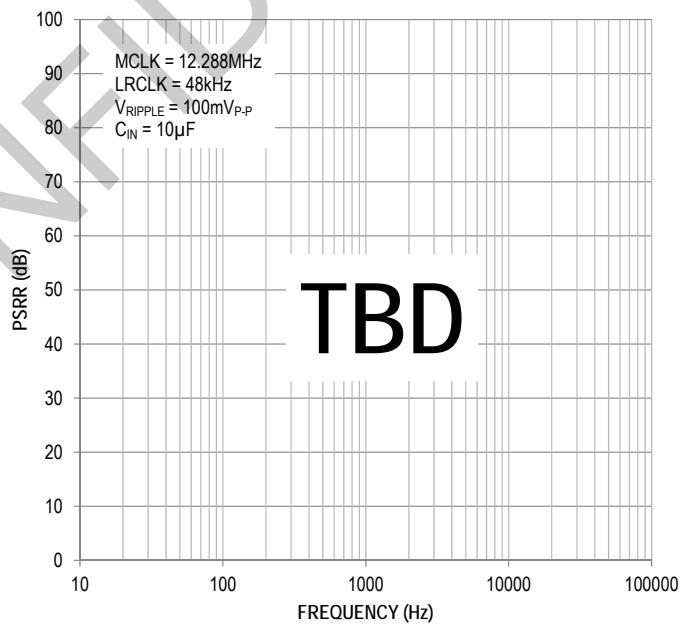


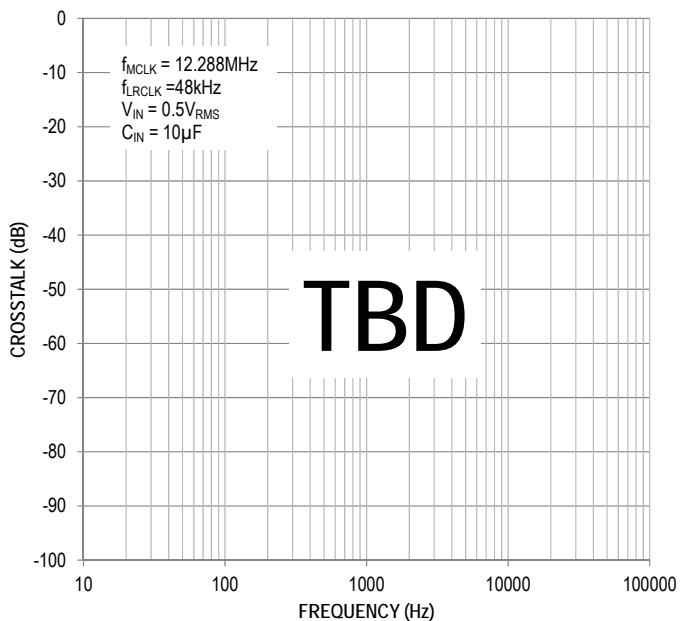
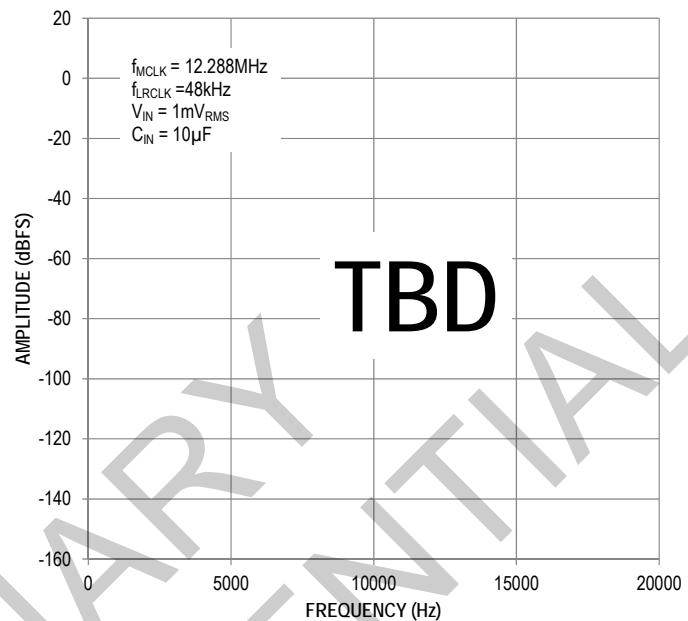
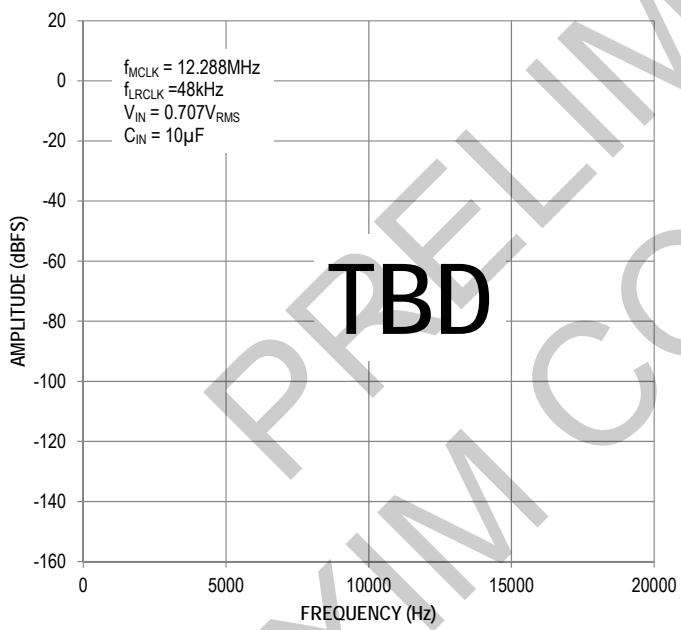
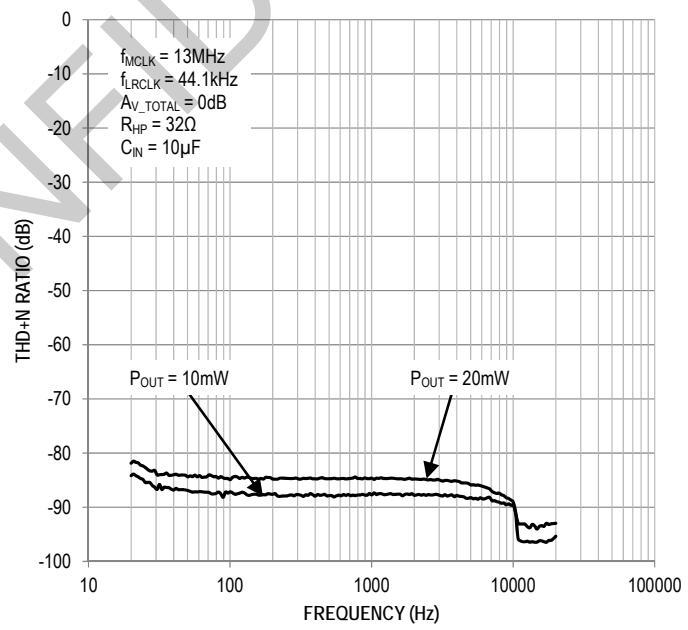
TOTAL HARMONIC DISTORTION PLUS NOISE
VS FREQUENCY (LINE TO ADC)



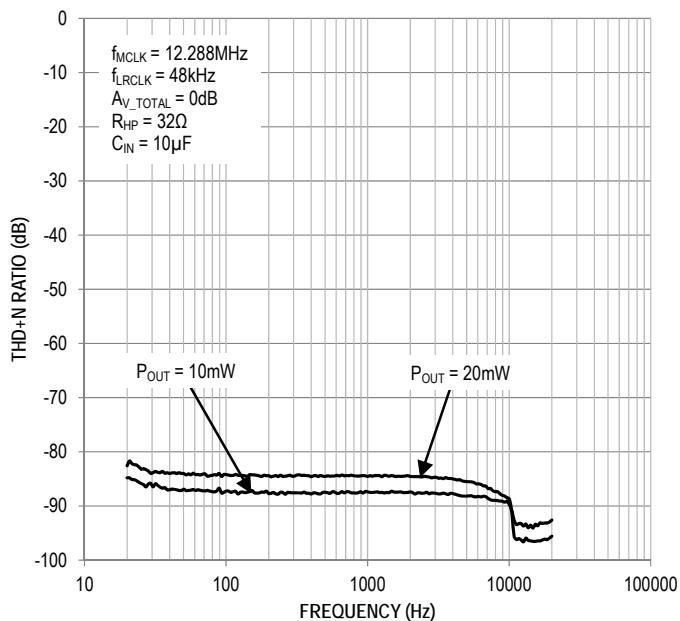
CROSSTALK vs FREQUENCY (LINE TO ADC)



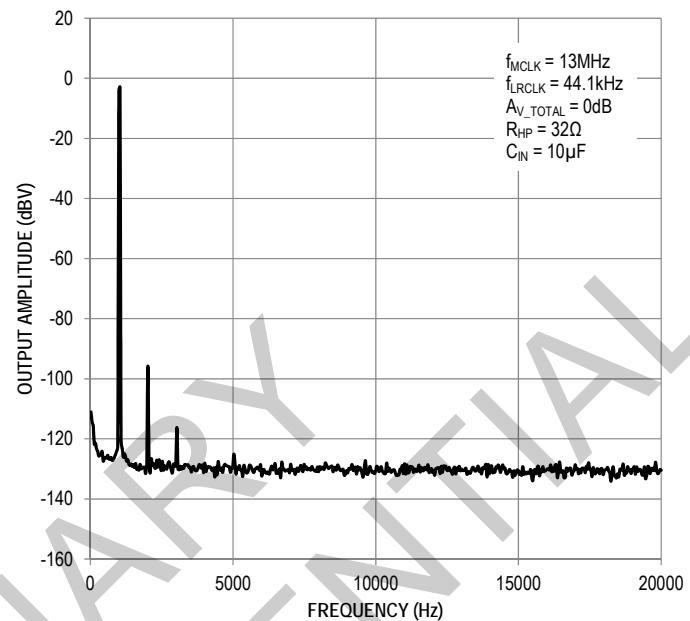
INBAND OUTPUT SPECTRUM vs FREQUENCY,
-3dBFS INPUT (LINE to ADC)TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (INPUT DIRECT TO ADC MIXER)INBAND OUTPUT SPECTRUM vs FREQUENCY,
-60dBFS INPUT (LINE to ADC)POWER SUPPLY REJECTION RATIO vs FREQUENCY (IN_
DIRECT TO ADC MIXER)

CROSSTALK vs FREQUENCY
(INPUT DIRECT TO ADC MIXER)INBAND OUTPUT SPECTRUM,
-60dBFS (IN_ DIRECT TO ADC MIXER)INBAND OUTPUT SPECTRUM,
-3dBFS (INPUT DIRECT TO ADC MIXER)TOTAL HARMONIC DISTORTION PLUS NOISE vs
FREQUENCY (LINE TO ADC TO DAC TO HEADPHONE)

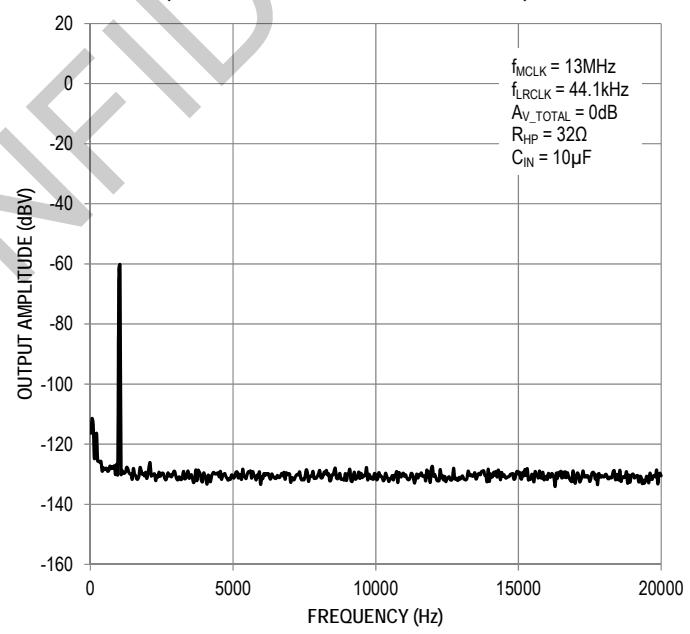
TOTAL HARMONIC DISTORTION PLUS NOISE vs
FREQUENCY (LINE TO ADC TO DAC TO HEADPHONE)



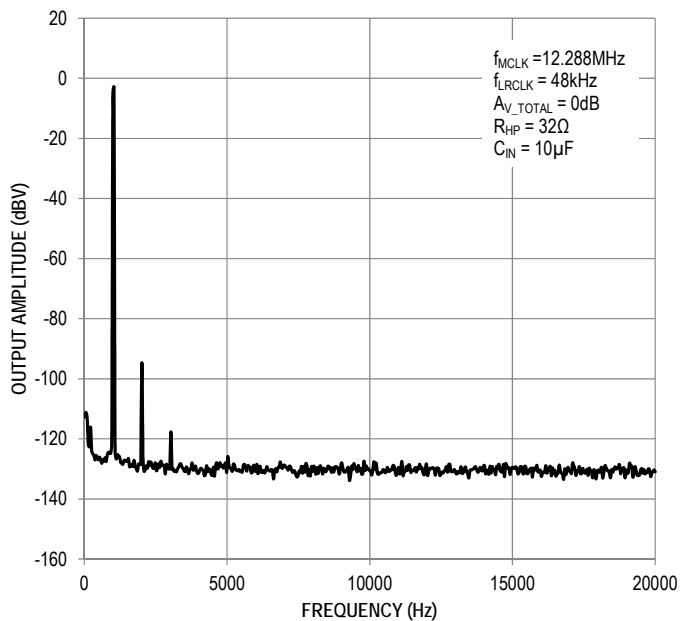
INBAND OUTPUT SPECTRUM, -3dBFS INPUT
(LINE TO ADC TO DAC TO HEADPHONE)



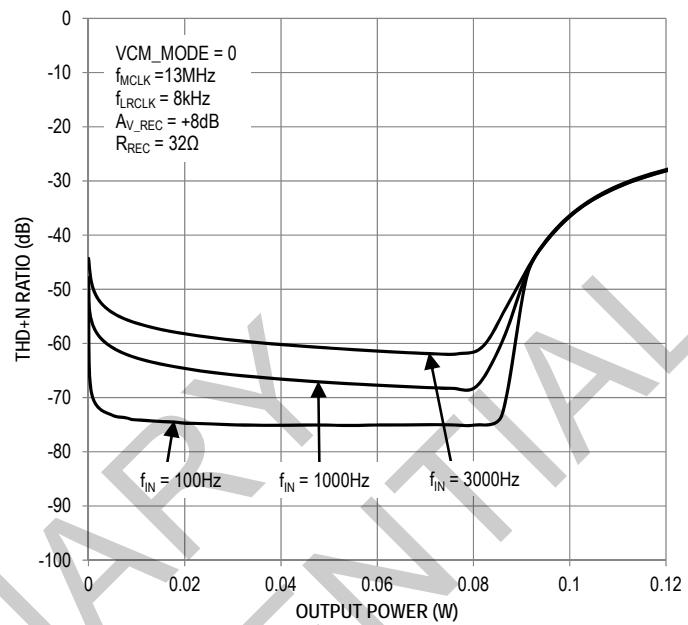
INBAND OUTPUT SPECTRUM, -60dBFS INPUT
(LINE TO ADC TO DAC TO HEADPHONE)



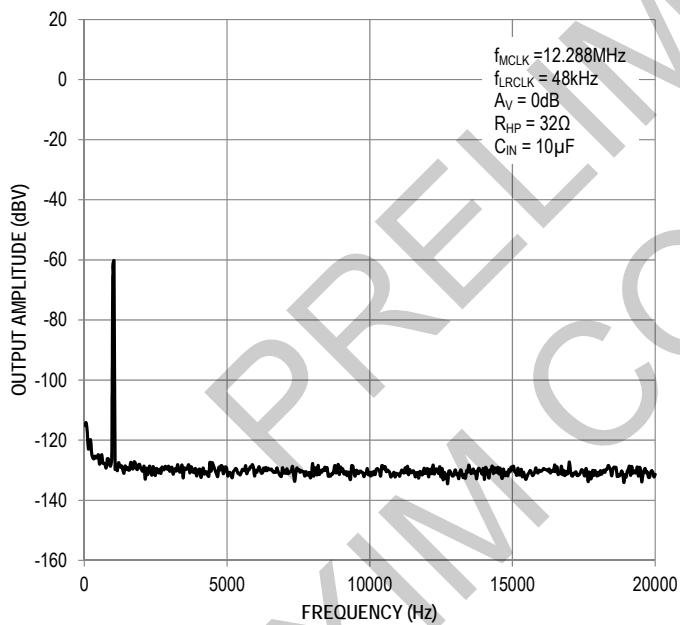
INBAND OUTPUT SPECTRUM, -3dBFS INPUT
(LINE TO ADC TO DAC TO HEADPHONE)



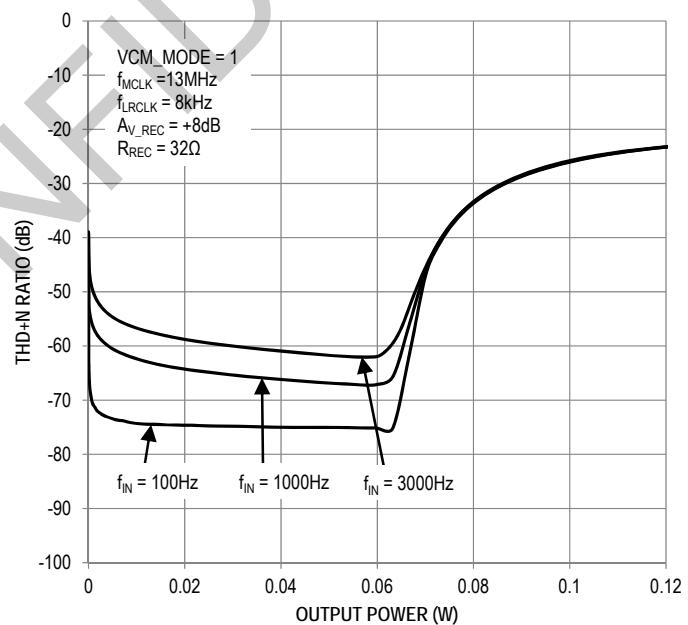
TOTAL HARMONIC DISTORTION PLUS NOISE
vs OUTPUT POWER (DAC TO RECEIVER)

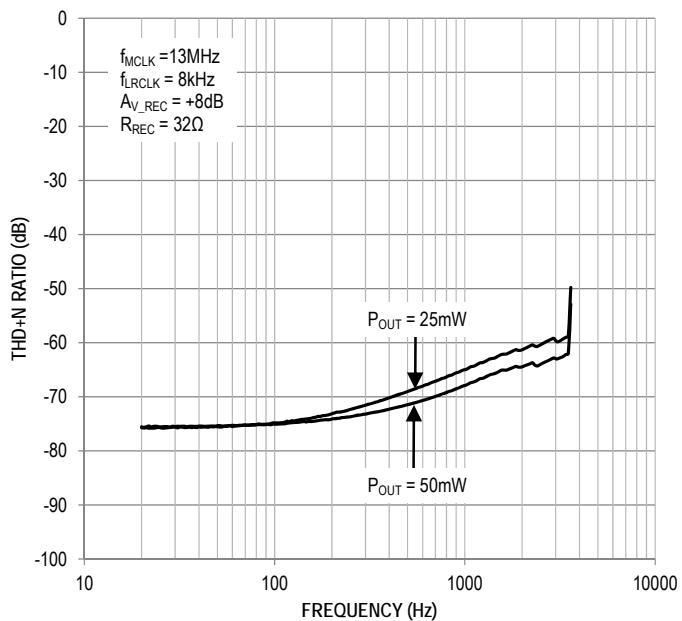


INBAND OUTPUT SPECTRUM, -60dBFS INPUT
(LINE TO ADC TO DAC TO HEADPHONE)

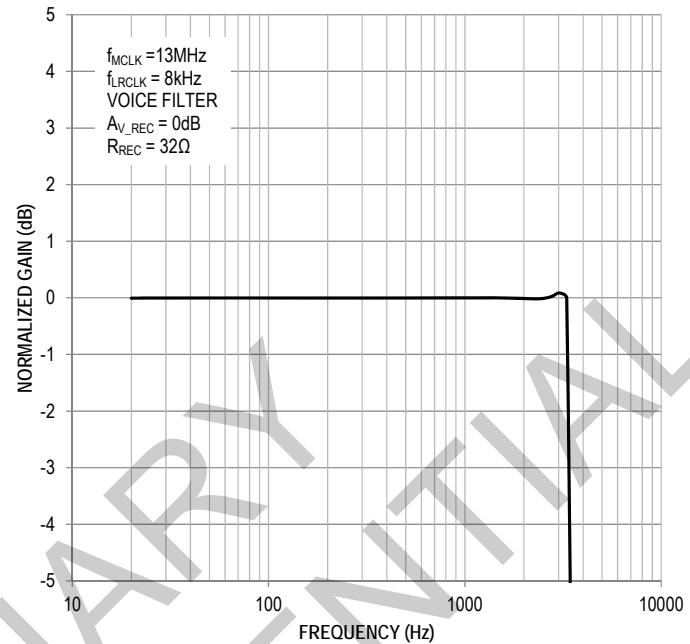
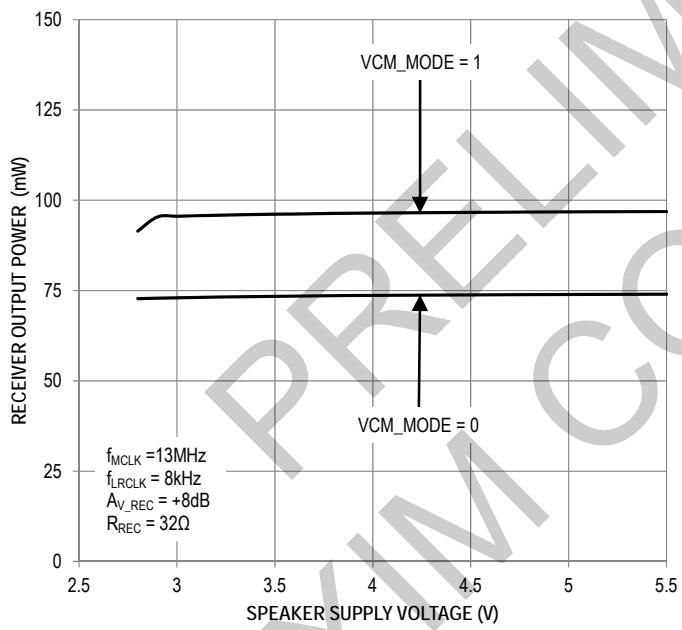
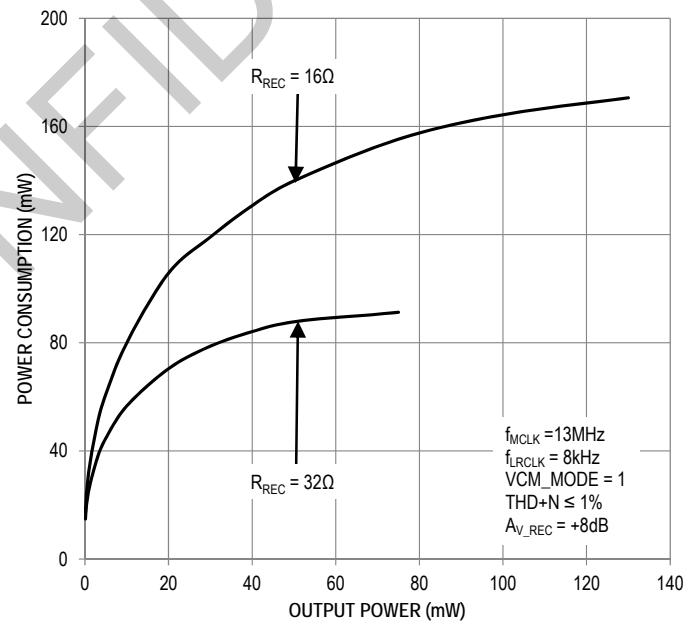


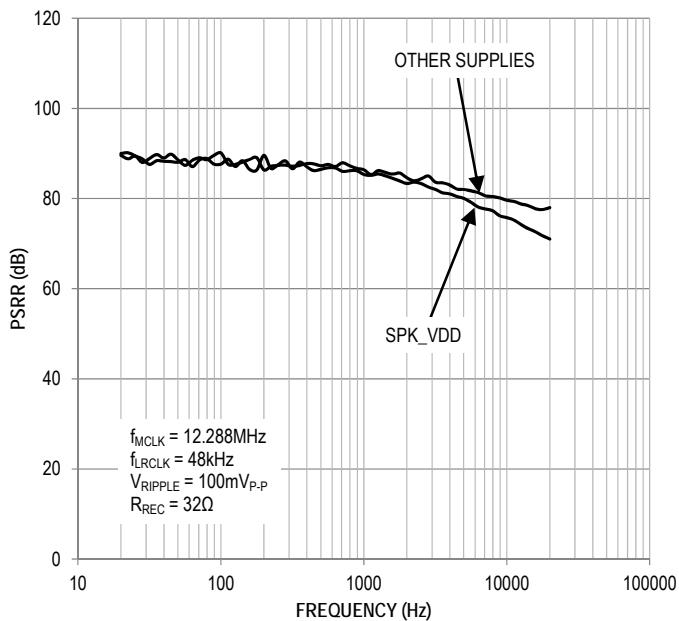
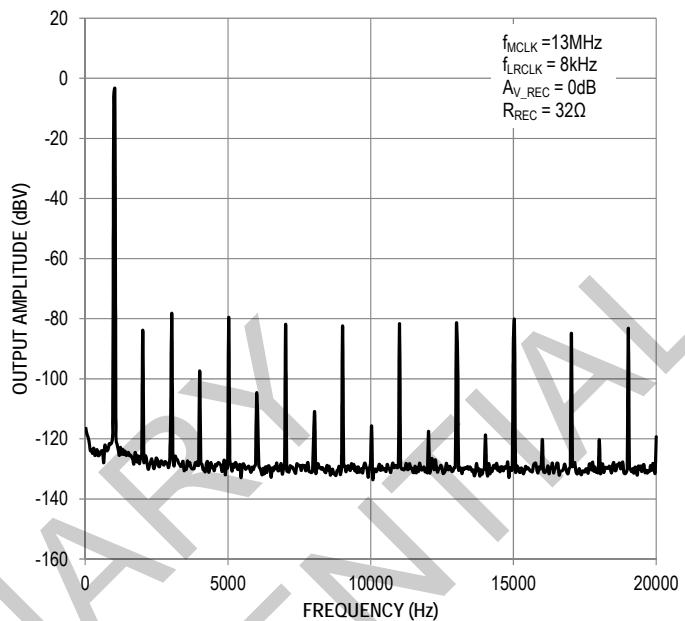
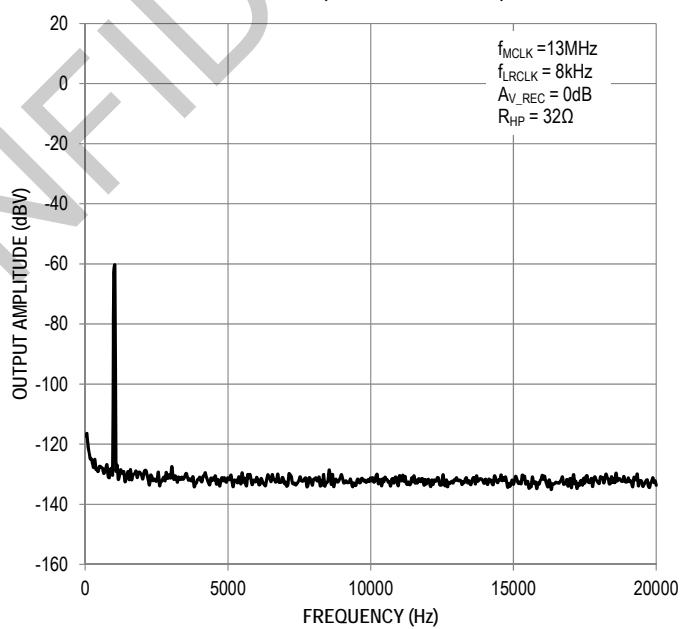
TOTAL HARMONIC DISTORTION
vs OUTPUT POWER (DAC TO RECEIVER)



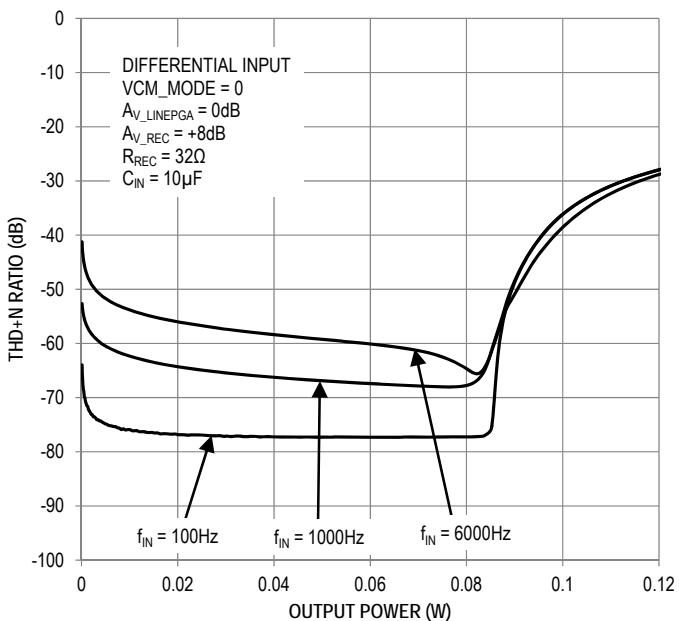
TOTAL HARMONIC DISTORTION
vs FREQUENCY (DAC TO RECEIVER)

GAIN vs FREQUENCY (DAC TO RECEIVER)

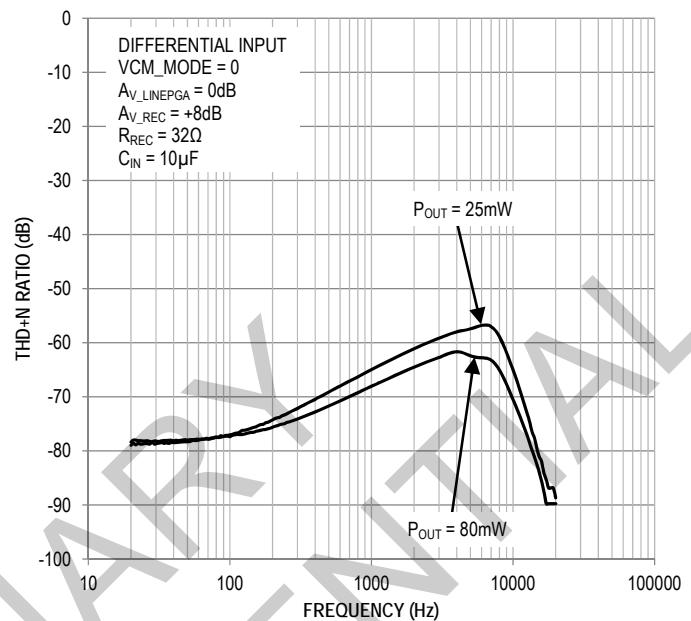
OUTPUT POWER vs SPEAKER SUPPLY VOLTAGE
(DAC TO RECEIVER)POWER CONSUMPTION vs
OUTPUT POWER (DAC TO RECEIVER)

POWER SUPPLY REJECTION RATIO vs FREQUENCY
(DAC to RECEIVER)INBAND OUTPUT SPECTRUM,
-3dBFS INPUT (DAC TO RECEIVER)INBAND OUTPUT SPECTRUM,
-60dBFS INPUT (DAC TO RECEIVER)

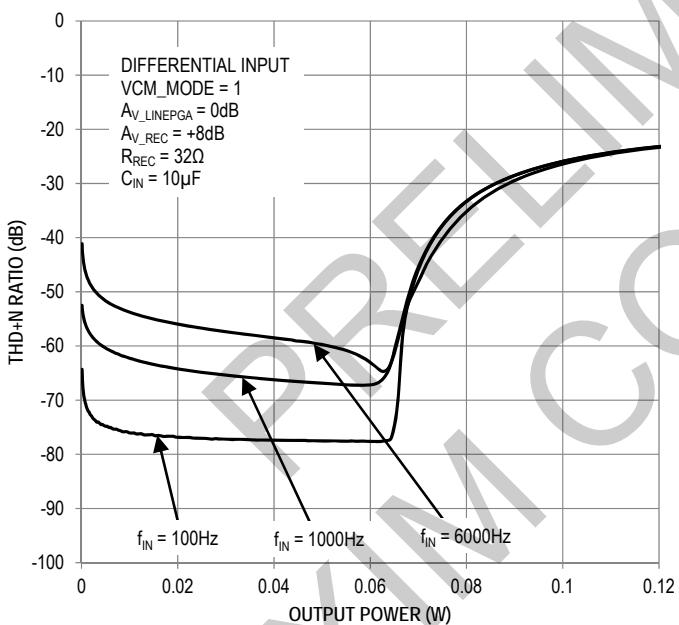
TOTAL HARMONIC DISTORTION PLUS NOISE
vs OUTPUT POWER (LINE TO RECEIVER)



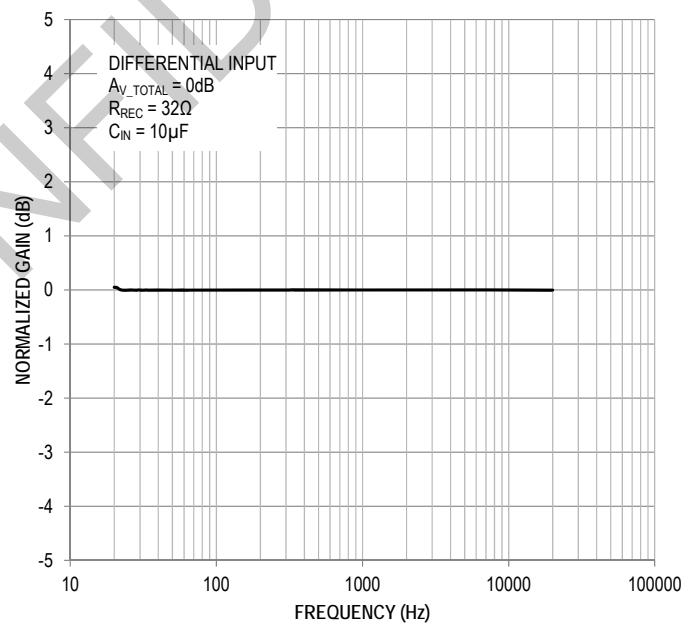
TOTAL HARMONIC DISTORTION PLUS NOISE vs
FREQUENCY (LINE TO RECEIVER)

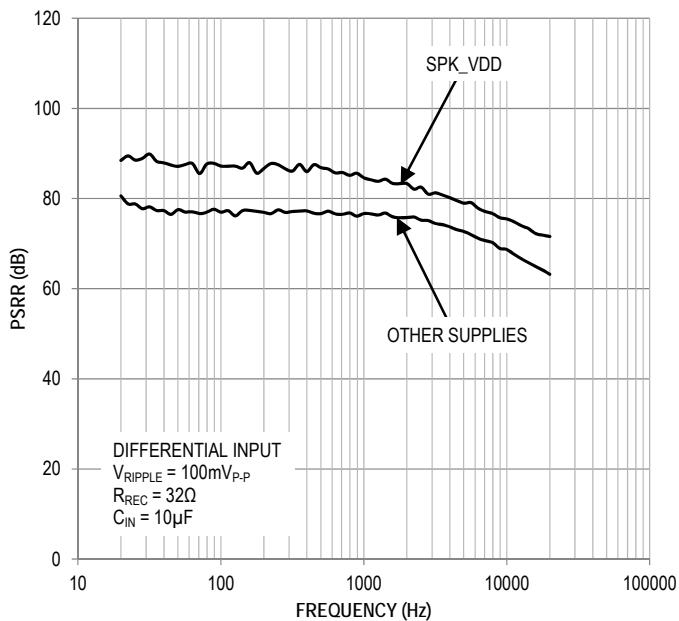
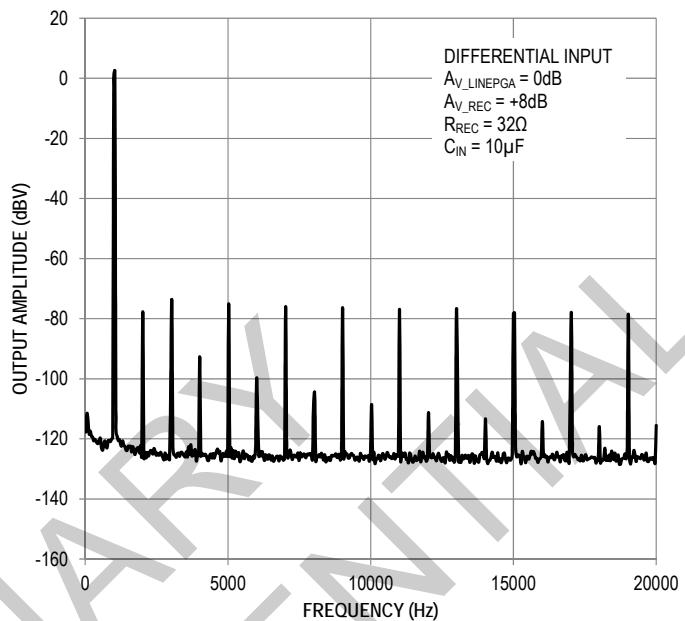
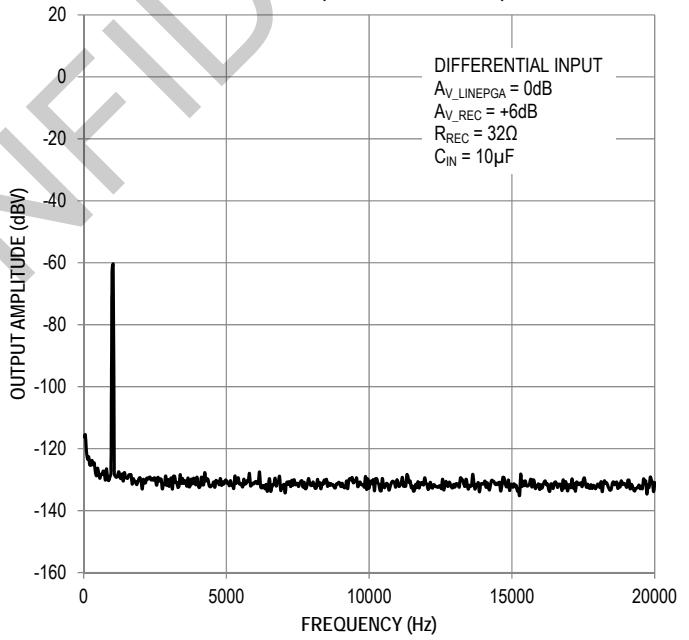


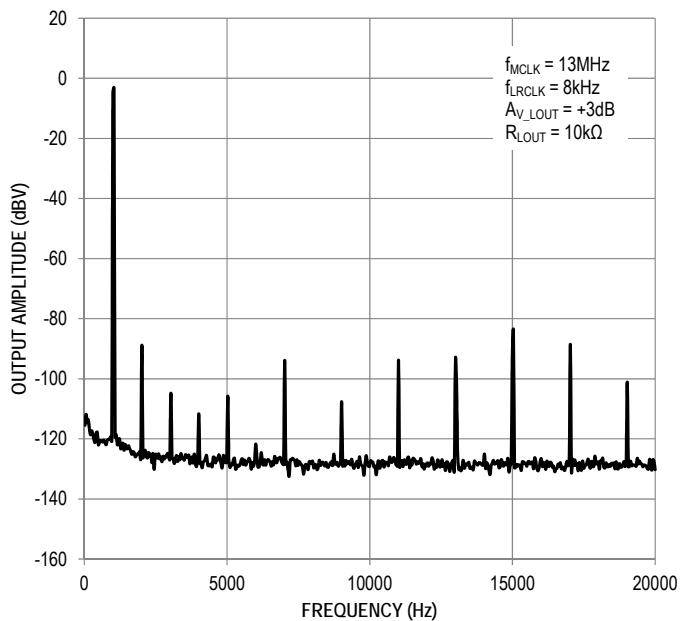
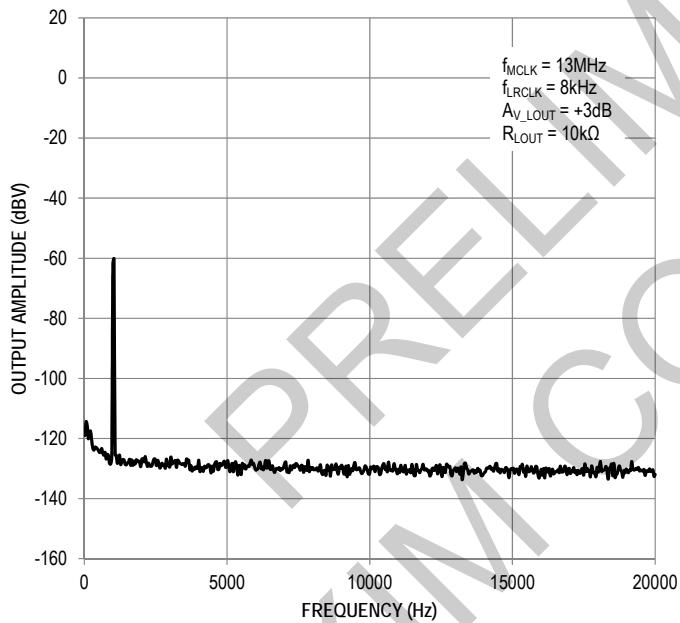
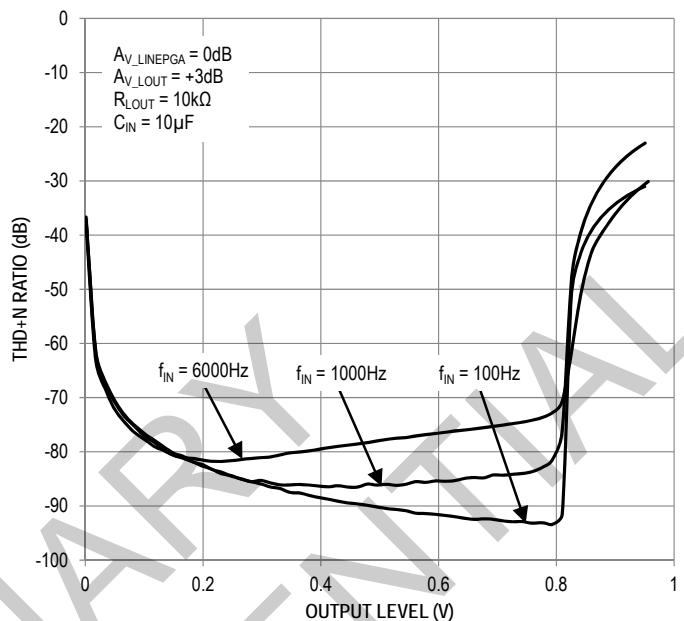
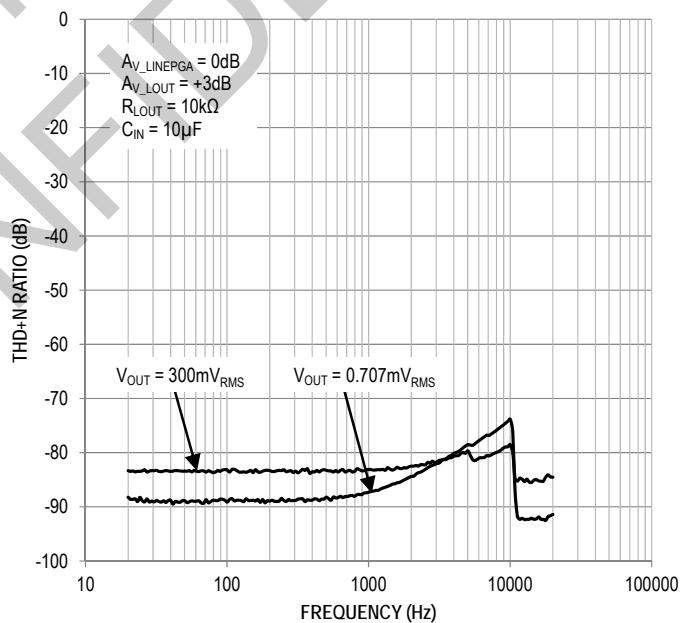
TOTAL HARMONIC DISTORTION PLUS NOISE
vs OUTPUT POWER (LINE TO RECEIVER)

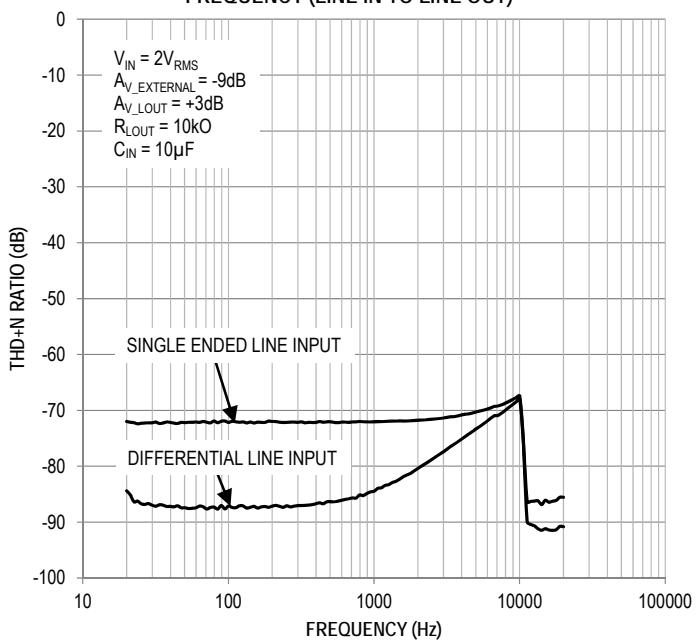
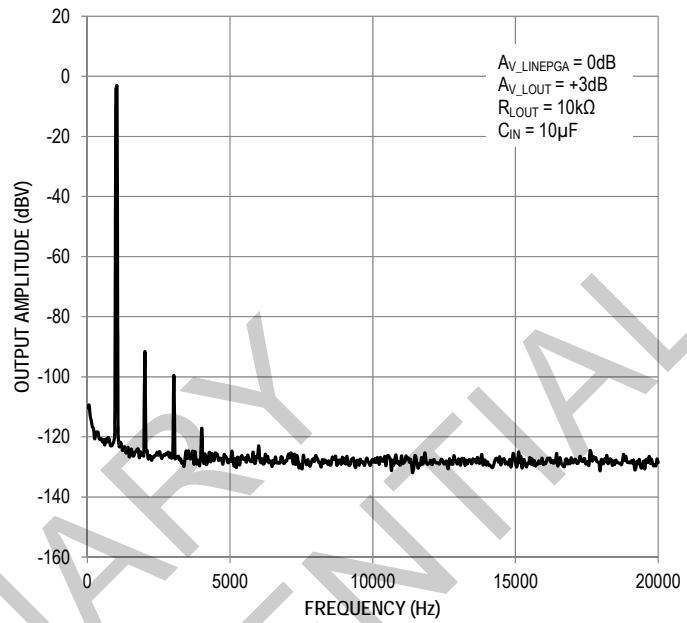
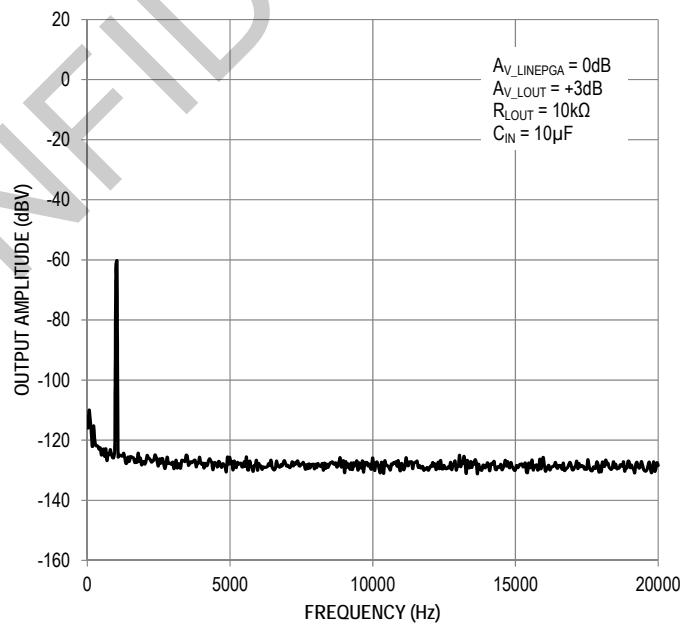


GAIN vs FREQUENCY
(LINE TO RECEIVER)

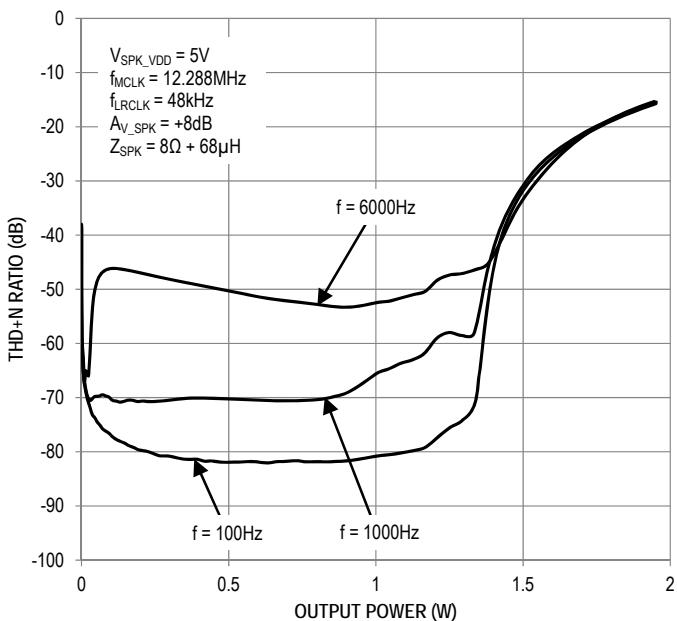


POWER SUPPLY REJECTION RATIO
vs FREQUENCY (LINE TO RECEIVER)INBAND OUTPUT SPECTRUM,
-3dBV INPUT (LINE TO RECEIVER)INBAND OUTPUT SPECTRUM,
-60dBV INPUT (LINE TO RECEIVER)

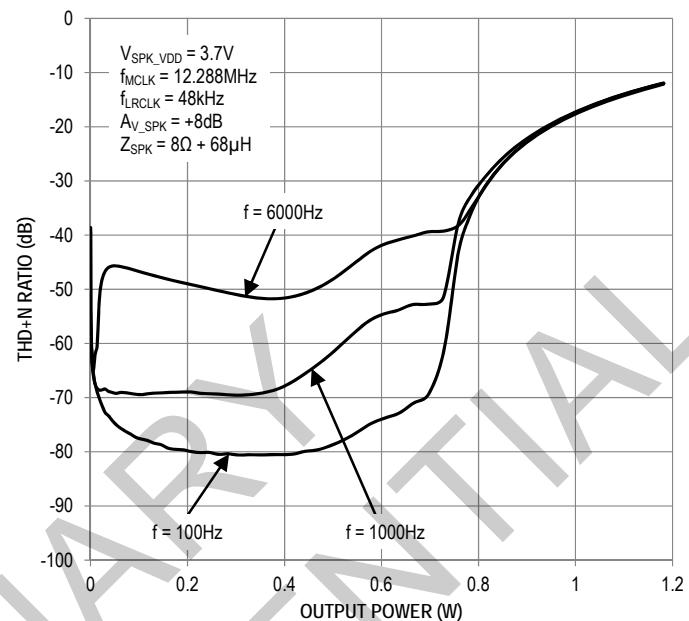
INBAND OUTPUT SPECTRUM,
-3d BFS INPUT (DAC TO LINE)INBAND OUTPUT SPECTRUM,
-60d BFS INPUT (DAC TO LINE)TOTAL HARMONIC DISTORTION PLUS NOISE
vs OUTPUT LEVEL (LINE IN TO LINE OUT)TOTAL HARMONIC DISTORTION PLUS NOISE vs
FREQUENCY (LINE IN TO LINE OUT)

TOTAL HARMONIC DISTORTION PLUS NOISE vs
FREQUENCY (LINE IN TO LINE OUT)INBAND OUTPUT SPECTRUM,
-3dBV INPUT (LINE IN TO LINE OUT)INBAND OUTPUT SPECTRUM,
-60dBV INPUT (LINE IN TO LINE OUT)

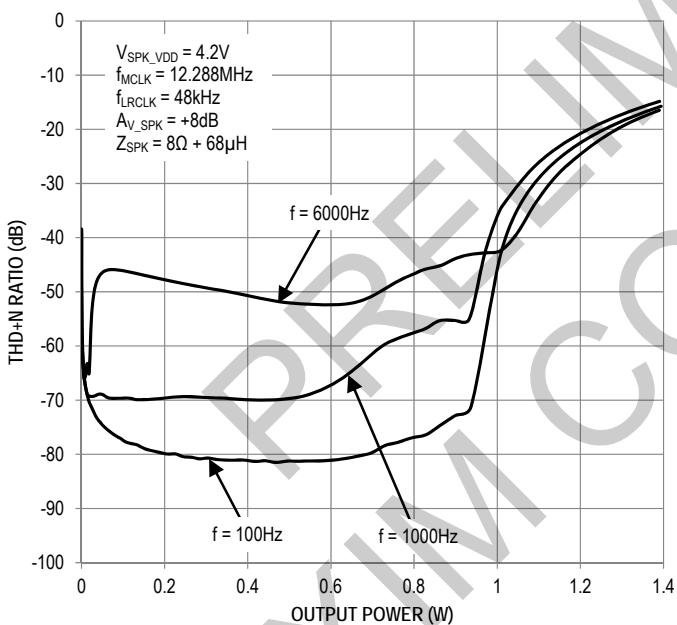
TOTAL HARMONIC DISTORTION PLUS NOISE
vs OUTPUT POWER (DAC TO SPEAKER)



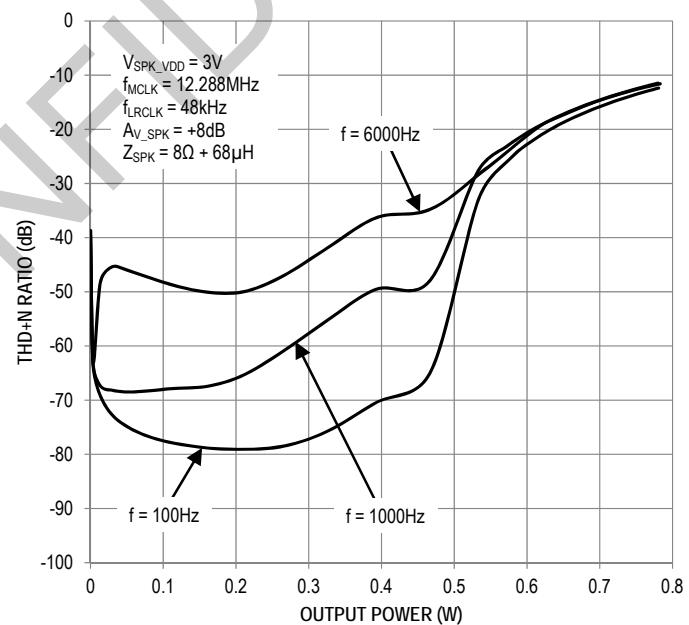
TOTAL HARMONIC DISTORTION PLUS NOISE
vs OUTPUT POWER (DAC TO SPEAKER)

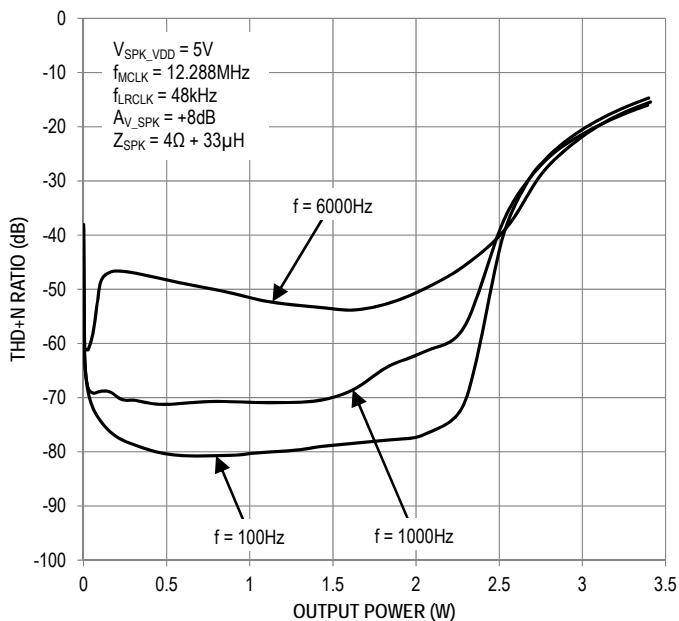
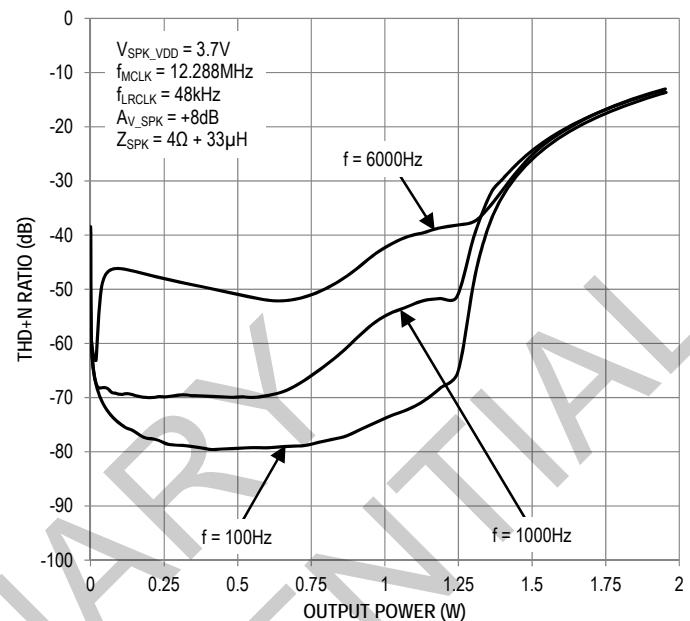
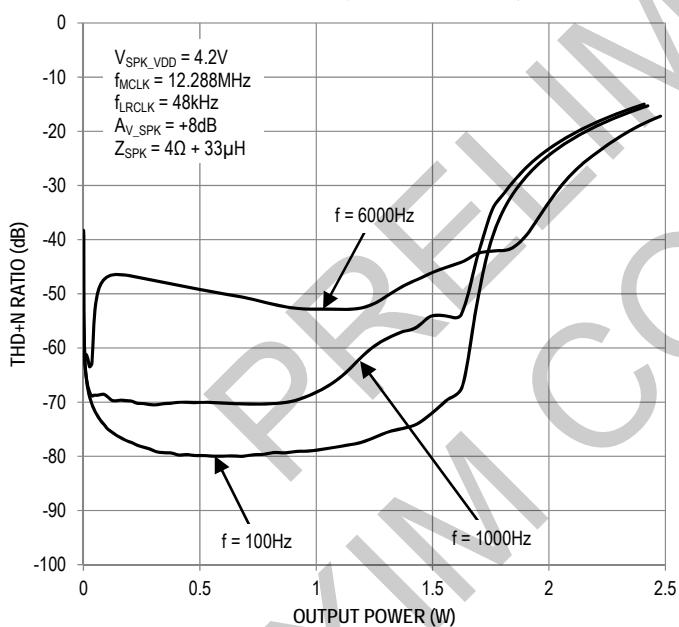
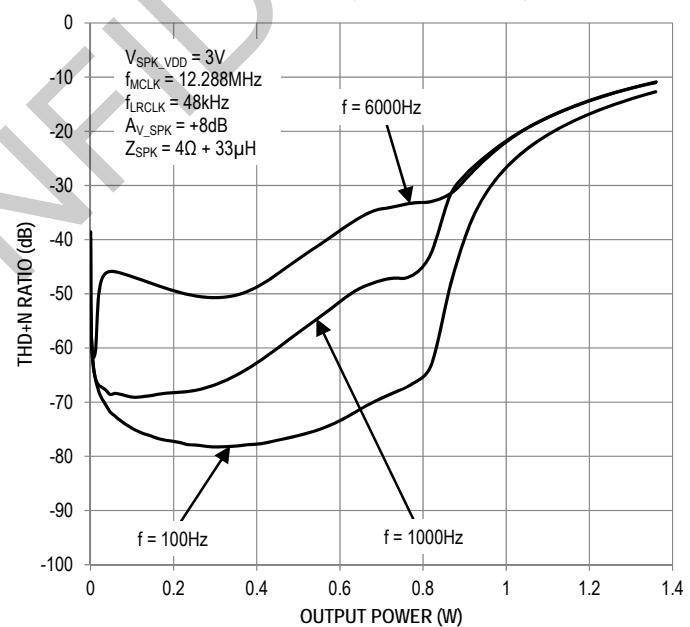


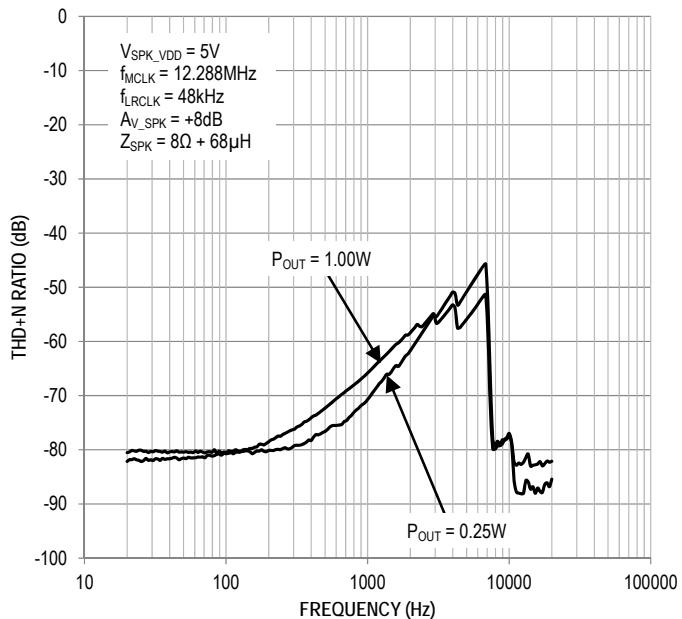
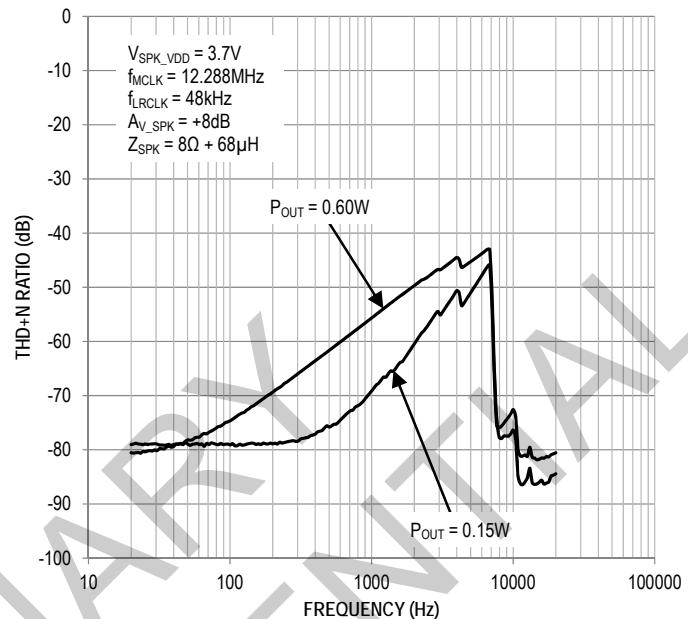
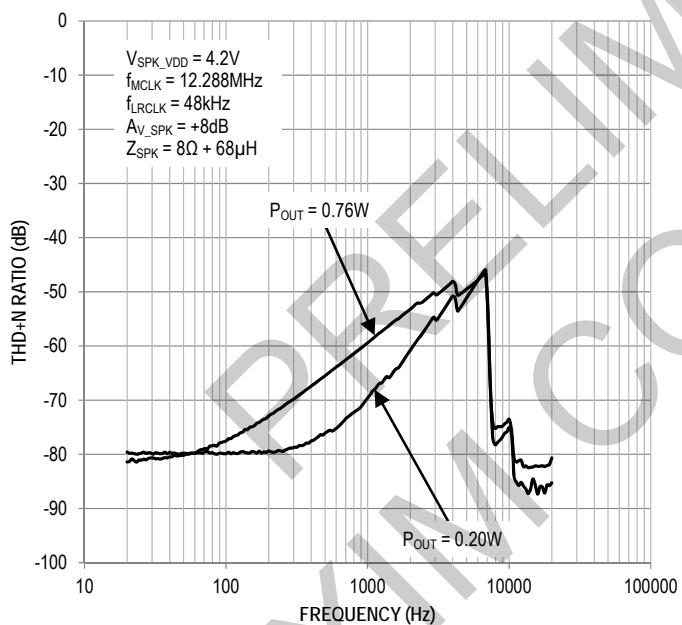
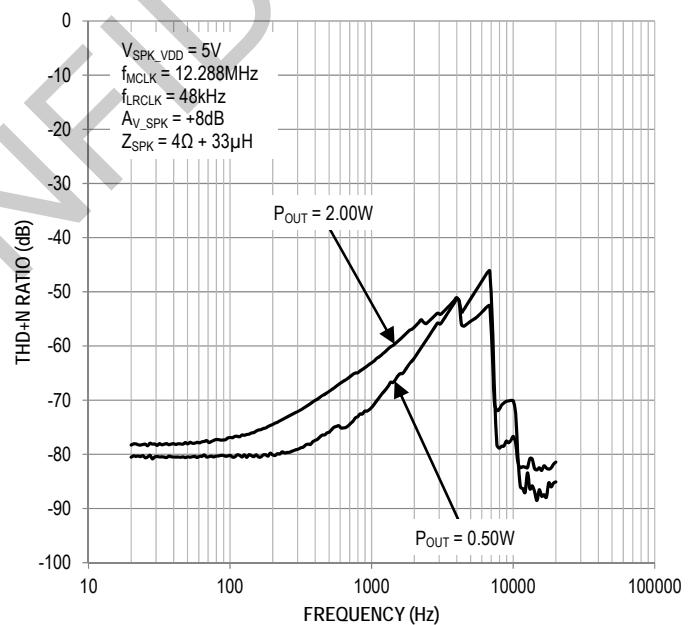
TOTAL HARMONIC DISTORTION PLUS NOISE
vs OUTPUT POWER (DAC TO SPEAKER)

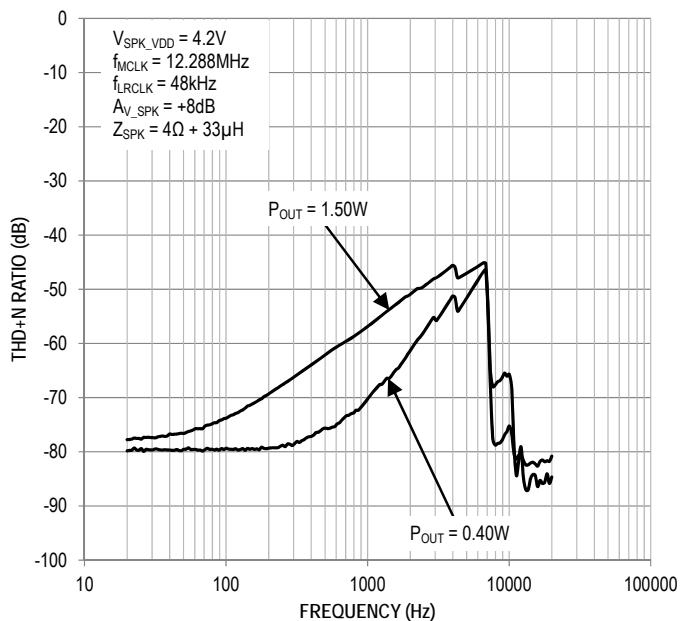
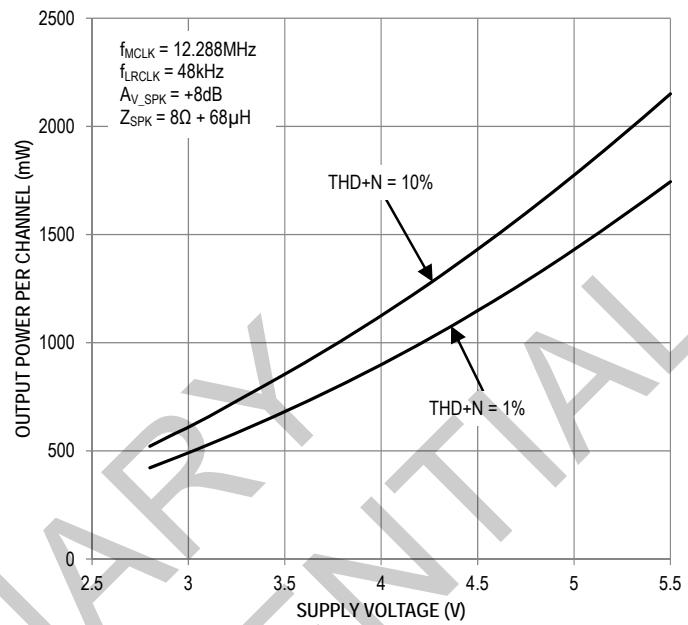
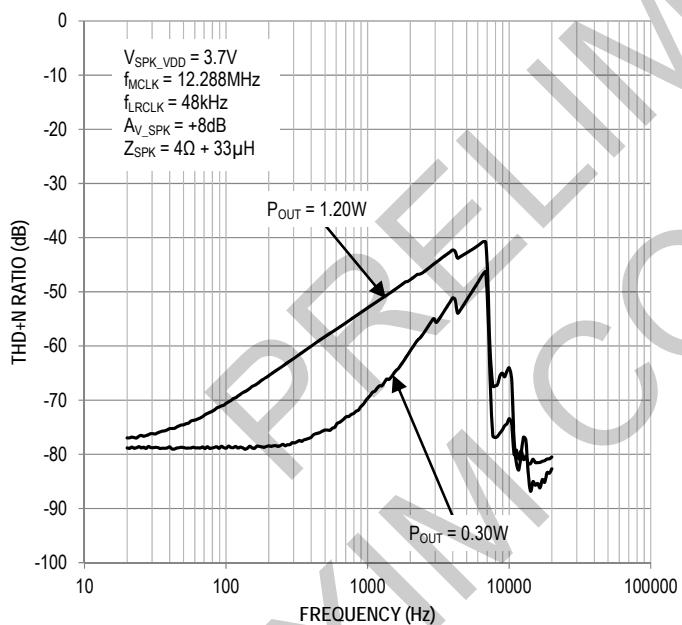
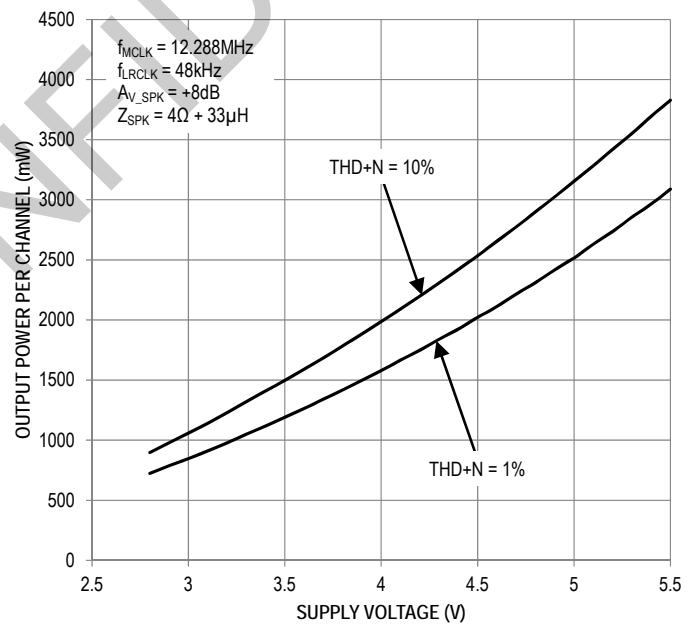


TOTAL HARMONIC DISTORTION PLUS NOISE
vs OUTPUT POWER (DAC TO SPEAKER)

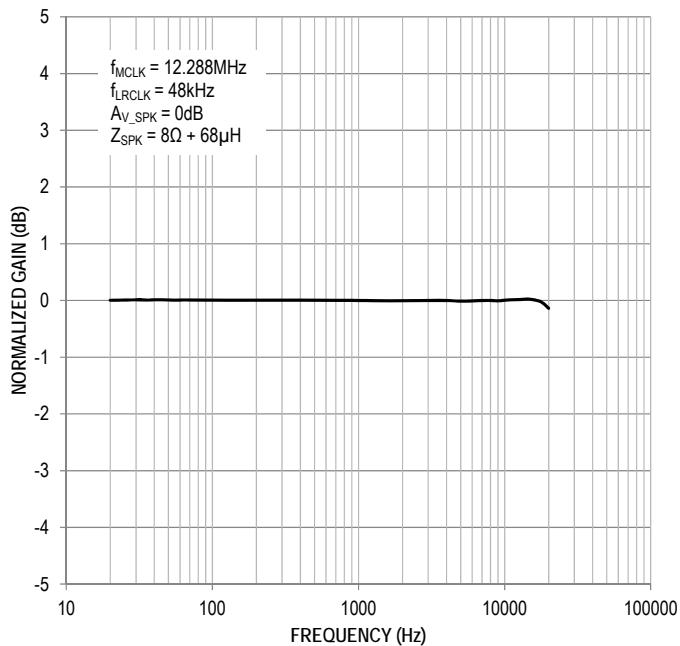


TOTAL HARMONIC DISTORTION PLUS NOISE
vs OUTPUT POWER (DAC TO SPEAKER)TOTAL HARMONIC DISTORTION PLUS NOISE
vs OUTPUT POWER (DAC TO SPEAKER)TOTAL HARMONIC DISTORTION PLUS NOISE
vs OUTPUT POWER (DAC TO SPEAKER)TOTAL HARMONIC DISTORTION PLUS NOISE
vs OUTPUT POWER (DAC TO SPEAKER)

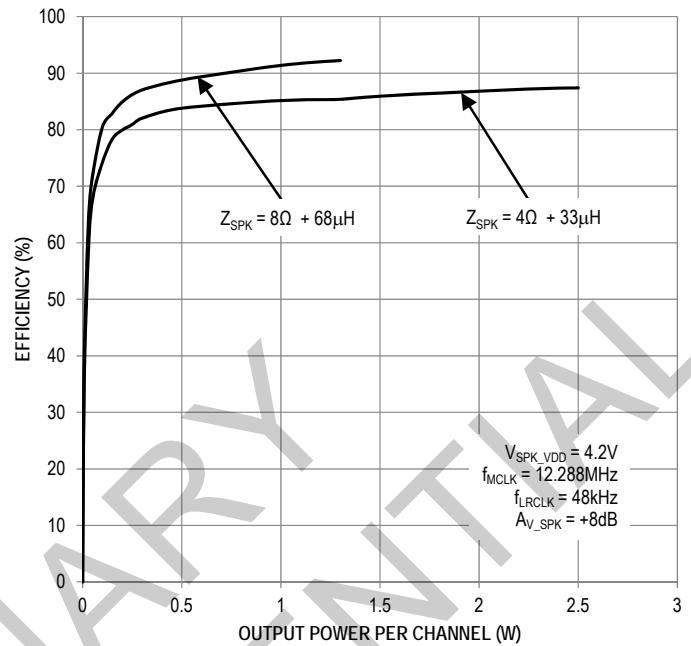
TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (DAC TO SPEAKER)TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (DAC TO SPEAKER)TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (DAC TO SPEAKER)TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (DAC TO SPEAKER)

TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (DAC TO SPEAKER)OUTPUT POWER vs SUPPLY VOLTAGE
(DAC TO SPEAKER)TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (DAC TO SPEAKER)OUTPUT POWER vs SUPPLY VOLTAGE
(DAC TO SPEAKER)

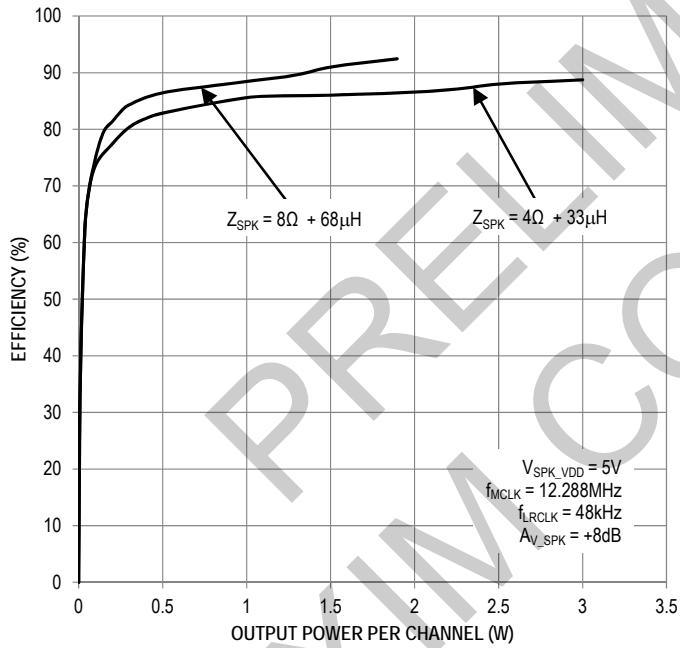
GAIN vs FREQUENCY (DAC TO SPEAKER)



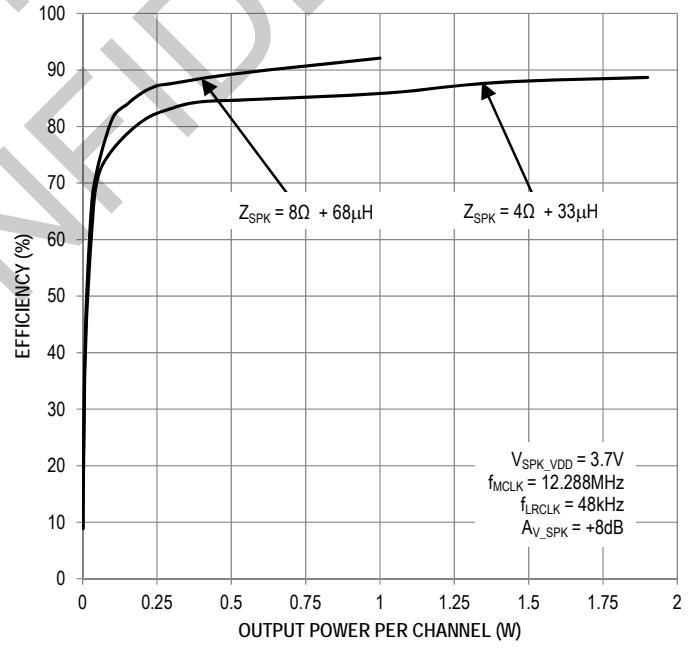
EFFICIENCY vs OUTPUT POWER (DAC TO SPEAKER)



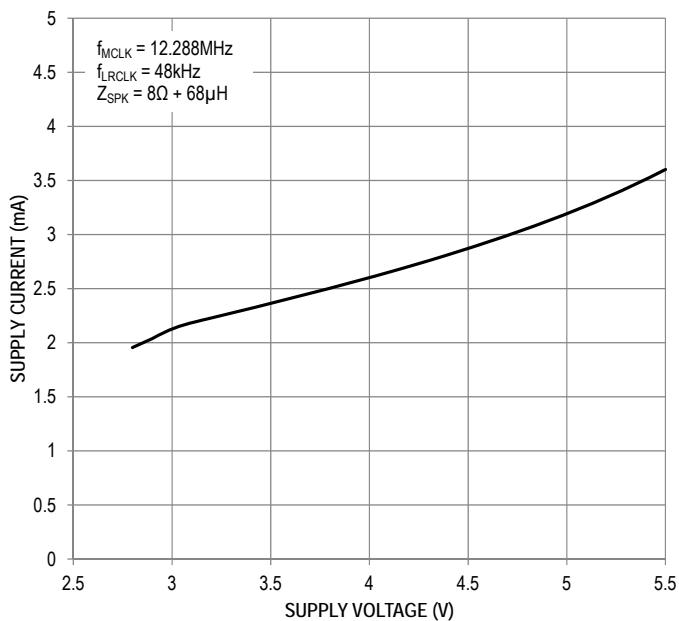
EFFICIENCY vs OUTPUT POWER (DAC TO SPEAKER)



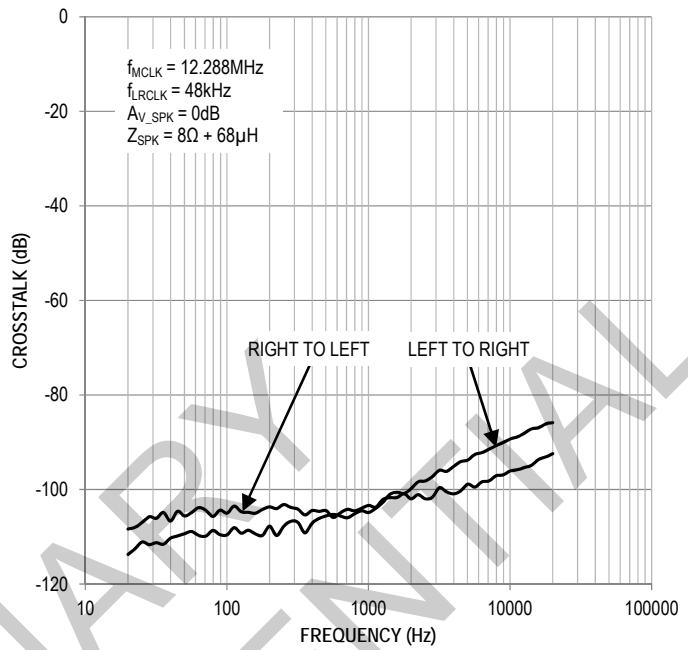
EFFICIENCY vs OUTPUT POWER (DAC TO SPEAKER)



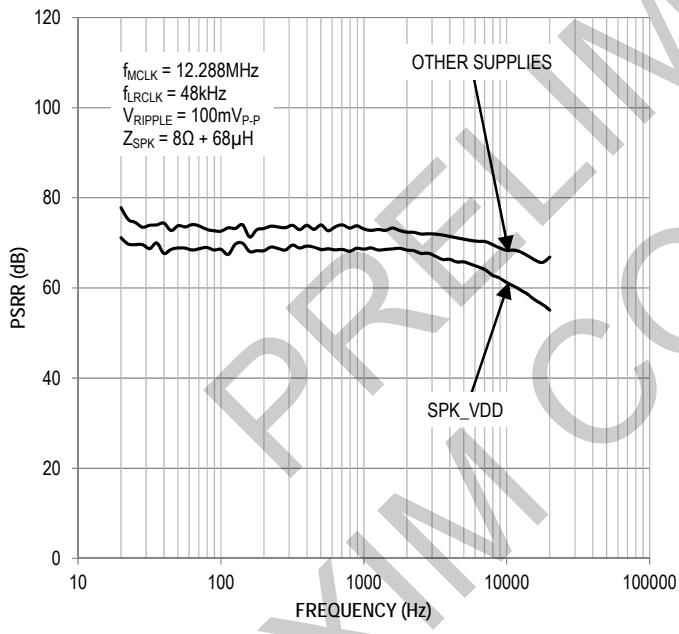
SUPPLY CURRENT vs SUPPLY VOLTAGE
(DAC TO SPEAKERS)

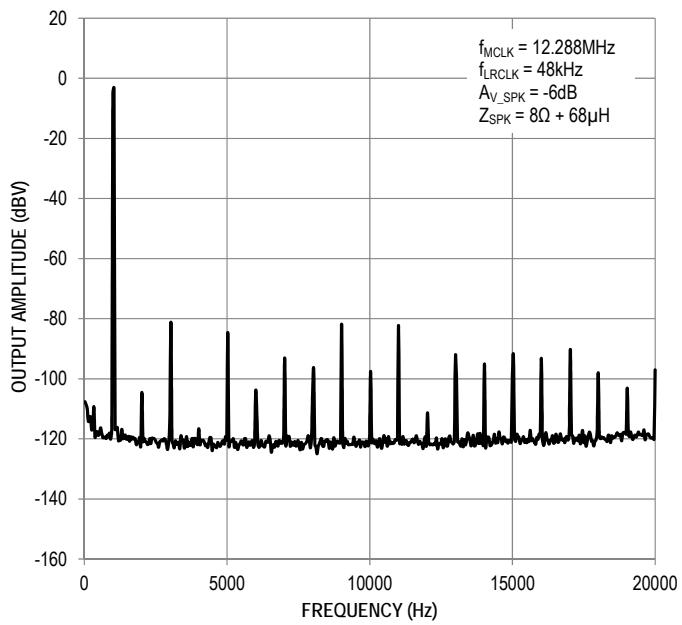
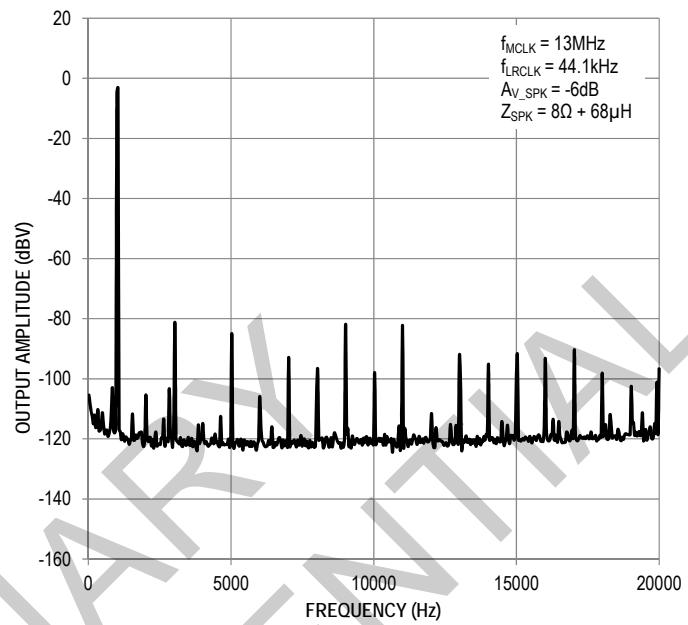
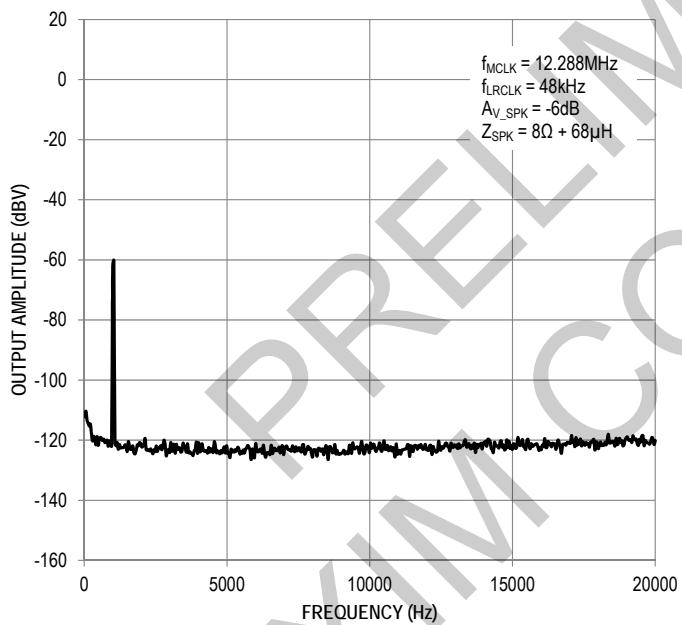
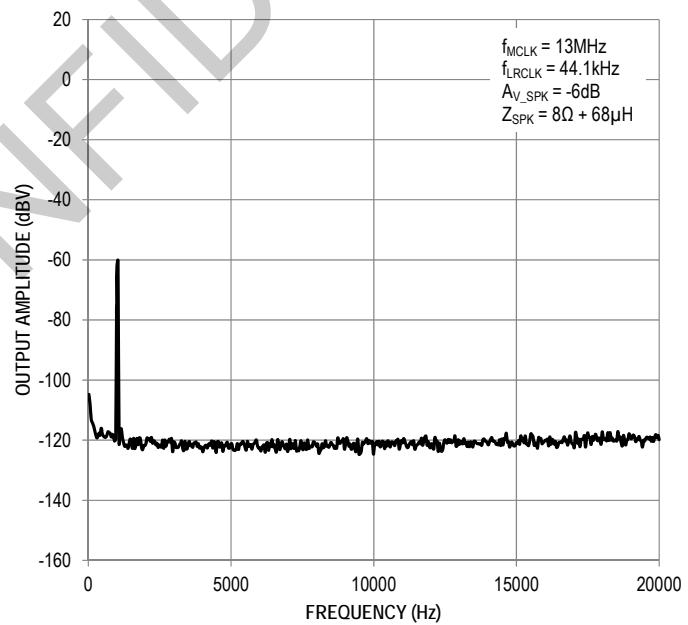


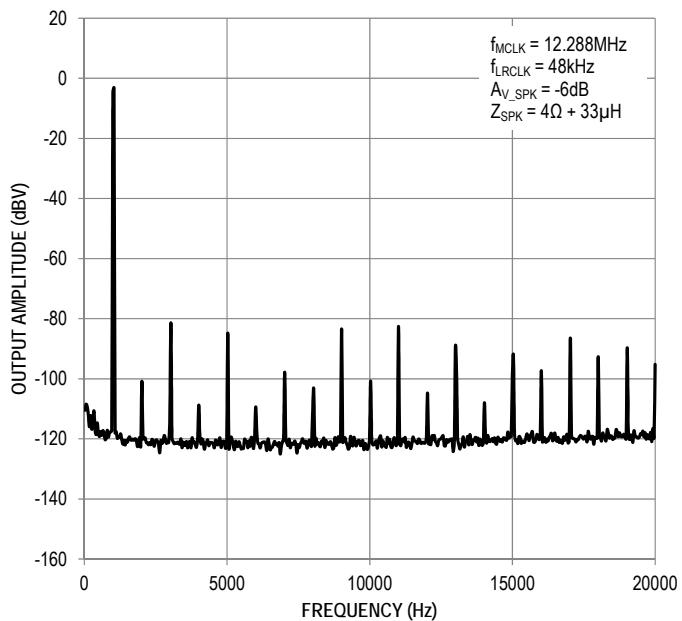
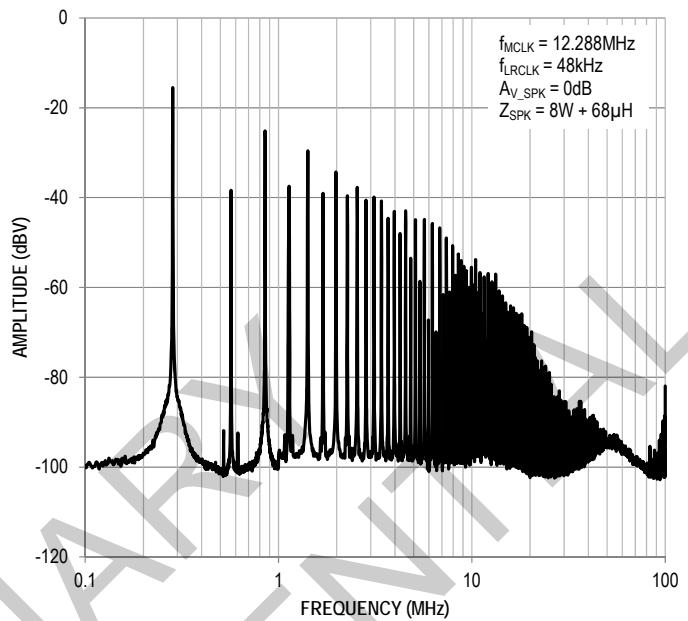
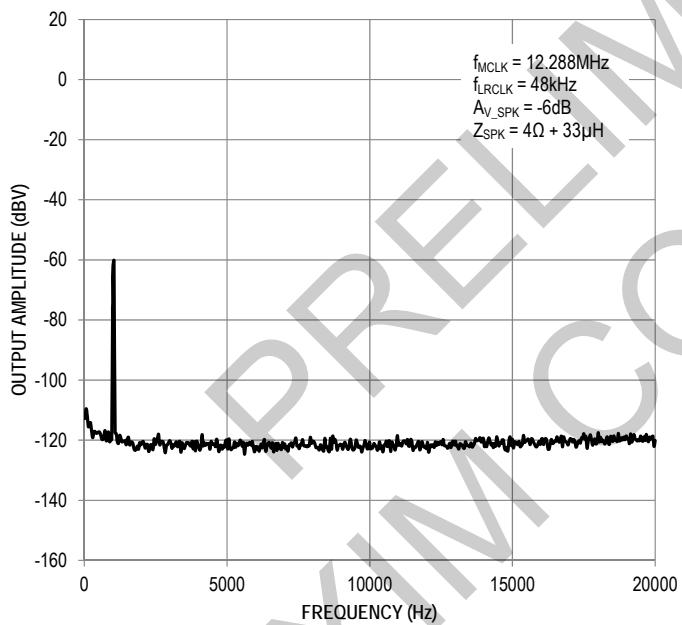
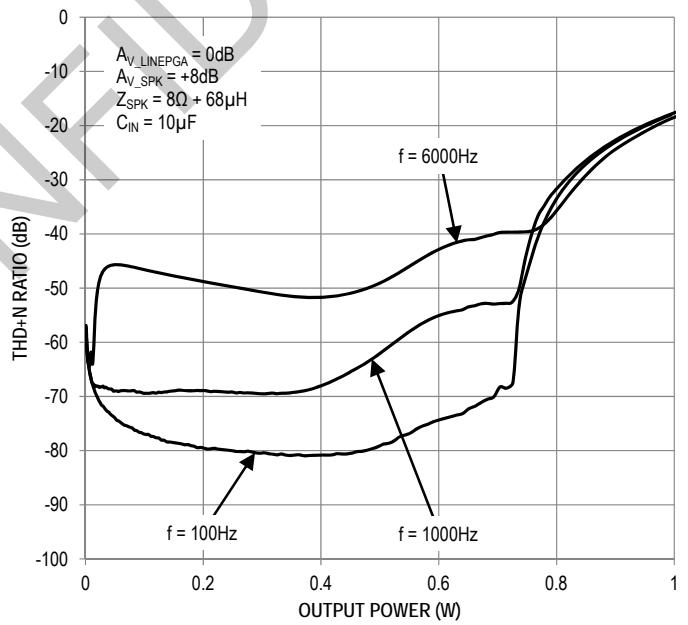
CROSSTALK vs FREQUENCY (DAC TO SPEAKERS)



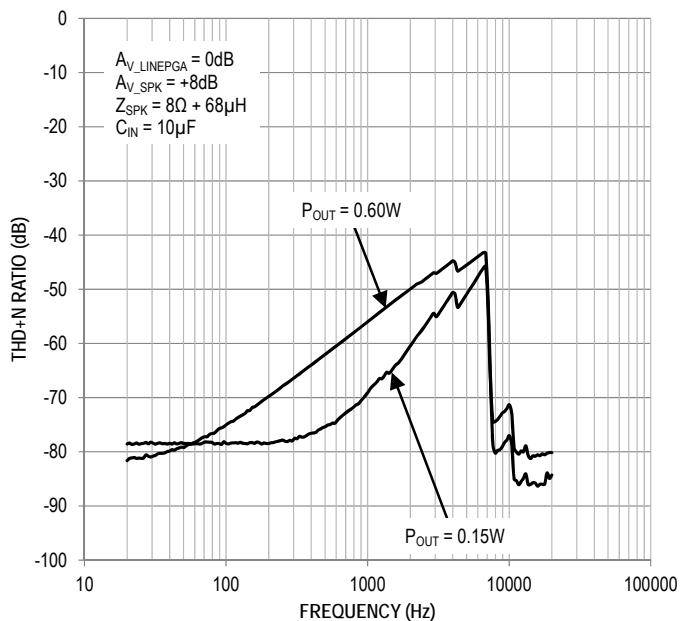
POWER SUPPLY REJECTION RATIO
vs FREQUENCY (DAC to SPEAKER)



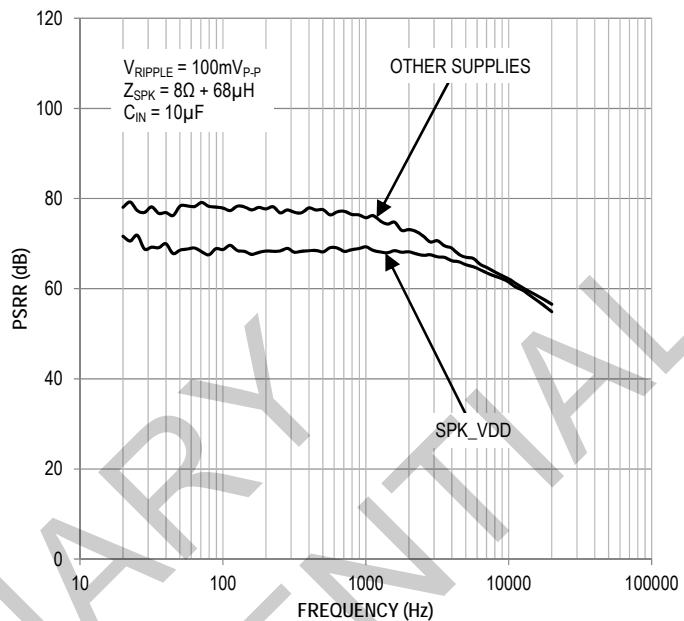
INBAND OUTPUT SPECTRUM,
-3dBFS INPUT (DAC TO SPEAKERS)INBAND OUTPUT SPECTRUM,
-3dBFS INPUT (DAC TO SPEAKERS)INBAND OUTPUT SPECTRUM,
-60dBFS INPUT (DAC TO SPEAKERS)INBAND OUTPUT SPECTRUM,
-60dBFS INPUT (DAC TO SPEAKERS)

INBAND OUTPUT SPECTRUM,
-3dBFS INPUT (DAC TO SPEAKERS)WIDEBAND FREQUENCY SPECTRUM
(DAC TO SPEAKERS)INBAND OUTPUT SPECTRUM,
-60dBFS INPUT (DAC TO SPEAKERS)TOTAL HARMONIC DISTORTION PLUS NOISE
vs OUTPUT POWER (LINE TO SPEAKER)

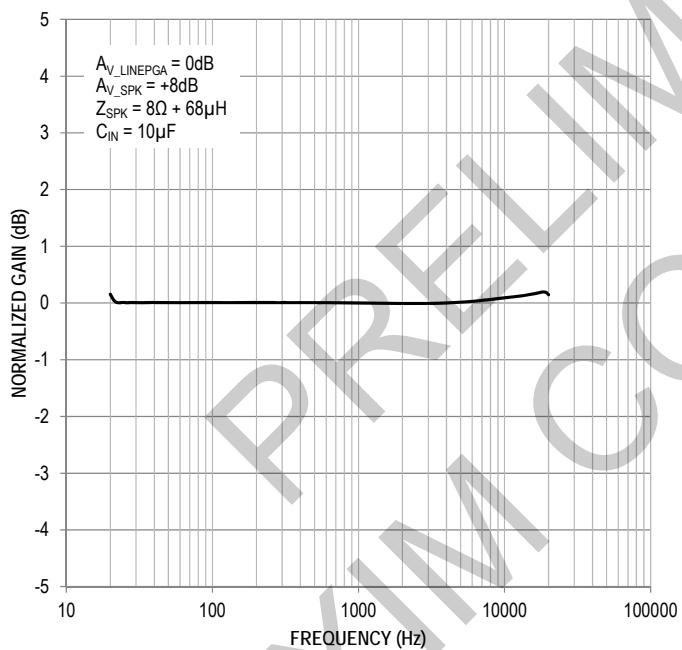
TOTAL HARMONIC DISTORTION PLUS NOISE vs
FREQUENCY (LINE TO SPEAKER)



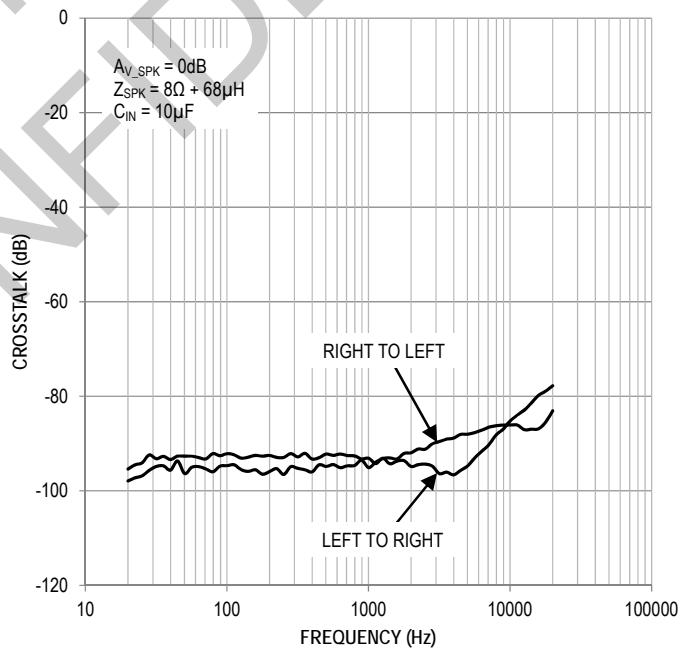
POWER SUPPLY REJECTION RATIO
vs FREQUENCY (LINE to SPEAKER)

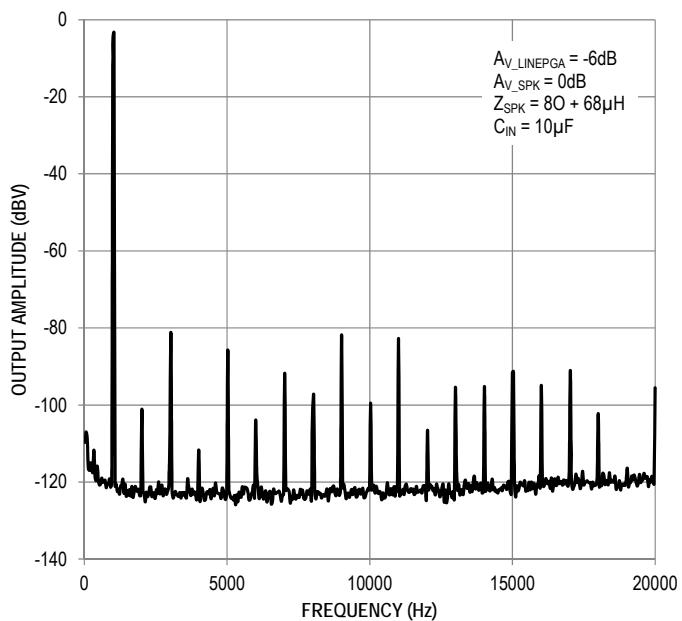
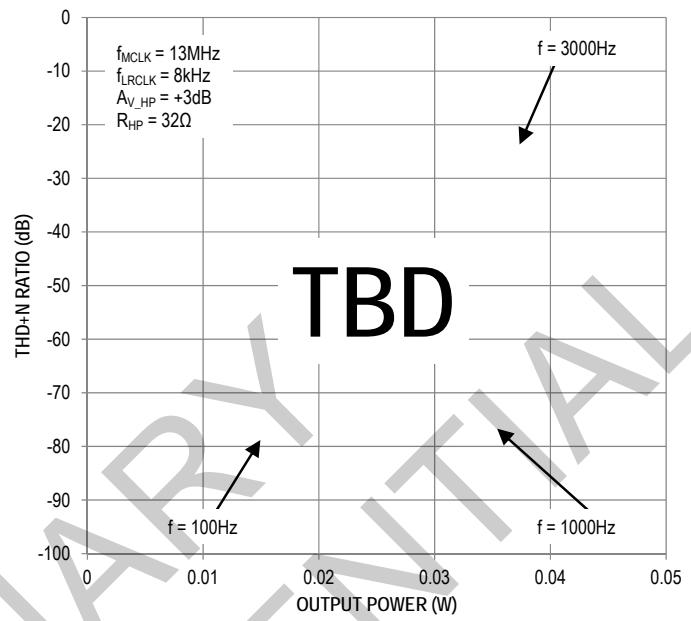
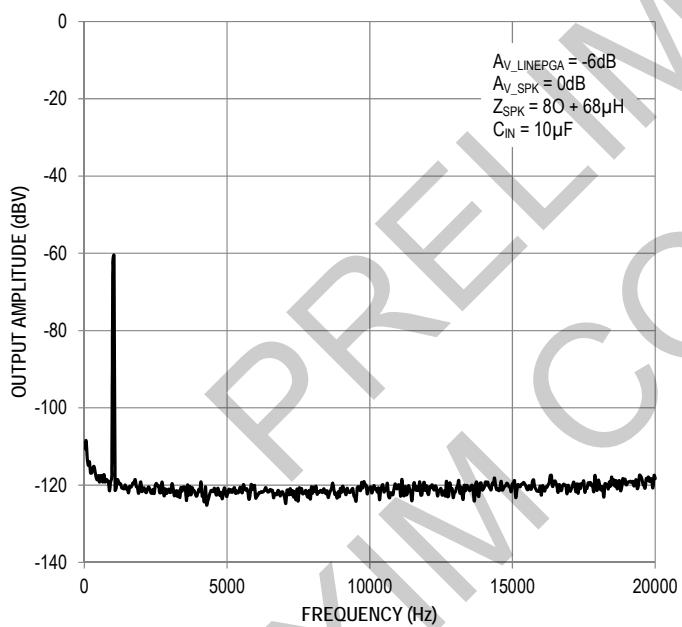
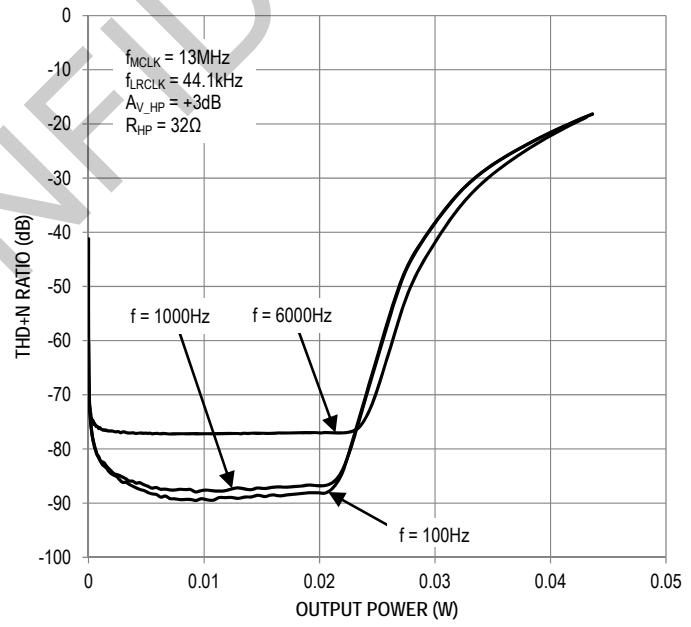


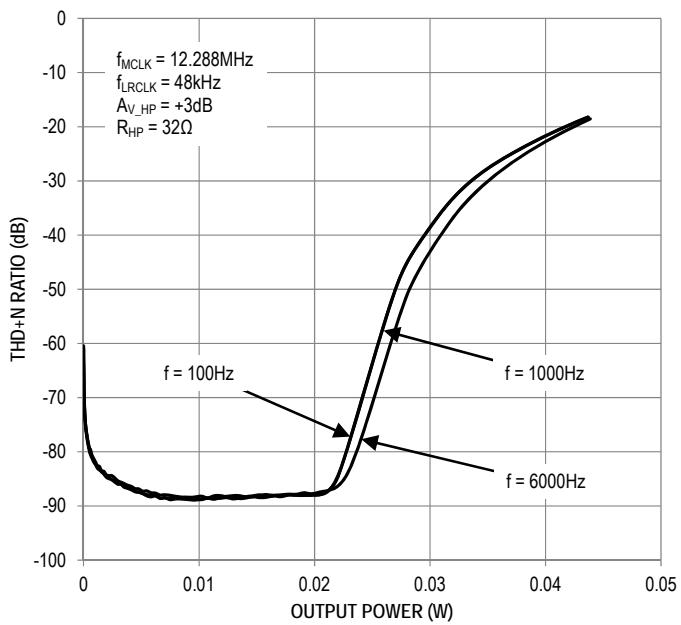
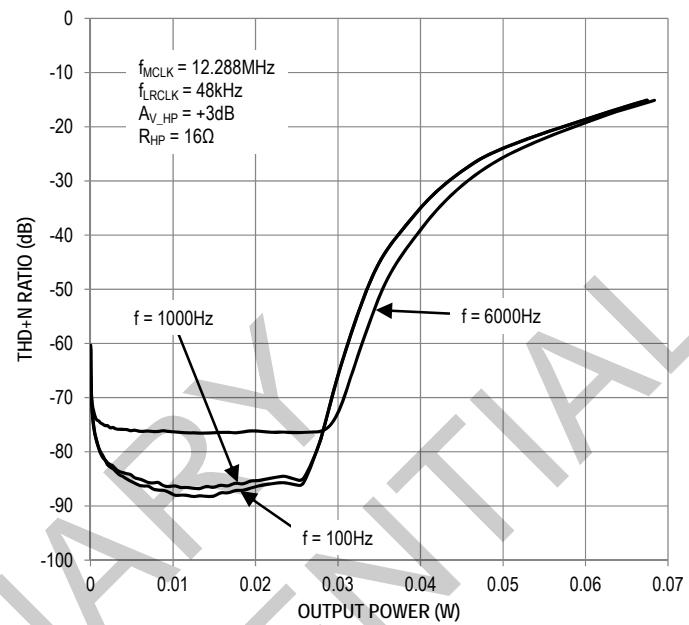
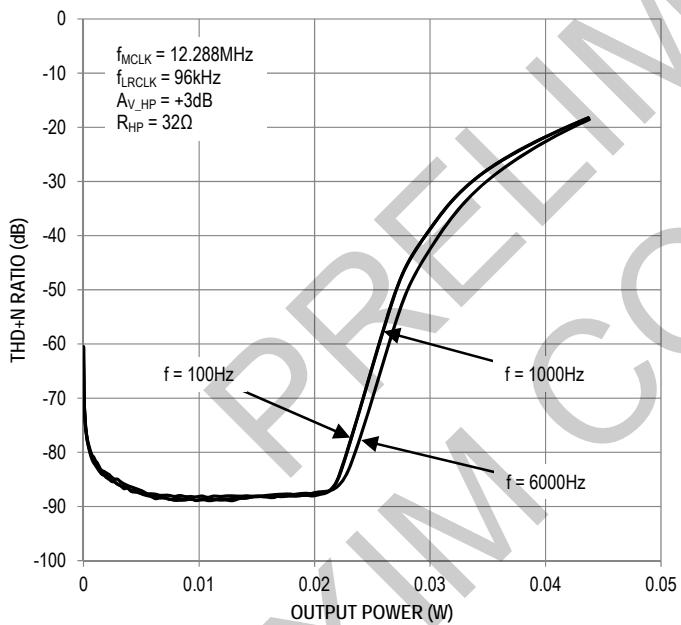
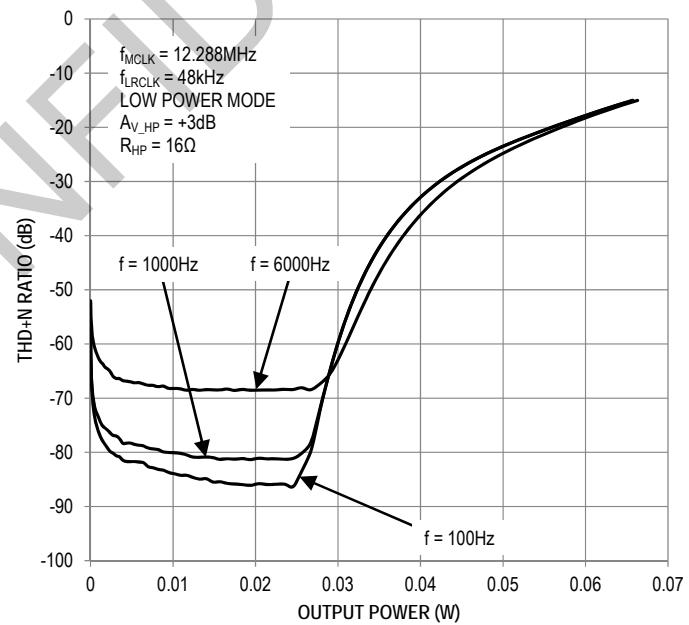
GAIN vs FREQUENCY (LINE TO SPEAKER)



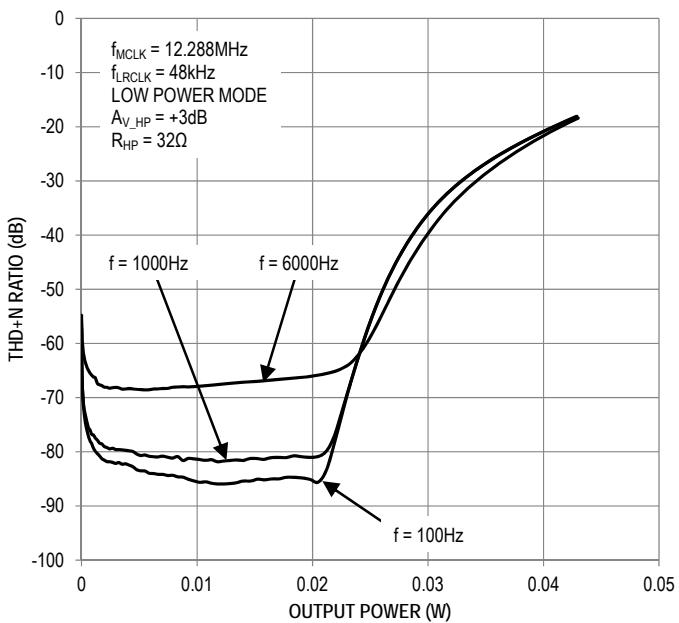
CROSSTALK vs FREQUENCY (LINE TO SPEAKER)



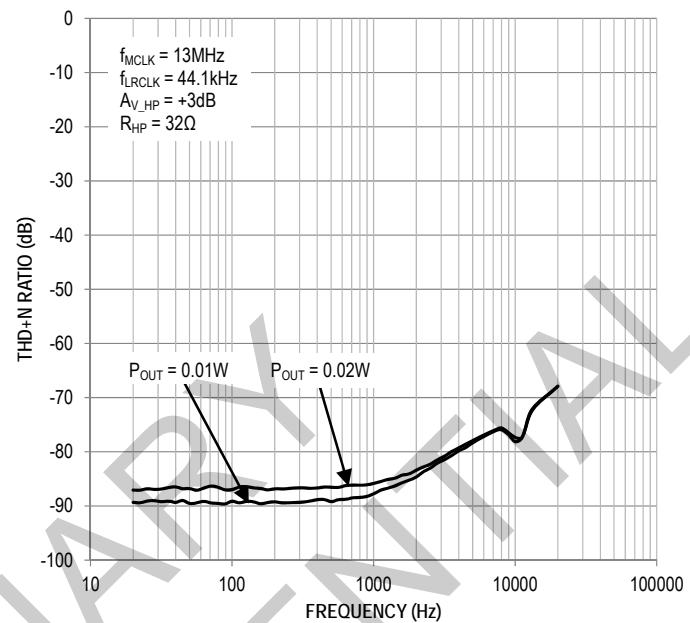
INBAND OUTPUT SPECTRUM,
-3dBV INPUT (LINE TO SPEAKERS)TOTAL HARMONIC DISTORTION PLUS NOISE
vs OUTPUT POWER (DAC TO HEADPHONE)INBAND OUTPUT SPECTRUM,
-60dBV INPUT (LINE TO SPEAKERS)TOTAL HARMONIC DISTORTION PLUS NOISE
vs OUTPUT POWER (DAC TO HEADPHONE)

TOTAL HARMONIC DISTORTION PLUS NOISE
vs OUTPUT POWER (DAC TO HEADPHONE)TOTAL HARMONIC DISTORTION PLUS NOISE
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vs OUTPUT POWER (DAC TO HEADPHONE)TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (DAC TO HEADPHONE)

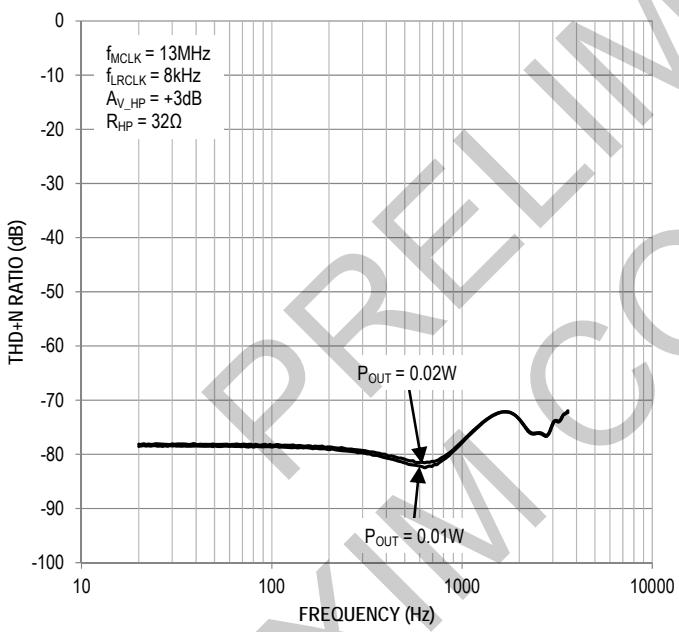
TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (DAC TO HEADPHONE)



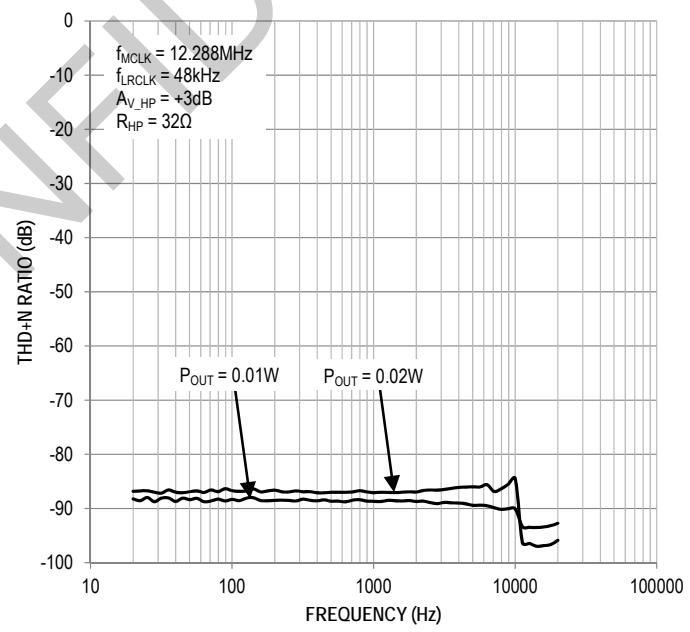
TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (DAC TO HEADPHONE)

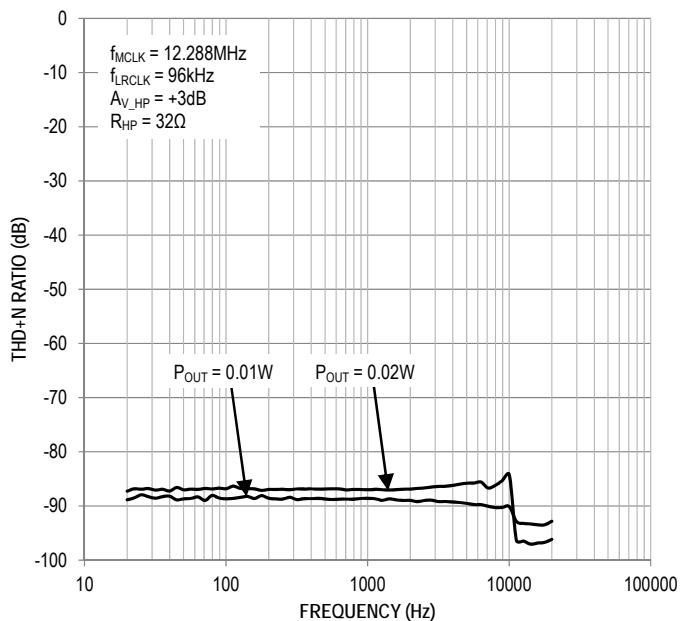
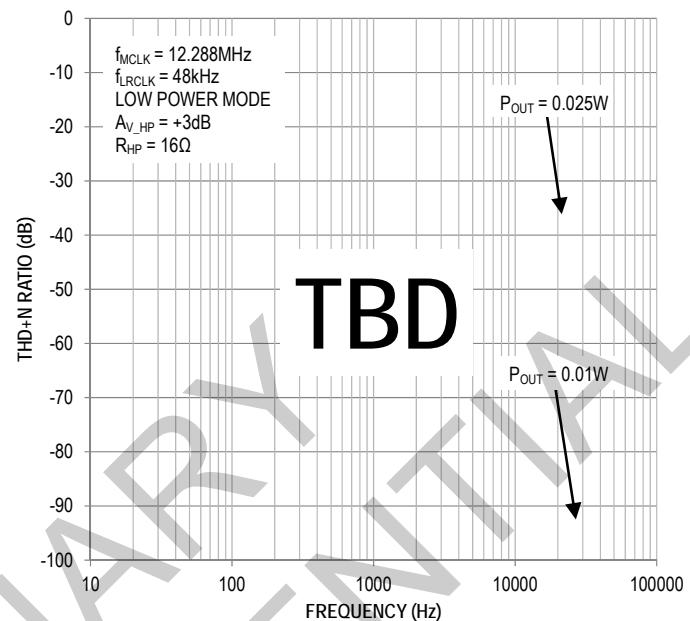
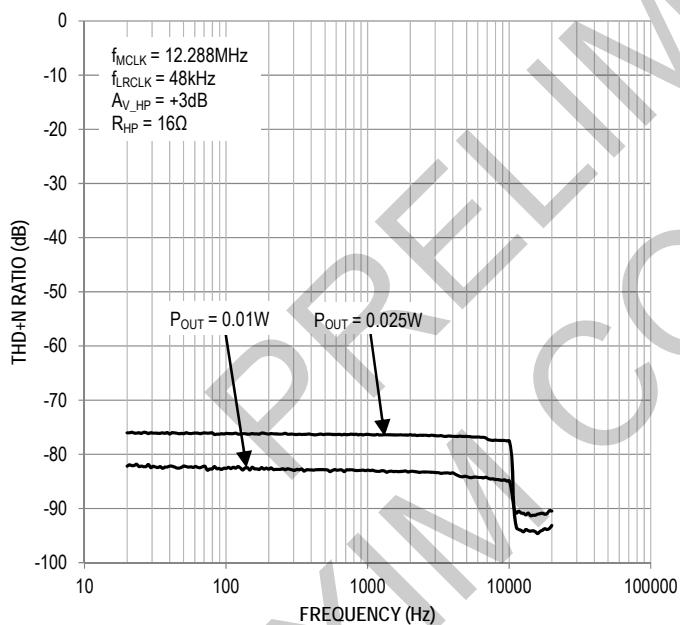
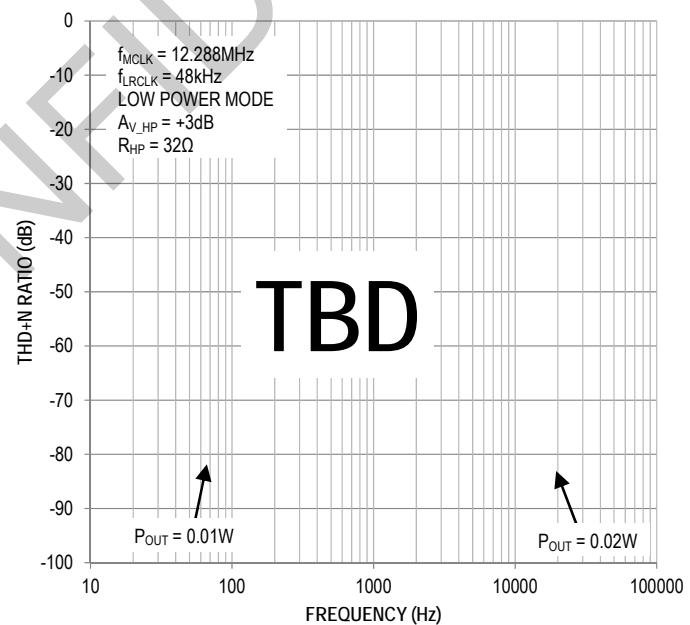


TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (DAC TO HEADPHONE)

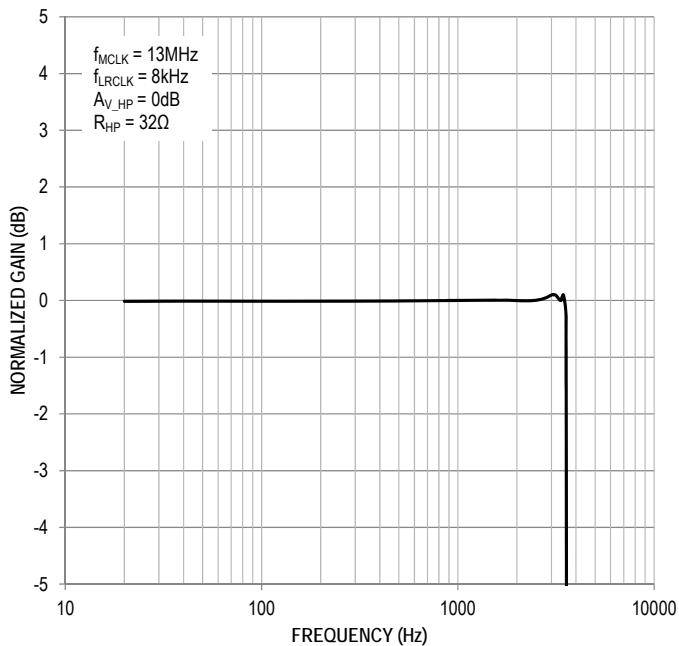


TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (DAC TO HEADPHONE)

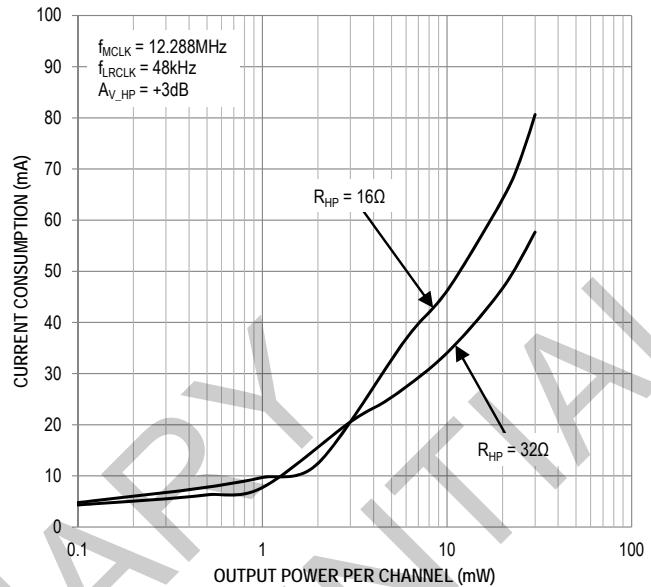


TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (DAC TO HEADPHONE)TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (DAC TO HEADPHONE)TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (DAC TO HEADPHONE)TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (DAC TO HEADPHONE)

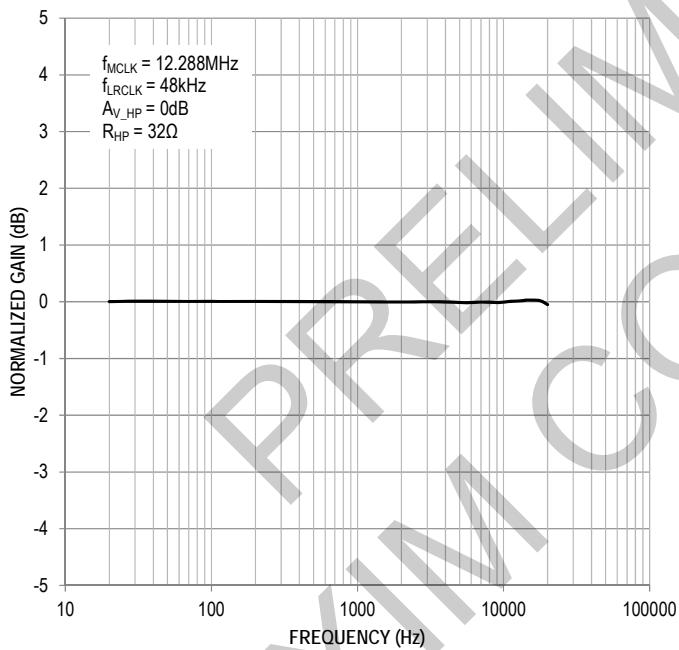
GAIN vs FREQUENCY (DAC TO HEADPHONE)



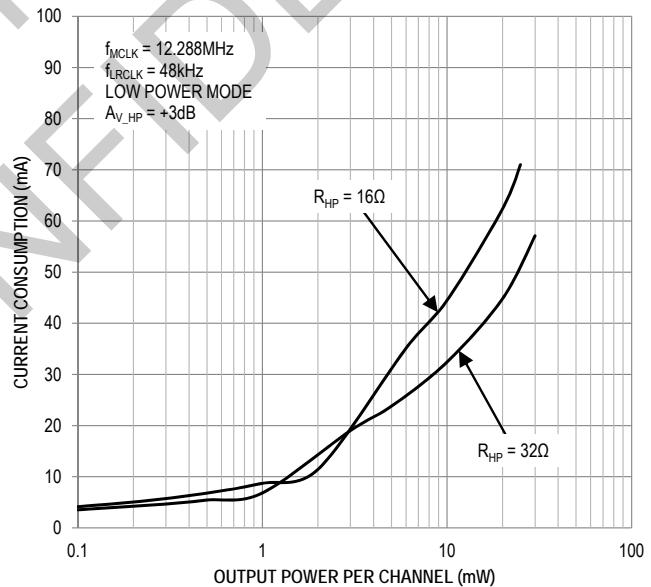
POWER CONSUMPTION vs OUTPUT POWER (DAC TO HEADPHONE)

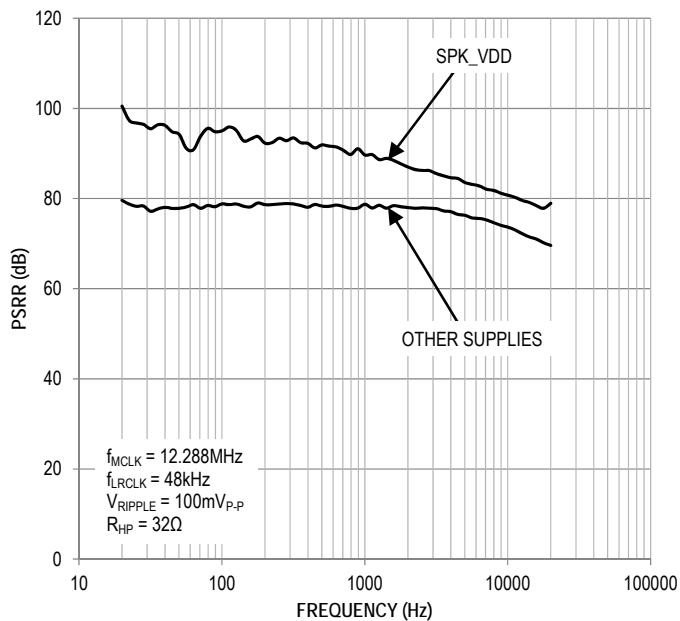


GAIN vs FREQUENCY (DAC TO HEADPHONE)

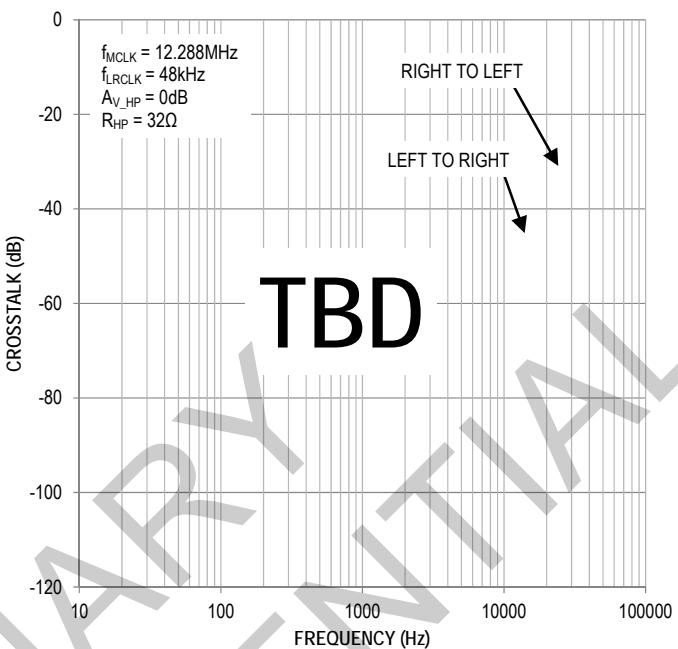
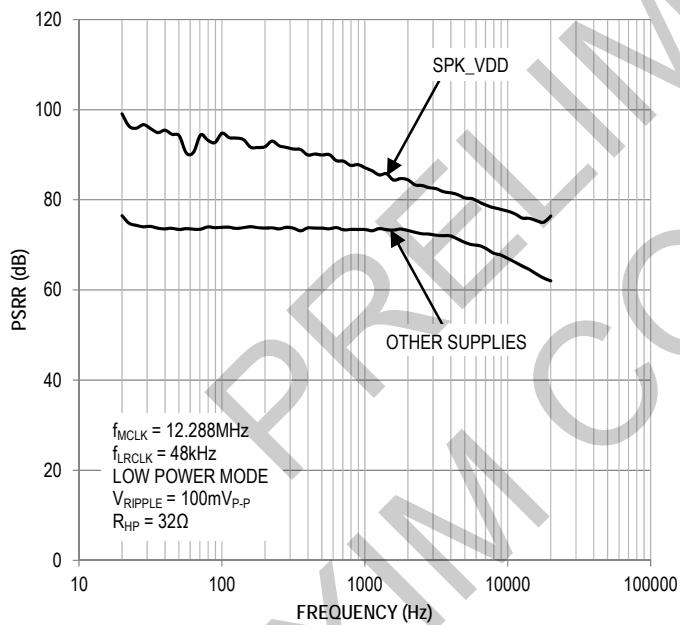


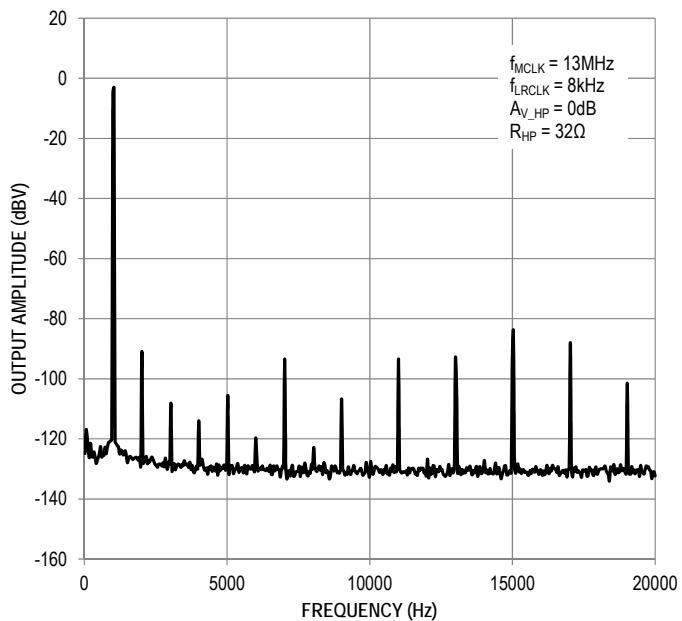
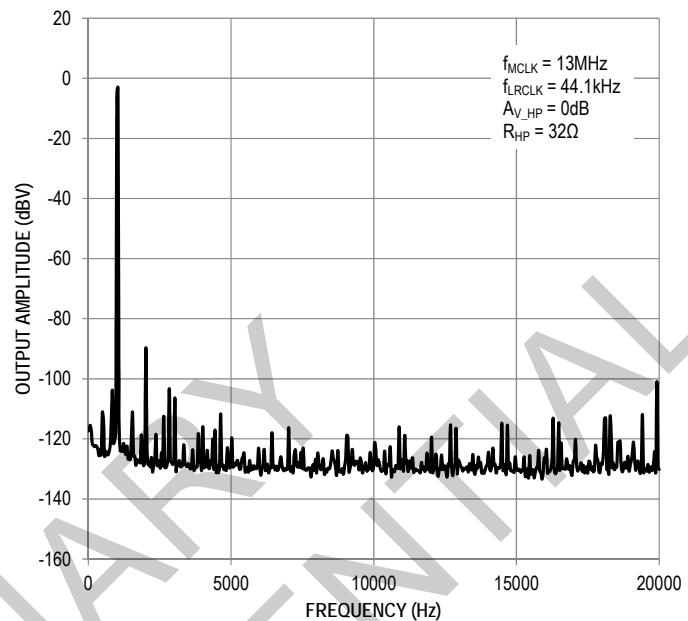
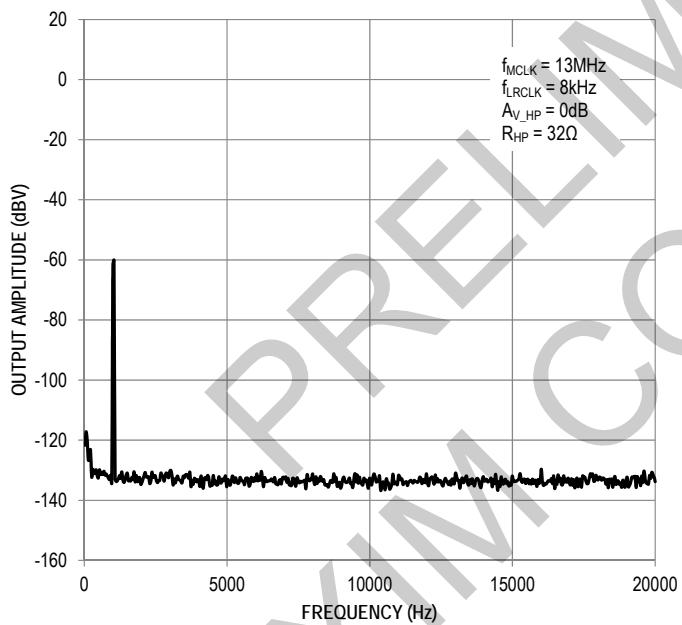
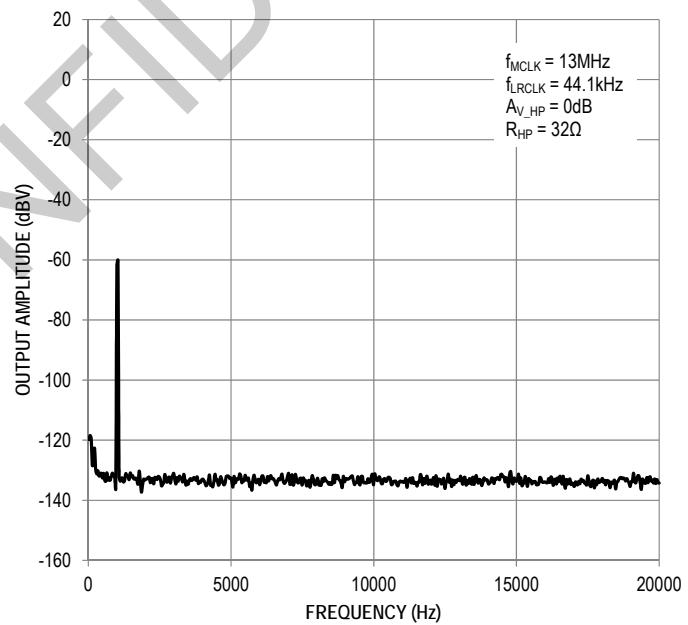
POWER CONSUMPTION vs OUTPUT POWER (DAC TO HEADPHONE)

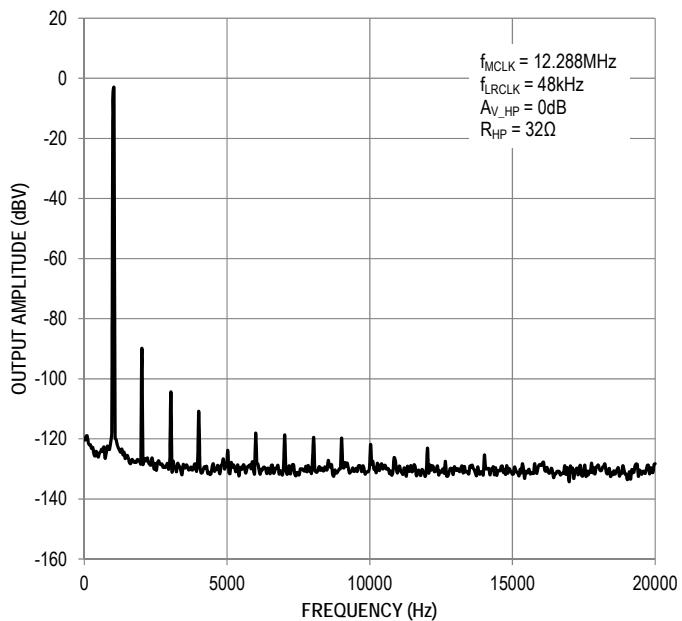
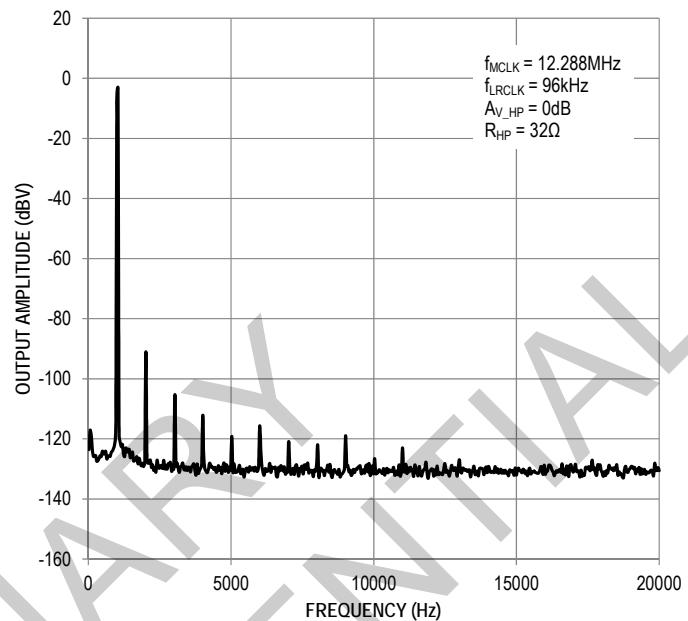
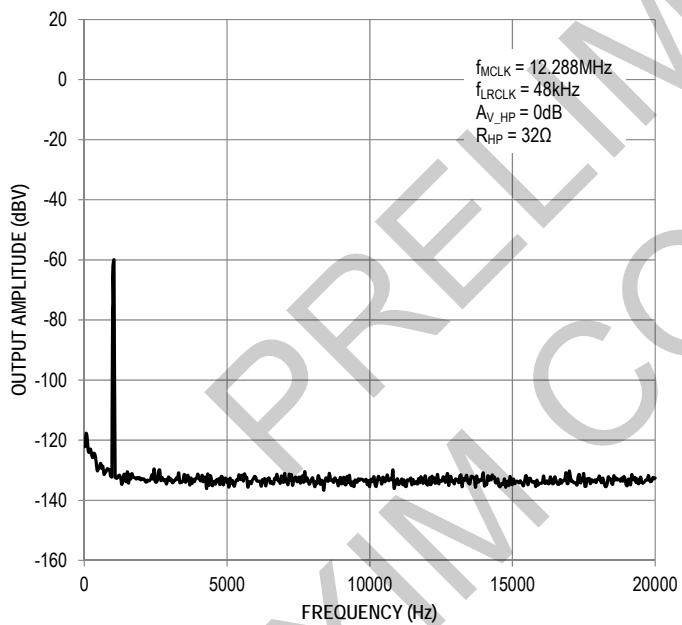
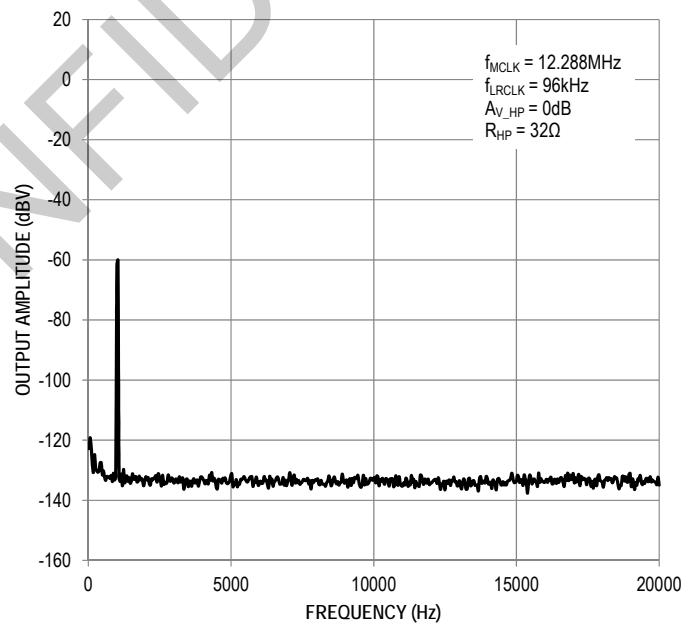


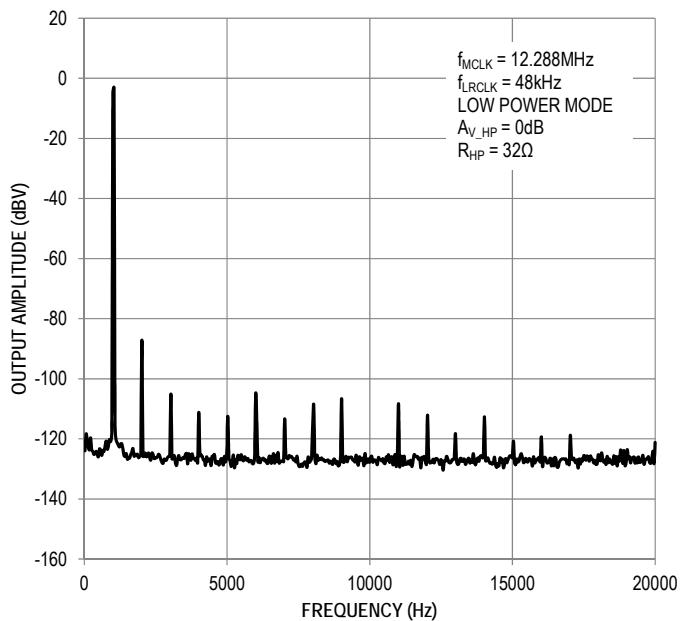
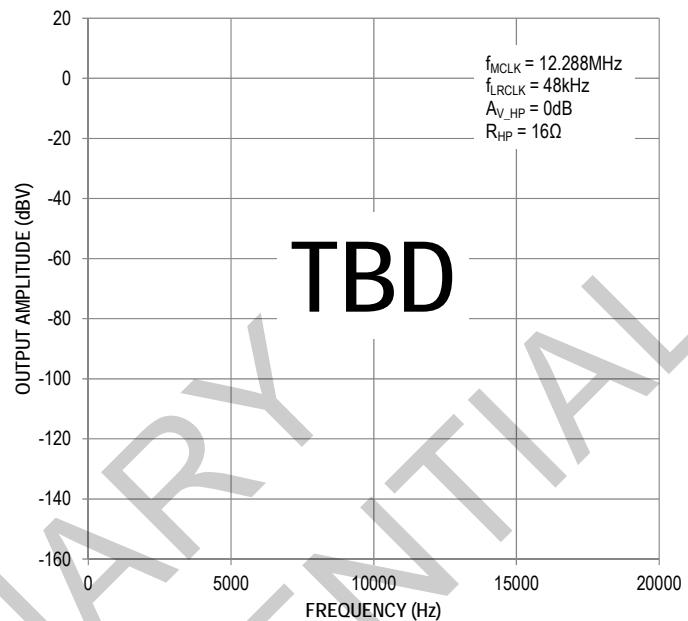
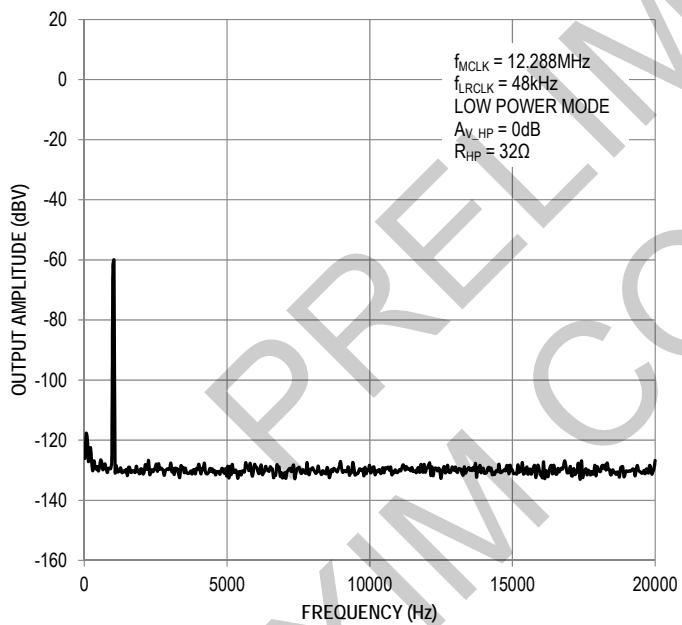
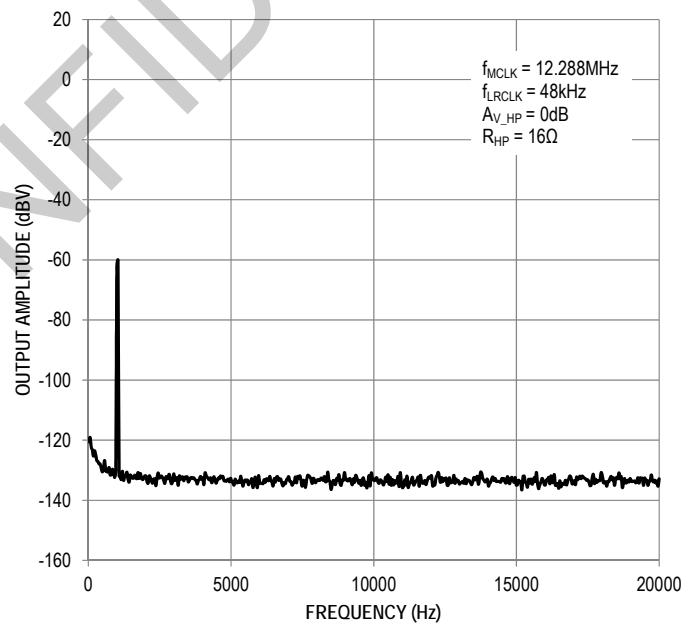
POWER SUPPLY REJECTION RATIO
vs FREQUENCY (DAC to HEADPHONES)

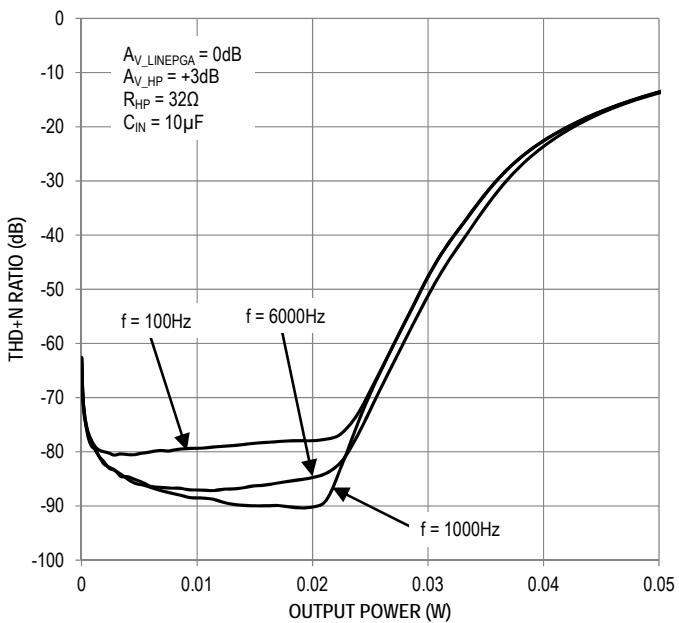
CROSSTALK vs FREQUENCY (DAC TO HEADPHONE)

POWER SUPPLY REJECTION RATIO
vs FREQUENCY (DAC to HEADPHONES)

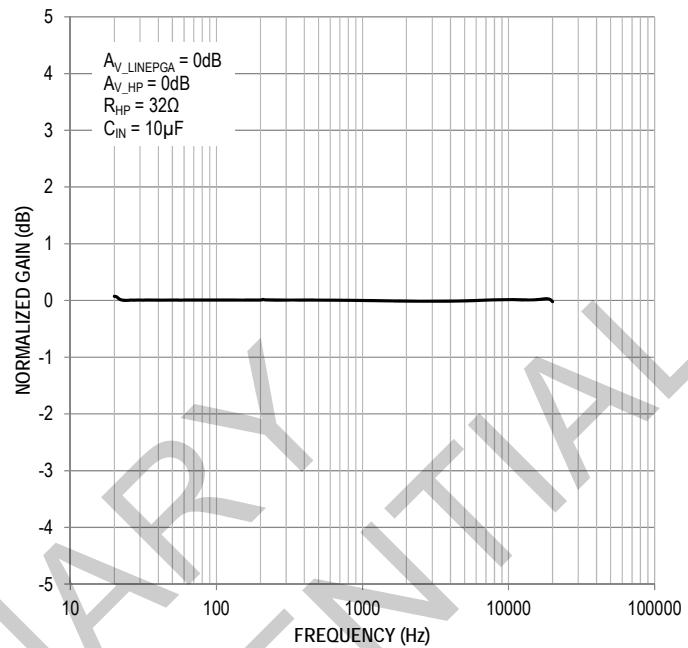
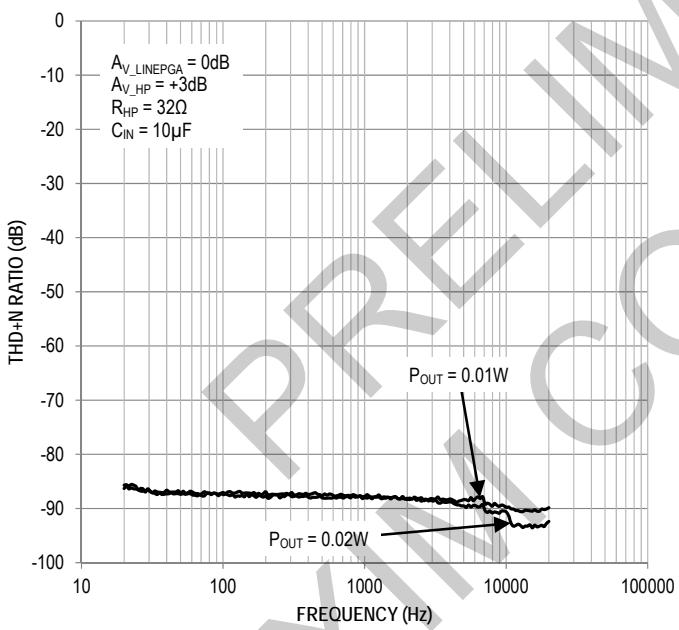
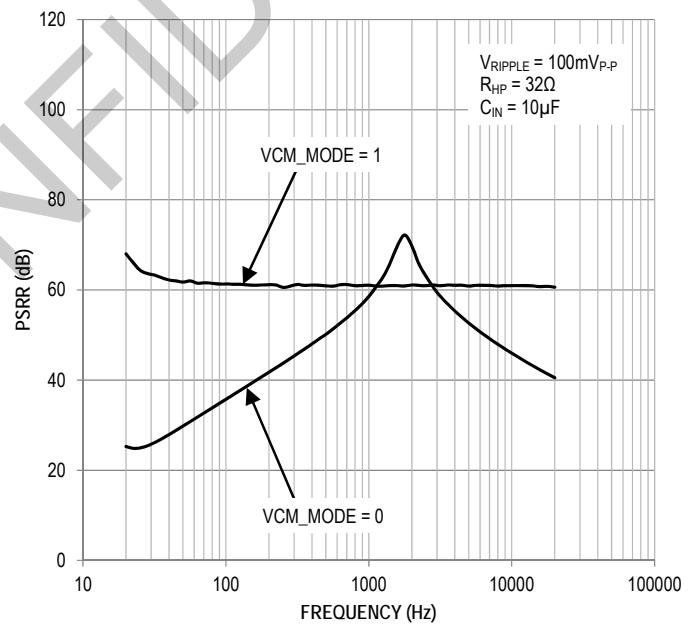
INBAND OUTPUT SPECTRUM,
-3dBFS INPUT (DAC TO HEADPHONE)INBAND OUTPUT SPECTRUM,
-3dBFS INPUT (DAC TO HEADPHONE)INBAND OUTPUT SPECTRUM,
-60dBFS INPUT (DAC TO HEADPHONE)INBAND OUTPUT SPECTRUM,
-60dBFS INPUT (DAC TO HEADPHONE)

INBAND OUTPUT SPECTRUM,
-3dBFS INPUT (DAC TO HEADPHONE)INBAND OUTPUT SPECTRUM,
-3dBFS INPUT (DAC TO HEADPHONE)INBAND OUTPUT SPECTRUM,
-60dBFS INPUT (DAC TO HEADPHONE)INBAND OUTPUT SPECTRUM,
-60dBFS INPUT (DAC TO HEADPHONE)

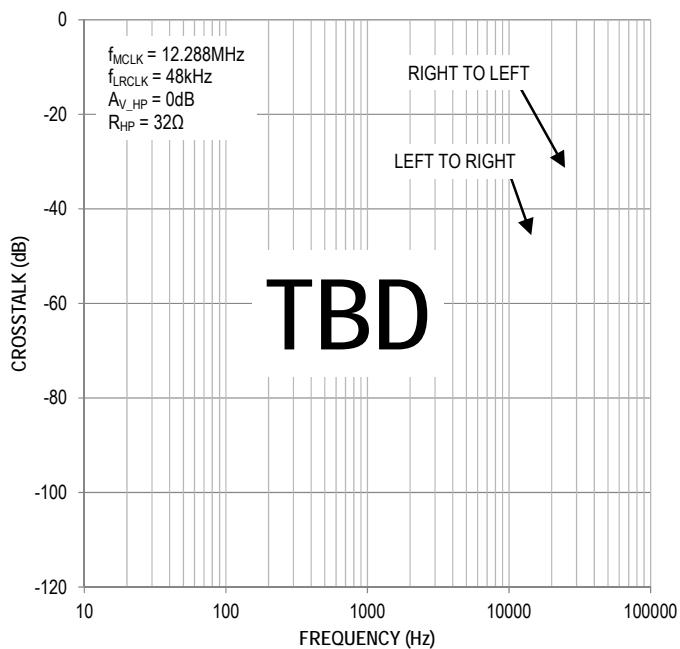
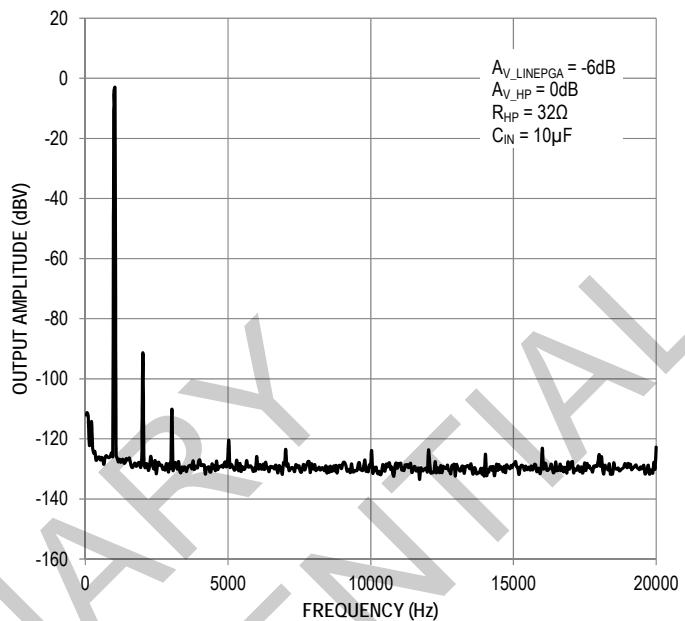
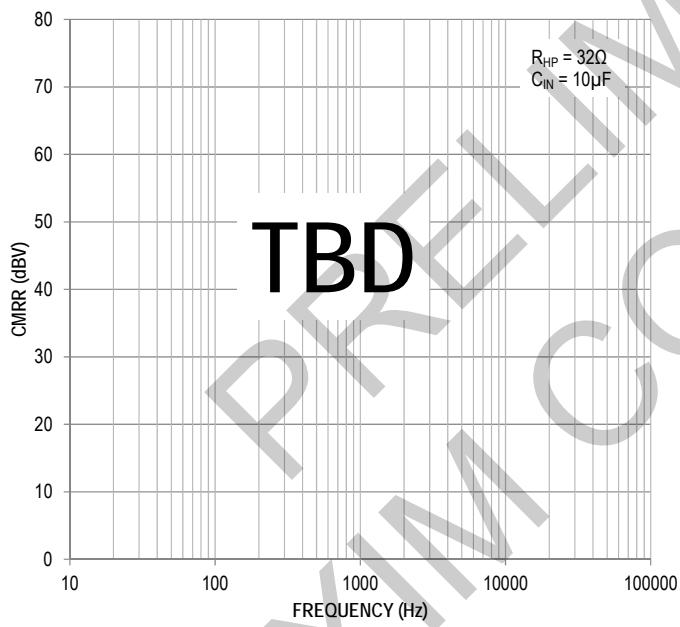
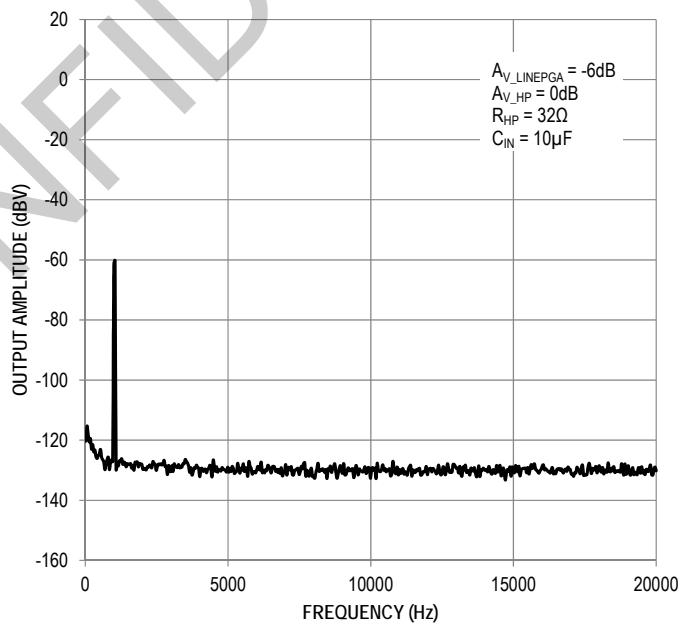
INBAND OUTPUT SPECTRUM,
-3dBFS INPUT (DAC TO HEADPHONE)INBAND OUTPUT SPECTRUM,
-3dBFS INPUT (DAC TO HEADPHONE)INBAND OUTPUT SPECTRUM,
-60dBFS INPUT (DAC TO HEADPHONE)INBAND OUTPUT SPECTRUM,
-60dBFS INPUT (DAC TO HEADPHONE)

TOTAL HARMONIC DISTORTION PLUS NOISE
vs OUTPUT POWER (LINE TO HEADPHONE)

GAIN vs FREQUENCY (LINE TO HEADPHONE)

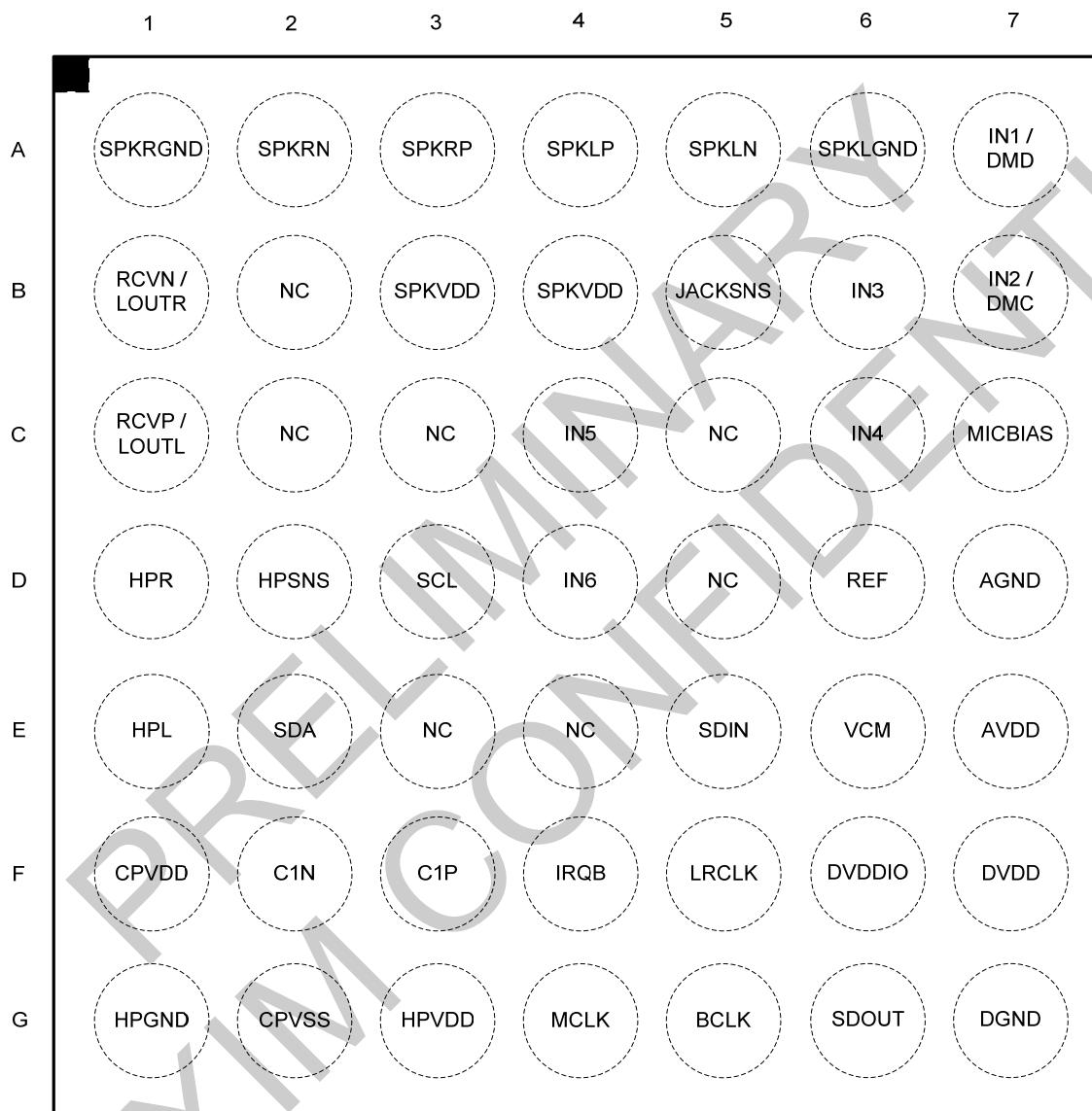
TOTAL HARMONIC DISTORTION PLUS NOISE
vs FREQUENCY (LINE TO HEADPHONE)POWER SUPPLY REJECTION RATIO
vs FREQUENCY (LINE to HEADPHONES)

CROSSTALK vs FREQUENCY (LINE TO HEADPHONE)

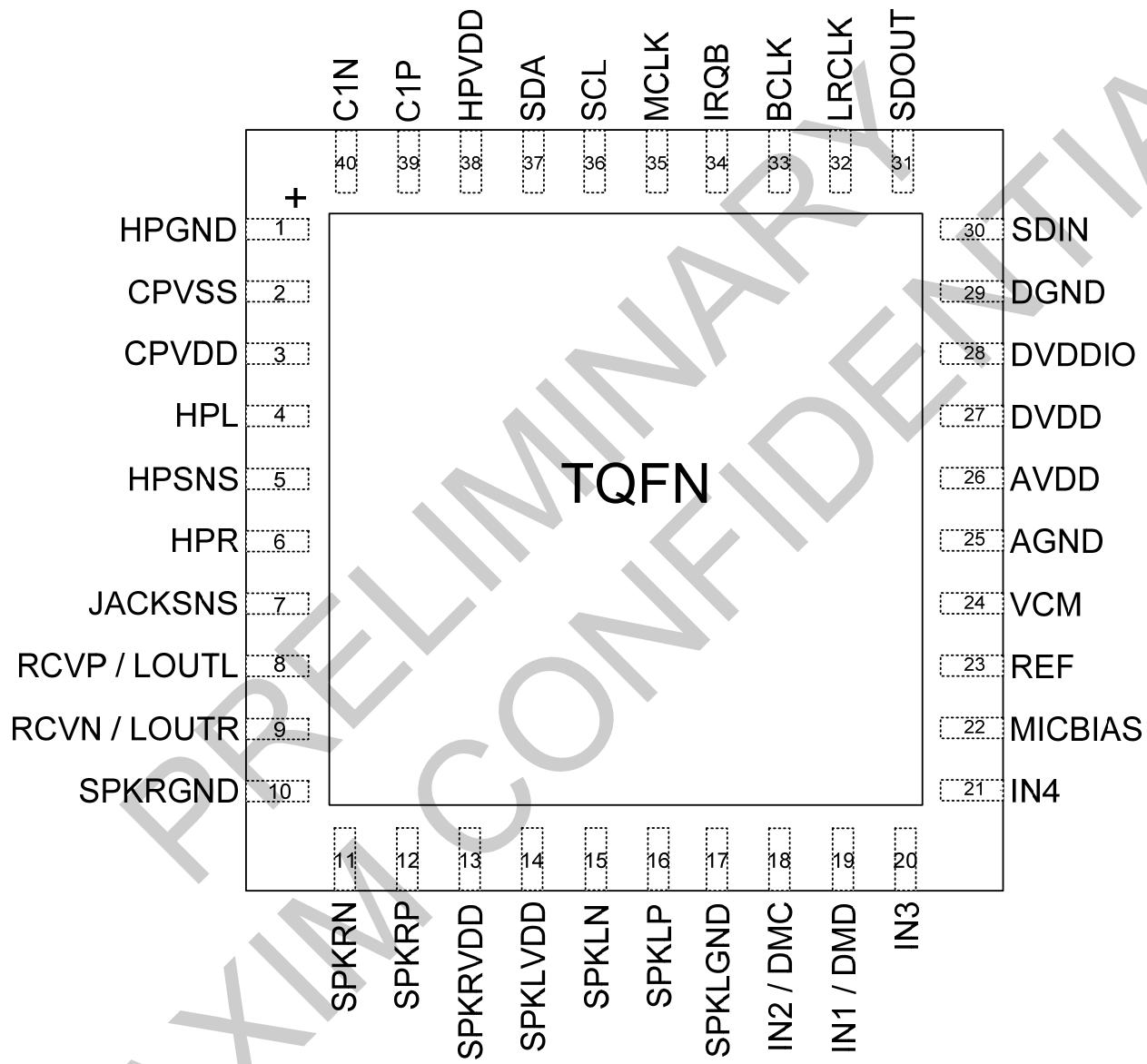
INBAND OUTPUT SPECTRUM,
-3dBV INPUT (LINE TO HEADPHONE)COMMON MODE REJECTION RATIO
vs FREQUENCY (LINE TO HEADPHONE)INBAND OUTPUT SPECTRUM,
-60dBV INPUT (LINE TO HEADPHONE)

BUMP CONFIGURATION (WLP)

Top View
Bump Side Down



MAX98090 – 49 BUMP WLP
0.4mm pitch

PIN CONFIGURATION (TQFN)

MAX98090 - 5mm x 5mm

PIN / BUMP DESCRIPTION

PIN TQFN	BUMP WLP	MAX98090	FUNCTION
1	G1	HPGND	Headphone Ground.
2	G2	CPVSS	Inverting Charge-Pump Output. Bypass to HPGND with a 1µF ceramic capacitor.
3	F1	CPVDD	Non-Inverting Charge-Pump Output. Bypass to HPGND with a 1µF ceramic capacitor.
4	E1	HPL	Left-Channel Headphone Output
5	D2	HPSNS	Headphone Amplifier Ground Sense. Connect to the headphone jack ground terminal or connect to ground.
6	D1	HPR	Right-Channel Headphone Output
7	B5	JACKSNS	Jack detection Input. Connect to the microphone terminal of the headset jack to detect jack activity.
8	C1	RCVP/LOUTL	Positive Earpiece Amplifier Output/Left Line Output
9	B1	RCVN/LOUTR	Negative Earpiece Amplifier Output/Right Line Output
10	A1	SPKRGND	Right Speaker Amplifier ground.
11	A2	SPKRN	Negative Right-Channel Class D Speaker Output
12	A3	SPKRP	Positive Right-Channel Class D Speaker Output
13	-	SPKRVDD	Right Speaker power supply. Bypass to SPKRGND with a 1µF capacitor.
14	-	SPKLVDD	Left Speaker and Microphone Bias Power Supply. Bypass to SPKLGND with a 1µF capacitor.
15	A5	SPKLN	Negative Left-Channel Class D Speaker Output
16	A4	SPKLP	Positive Left-Channel Class D Speaker Output
17	A6	SPKLGND	Left Speaker Amplifier Ground.
18	B7	IN2 / DMC	Positive Differential Microphone 1 Input or single-ended Line Input 2. AC-couple with a series 1µF capacitor. Can be retasked as a digital microphone clock output.
19	A7	IN1 / DMD	Negative Differential Microphone 1 Input or single-ended Line Input 1. AC-couple with a series 1µF capacitor. Can be retasked as a digital microphone data input.
20	B6	IN3	Negative Differential Microphone 2 Input or single-ended Line Input 3. AC-couple with a series 1µF capacitor.
21	C6	IN4	Positive Differential Microphone 2 Input or single-ended Line input 4. AC-couple with a series 1µF capacitor.
22	C7	MICBIAS	Low-Noise Bias Voltage. The bias voltage is programmable. An external resistor in the 2.2k to 1k range should be used to set the microphone current.
23	D6	REF	Converter Reference. Bypass to AGND with a 2.2µF capacitor.
24	E6	VCM	Common Mode Reference Voltage. Bypass to AGND with a 1µF capacitor.
25	D7	AGND	Analog Ground.
26	E7	AVDD	Analog Power Supply. Bypass to AGND with a 1µF capacitor.
27	F7	DVDD	Digital Power Supply. Bypass to DGND with a 1µF capacitor.
28	F6	DVDDIO	Digital Audio Interface Power-Supply Input. Bypass to DGND with a 1µF capacitor.
29	G7	DGND	Digital Ground
30	E5	SDIN	Digital Audio Serial Data DAC Input
31	G6	SDOUT	Digital Audio Serial Data ADC Output. The output voltage is referenced to DVDDIO.
32	F5	LRCLK	Digital Audio Left-Right Clock Input/Output. LRCLK is the audio sample rate clock and determines whether audio data is routed to the left or right channel. In TDM mode, LRCLK is a frame sync pulse. LRCLK is an input when the AX49 is in slave mode and an output when in master mode.

33	G5	BCLK	Digital Audio Bit Clock Input/Output. BCLK is an input when the IC is in slave mode and an output when in master mode. The input/output voltage is referenced to DVDDIO.
34	F4	/IRQ\	Active Low Hardware Interrupt Output. Connect a 10KΩ pull-up resistor to VDD.
35	G4	MCLK	Master Clock Input. Acceptable input frequency range is 10MHz to 60MHz.
36	D3	SCL	I ² C Serial Clock Input. Connect a pull-up resistor to DVDD for full output swing.
37	E2	SDA	I ² C Serial Data Input/Output. Connect a pull-up resistor to DVDD for full output swing.
38	G3	HPVDD	Headphone Power Supply. Bypass to HPGND with a 1µF capacitor.
39	F3	C1P	Charge-Pump Flying Capacitor Positive Terminal. Connect a 1µF ceramic capacitor between C1N and C1P.
40	F2	C1N	Charge-Pump Flying Capacitor Negative Terminal. Connect a 1µF ceramic capacitor between C1N and C1P.
-	B3, B4	SPKVDD	Speaker and Microphone Bias Power Supply. Bypass to SPK_GND with a 1µF capacitor.
-	C4	IN5	Auxiliary Negative Differential Microphone Input or single-ended line input AC-couple with a series 1µF capacitor.
-	D4	IN6	Auxiliary Positive Differential Microphone Input or single-ended line input AC-couple with a series 1µF capacitor.
-	B2, C2, C3, C5, D5, E3, E4	NC	Not internally connected.

DETAILED DESCRIPTION

The MAX98090 is a fully integrated stereo audio codec with FLEXSOUND audio processing and integrated input and output audio amplifiers.

The device features either six (WLP package) or four (TQFN package) flexible analog inputs. Each pair can be configured as a differential analog microphone input, a single ended or differential Line input(s), or as a reduced power, direct differential analog input to the ADC mixer. One input pair, IN1/IN2, can also be re-tasked to support two digital microphones. As a result, any combination of two microphones (either analog or digital) can be recorded from simultaneously. The input analog signals are amplified by up to 50dB, and then are either recorded by the stereo ADC or routed directly to the analog output mixers for playback.

The ADC supports sample rates between 8kHz and 96kHz, an optional dither enable, and features two performance modes and oversampling rates. The ADC to DAI recording path features both voice (IIR) and Music (FIR) filtering, optional DC blocking and configurable biquad filters, and up to 21dB of programmable digital gain and level control.

The digital audio interface (DAI) can simultaneously transmit and receive separate and distinct stereo audio signals in a wide range of formats including I²S, LJ, RJ, and up to four slots in TDM. Like the ADC to DAI recording path, the DAI to DAC playback path supports sample rates from 8kHz to 96kHz, both voice (IIR) and Music (FIR) filtering (high stop band attenuation at fs/2), optional DC blocking filters, and up to 18dB of digital gain and level control. In addition, the DAI playback path also features a 7 band parametric biquad equalizer, automatic level control (ALC) with up to 12dB of compression, and a summing digital sidetone from the ADC recording path.

The MAX98090 includes three analog output drivers. The first is a differential receiver / earpiece BTL amplifier. Alternatively, the receiver amplifier can also be configured a stereo single ended line output.

The second is an integrated, filterless, class D stereo speaker amplifier. This amplifier provides efficient amplification for two speakers, and includes active emissions limiting to minimize the radiated emissions (EMI) traditionally associated with class D. The right channel features a slave mode where the switching is synchronized to that of the left channel to eliminate the beat tone that can occur with asynchronous operation. In most systems, no output filtering is required.

Finally, the third is a class H, ground referenced stereo headphone amplifier featuring Maxim's second generation DirectDrive architecture. The class H headphone amplifiers use a charge pump to generate a ground referenced output signal. This eliminates the need for either DC blocking capacitors or a mid-rail bias for the headphone jack ground return. The charge pump generates both the positive and negative supply for the headphone amplifier. A tracking circuit monitors the input signal level and automatically selects between two supply voltage levels based on the signal level. For low signal levels the charge pump outputs HPVDD / 2 and -HPVDD / 2 for improved efficiency. For high signal levels the charge pump outputs HPVDD and -HPVDD to maximum output power. Ground sense reduces output noise caused by ground return current.

Device I²C Register Map

Table 1 lists all of the registers, their addresses, and power-on-reset (PoR) states. Registers 0x01, 0x02 and 0xFF are read-only. Register 0x00, and all of the remaining registers, are read/write. Write zeros to all unused bits in the register table when updating the register, unless otherwise noted.

Table 1: MAX98090 Control Register Map (Register Bits in Bold are WLP Package Only)

REGISTER DESCRIPTION			REGISTER CONTENTS								POR STATE	DS PAGE			
ADDR	NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0					
RESET / STATUS / INTERRUPT REGISTERS															
0x00	SOFTWARE RESET	W	SWRESET	-	-	-	-	-	-	-	0x00	116			
0x01	DEVICE STATUS	CoR	CLD	SLD	ULK	-	-	JDET	ALCACT	ALCCLP	0x00	112			
0x02	JACK STATUS	R	-	-	-	-	-	LSNS	JKSNS	-	0x00	111			
0x03	INTERRUPT MASKS	R/W	ICLD	ISLD	IULK	-	-	IJDET	IALCACT	IALCCLP	0x04	113			
QUICK SETUP REGISTERS															
0x04	SYSTEM CLOCK	W	26M	19P2M	13M	12P288M	12M	11P2896M	-	256Fs	0x00	114			
0x05	SAMPLE RATE	W	-	-	SR_96K	SR_32K	SR_48K	SR_44K1	SR_16K	SR_8K	0x00	114			
0x06	DAI INTERFACE	W	-	-	RJ_M	RJ_S	LJ_M	LJ_S	I2S_M	I2S_S	0x00	114			
0x07	DAC PATH	W	DIG2_HP	DIG2_EAR	DIG2_SPK	DIG2_LOUT	-	-	-	-	0x00	115			
0x08	MIC/DIRECT TO ADC	W	IN12_MIC1	IN34_MIC2	IN56_MIC1	IN56_MIC2	IN12_DADC	IN34_DADC	IN56_DADC	-	0x00	115			
0x09	LINE TO ADC	W	IN12S_AB	IN34S_AB	IN56S_AB	IN34D_A	IN56D_B	-	-	-	0x00	115			
0x0A	ANALOG MIC LOOP	W	IN12_M1HPL	IN12_M1SPKL	IN12_M1EAR	IN12_M1LOUTL	IN34_M2HPR	IN34_M2SPKR	IN34_M2EAR	IN34_M2LOUTR	0x00	116			
0x0B	ANALOG LINE LOOP	W	IN12S_ABHP	IN34D_AS PKL	IN34D_AEAR	IN12S_ABLOUT	IN34S_ABHP	IN56D_BSPKR	IN56D_BEAR	IN34S_ABLOUT	0x00	116			
RESERVED REGISTERS															
0x0C	RESERVED	-									0x00	-			
ANALOG INPUT CONFIGURATION REGISTERS															
0x0D	INPUT CONFIG.	R/W	IN34DIFF	IN56DIFF	IN1SEEN	IN2SEEN	IN3SEEN	IN4SEEN	IN5SEEN	IN6SEEN	0x00	78			
0x0E	LINE INPUT LEVEL	R/W	MIXG135	MIXG246	LINAPGA[2:0]			LINBPGA[2:0]			0x1B	78			
0x0F	LINE CONFIG.	R/W	EXTBUFA	EXTBUFB	-	-	-	-	EXTMIC[1:0]		0x00	78			
0x10	MIC1 INPUT LEVEL	R/W	-	PA1EN[1:0]	PGAM1[4:0]						0x11	74			
0x11	MIC2 INPUT LEVEL	R/W	-	PA2EN[1:0]	PGAM2[4:0]						0x11	74			
MICROPHONE CONFIGURATION REGISTERS															
0x12	MIC BIAS VOLTAGE	R/W	-	-	-	-	-	-	MBVSEL[1:0]		0x00	75			
0x13	DIGITAL MIC CONFIG.	R/W	-	MICCLK[2:0]			-	-	DIGMICR	DIGMICL	0x00	76			
0x14	DIGITAL MIC MODE	R/W	DMIC_COMP[3:0]				-	-	DMIC_FREQ[1:0]		0x00	76			
ADC PATH AND CONFIGURATION REGISTERS															
0x15	LEFT ADC MIXER	R/W	MIXADL[7:0]								0x00	80			
0x16	RIGHT ADC MIXER	R/W	MIXADR[7:0]								0x00	80			
0x17	LEFT ADC LEVEL	R/W	-	AVLG[2:0]			AVL[3:0]				0x03	81			
0x18	RIGHT ADC LEVEL	R/W	-	AVRG[2:0]			AVR[3:0]				0x03	81			
0x19	ADC BIQUAD LEVEL	R/W	-	-	-	-	AVBQ[3:0]				0x00	83			
0x1A	ADC SIDETONE	R/W	DSTS[1:0]		-	DVST[4:0]					0x00	82			

REGISTER DESCRIPTION			REGISTER CONTENTS								POR STATE	DS PAGE										
ADDR	NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0												
CLOCK CONFIGURATION REGISTERS																						
0x1B	SYSTEM CLOCK	R/W	-	-	PSCLK[1:0]		-	-	-	-	0x00	88										
0x1C	CLOCK MODE	R/W	FREQ1[3:0]				-	-	-	USE_M1	0x00	88										
0x1D	ANY CLOCK 1	R/W	-	NI1[14:8]								0x00	89									
0x1E	ANY CLOCK 2	R/W	NI1[7:0]								0x00	89										
0x1F	ANY CLOCK 3	R/W	MI1[15:8]								0x00	90										
0x20	ANY CLOCK 4	R/W	MI1[7:0]								0x00	90										
0x21	MASTER MODE	R/W	MAS	-	-	-	-	-	BSEL[2:1]		0x00	86										
INTERFACE CONTROL REGISTERS																						
0x22	INTERFACE FORMAT	R/W	-	-	RJ	WCI	BCI	DLY	WS[1:0]		0x00	87										
0x23	TDM FORMAT 1	R/W	-	-	-	-	-	-	FSW	TDM	0x00	91										
0x24	TDM FORMAT 2	R/W	SLOTL[1:0]		SLOTR[1:0]		SLOTDLY[3:0]					0x00	91									
0x25	I/O CONFIGURATION	R/W	-	-	LTEN	LBEN	DMONO	HIZOFF	SDOEN	SDIEN	0x00	84										
0x26	FILTER CONFIG.	R/W	MODE	AHPF	DHPF	DHF	-	-	-	-	0x80	85										
0x27	DAI PLAYBACK LEVEL	R/W	DV1M	-	DV1G[1:0]		DV1[3:0]					0x00	92									
0x28	EQ PLAYBACK LEVEL	R/W	-	-	-	/EQCLP\	DVEQ[3:0]					0x00	94									
HEADPHONE (HP) CONTROL REGISTERS																						
0x29	LEFT HP MIXER	R/W	-	-	MIXHPL[5:0]						0x00	102										
0x2A	RIGHT HP MIXER	R/W	-	-	MIXHPR[5:0]						0x00	102										
0x2B	HP CONTROL	R/W	-	-	MIXHPRSEL	MIXHPLSEL	MIXHPRG[1:0]	MIXHPLG[1:0]				0x00	103									
0x2C	LEFT HP VOLUME	R/W	HPLM	-	-	HPVOLL[4:0]						0x1A	103									
0x2D	RIGHT HP VOLUME	R/W	HPRM	-	-	HPVOLR[4:0]						0x1A	104									
SPEAKER (SPK) CONFIGURATION REGISTERS																						
0x2E	LEFT SPK MIXER	R/W	-	-	MIXSPL[5:0]						0x00	100										
0x2F	RIGHT SPK MIXER	R/W	-	SPK_SLAVE	MIXSPR[5:0]						0x00	100										
0x30	SPK CONTROL	R/W	-	-	-	MIXSPRG[1:0]	MIXSPLG[1:0]					0x00	101									
0x31	LEFT SPK VOLUME	R/W	SPLM	-	SPVOLL[5:0]						0x2C	101										
0x32	RIGHT SPK VOLUME	R/W	SPRM	-	SPVOLR[5:0]						0x2C	101										
AUTOMATIC LEVEL CONTROL (ALC) CONFIGURATION REGISTERS																						
0x33	ALC TIMING	R/W	ALCEN	ALCRLS[2:0]			-	ALCATK[2:0]				0x00	92									
0x34	ALC COMPRESSOR	R/W	ALCCMP[2:0]				ALCTHC[4:0]					0x00	93									
0x35	ALC EXPANDER	R/W	ALCEXP[2:0]				ALCTHE[4:0]					0x00	93									
0x36	ALC GAIN	R/W	-	-	-	ALCG[4:0]						0x00	93									
RECEIVER (RCV) OR EARPiece) AND LINE OUTPUT (LOUT) REGISTERS																						
0x37	RCV/LOUTL MIXER	R/W	-	-	MIXRCVL[5:0]						0x00	97, 106										
0x38	RCV/LOUTL CONTROL	R/W	-	-	-	-	-	-	MIXRCVLG[1:0]		0x00	97, 106										
0x39	RCV/LOUTL VOLUME	R/W	RCVLM	-	-	RCVLVOL[4:0]						0x15	98, 107									
0x3A	LOUTR MIXER	R/W	LINMOD	-	MIXRCVR[5:0]						0x00	107										
0x3B	LOUTR CONTROL	R/W	-	-	-	-	-	-	MIXRCVRG[1:0]		0x00	107										
0x3C	LOUTR VOLUME	R/W	RCVRM	-	-	RCVRVOL[4:0]						0x15	108									

REGISTER DESCRIPTION			REGISTER CONTENTS									POR STATE	DS PAGE
ADDR	NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0			
JACK DETECT AND ENABLE REGISTERS													
0x3D	JACK DETECT	R/W	JDETEN	JDWK	-	-	-	-	-	JDEB[1:0]	0x00	111	
0x3E	INPUT ENABLE	R/W	-	-	-	MBEN	LINEAEN	LINEBEN	ADREN	ADLEN	0x00	71	
0x3F	OUTPUT ENABLE	R/W	HPREN	HPLEN	SPREN	SPLEN	RCVLEN	RCVREN	DAREN	DALEN	0x00	71	
0x40	LEVEL CONTROL	R/W	-	-	-	-	-	/ZDEN\	/VS2EN\	/VSEN\	0x00	109	
0x41	DSP FILTER ENABLE	R/W	-	-	-	-	ADCBQEN	EQ3BANDEN	EQ5BANDEN	EQ7BANDEN	0x00	94	
BIAS AND POWER MODE CONFIGURATION REGISTERS													
0x42	BIAS CONTROL	R/W	-	-	-	-	-	-	-	VCM_MODE	0x00	69	
0x43	DAC CONTROL	R/W	-	-	-	-	-	-	-	PERFMODE	DACHP	0x00	69
0x44	ADC CONTROL	R/W	-	-	-	-	-	OSR128	ADCDITHER	ADCHP	0x06	70	
0x45	DEVICE SHUTDOWN	R/W	/SHDN\	-	-	-	-	-	-	-	0x00	70	
DAI PARAMETRIC EQUALIZER BAND 1: BIQUAD FILTER COEFFICIENT REGISTERS													
0x46	EQUALIZER BAND 1 COEFFICIENT B0	R/W	B0_1[23:16]									0x00	95
0x47		R/W	B0_1[15:8]									0x00	
0x48		R/W	B0_1[7:0]									0x00	
0x49	EQUALIZER BAND 1 COEFFICIENT B1	R/W	B1_1[23:16]									0x00	
0x4A		R/W	B1_1[15:8]									0x00	
0x4B		R/W	B1_1[7:0]									0x00	
0x4C	EQUALIZER BAND 1 COEFFICIENT B2	R/W	B2_1[23:16]									0x00	
0x4D		R/W	B2_1[15:8]									0x00	
0x4E		R/W	B2_1[7:0]									0x00	
0x4F	EQUALIZER BAND 1 COEFFICIENT A1	R/W	A1_1[23:16]									0x00	
0x50		R/W	A1_1[15:8]									0x00	
0x51		R/W	A1_1[7:0]									0x00	
0x52	EQUALIZER BAND 1 COEFFICIENT A2	R/W	A2_1[23:16]									0x00	
0x53		R/W	A2_1[15:8]									0x00	
0x54		R/W	A2_1[7:0]									0x00	
DAI PARAMETRIC EQUALIZER BAND 2: BIQUAD FILTER COEFFICIENT REGISTERS													
0x55	EQUALIZER BAND 2 COEFFICIENT B0	R/W	B0_2[23:16]									0x00	95
0x56		R/W	B0_2[15:8]									0x00	
0x57		R/W	B0_2[7:0]									0x00	
0x58	EQUALIZER BAND 2 COEFFICIENT B1	R/W	B1_2[23:16]									0x00	
0x59		R/W	B1_2[15:8]									0x00	
0x5A		R/W	B1_2[7:0]									0x00	
0x5B	EQUALIZER BAND 2 COEFFICIENT B2	R/W	B2_2[23:16]									0x00	
0x5C		R/W	B2_2[15:8]									0x00	
0x5D		R/W	B2_2[7:0]									0x00	
0x5E	EQUALIZER BAND 2 COEFFICIENT A1	R/W	A1_2[23:16]									0x00	
0x5F		R/W	A1_2[15:8]									0x00	
0x60		R/W	A1_2[7:0]									0x00	
0x61	EQUALIZER BAND 2 COEFFICIENT A2	R/W	A2_2[23:16]									0x00	
0x62		R/W	A2_2[15:8]									0x00	
0x63		R/W	A2_2[7:0]									0x00	

REGISTER DESCRIPTION			REGISTER CONTENTS								POR STATE	DS PAGE
ADDR	NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0		
DAI PARAMETRIC EQUALIZER BAND 3: BIQUAD FILTER COEFFICIENT REGISTERS												
0x64	EQUALIZER BAND 3 COEFFICIENT B0	R/W	B0_3[23:16]								0x00	95
0x65		R/W	B0_3[15:8]								0x00	
0x66		R/W	B0_3[7:0]								0x00	
0x67	EQUALIZER BAND 3 COEFFICIENT B1	R/W	B1_3[23:16]								0x00	
0x68		R/W	B1_3[15:8]								0x00	
0x69		R/W	B1_3[7:0]								0x00	
0x6A	EQUALIZER BAND 3 COEFFICIENT B2	R/W	B2_3[23:16]								0x00	
0x6B		R/W	B2_3[15:8]								0x00	
0x6C		R/W	B2_3[7:0]								0x00	
0x6D	EQUALIZER BAND 3 COEFFICIENT A1	R/W	A1_3[23:16]								0x00	95
0x6E		R/W	A1_3[15:8]								0x00	
0x6F		R/W	A1_3[7:0]								0x00	
0x70	EQUALIZER BAND 3 COEFFICIENT A2	R/W	A2_3[23:16]								0x00	
0x71		R/W	A2_3[15:8]								0x00	
0x72		R/W	A2_3[7:0]								0x00	
DAI PARAMETRIC EQUALIZER BAND 4: BIQUAD FILTER COEFFICIENT REGISTERS												
0x73	EQUALIZER BAND 4 COEFFICIENT B0	R/W	B0_4[23:16]								0x00	95
0x74		R/W	B0_4[15:8]								0x00	
0x75		R/W	B0_4[7:0]								0x00	
0x76	EQUALIZER BAND 4 COEFFICIENT B1	R/W	B1_4[23:16]								0x00	
0x77		R/W	B1_4[15:8]								0x00	
0x78		R/W	B1_4[7:0]								0x00	
0x79	EQUALIZER BAND 4 COEFFICIENT B2	R/W	B2_4[23:16]								0x00	
0x7A		R/W	B2_4[15:8]								0x00	
0x7B		R/W	B2_4[7:0]								0x00	
0x7C	EQUALIZER BAND 4 COEFFICIENT A1	R/W	A1_4[23:16]								0x00	
0x7D		R/W	A1_4[15:8]								0x00	
0x7E		R/W	A1_4[7:0]								0x00	
0x7F	EQUALIZER BAND 4 COEFFICIENT A2	R/W	A2_4[23:16]								0x00	
0x80		R/W	A2_4[15:8]								0x00	
0x81		R/W	A2_4[7:0]								0x00	

REGISTER DESCRIPTION			REGISTER CONTENTS								POR STATE	DS PAGE
ADDR	NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0		
DAI PARAMETRIC EQUALIZER BAND 5: BIQUAD FILTER COEFFICIENT REGISTERS												
0x82	EQUALIZER BAND 5 COEFFICIENT B0	R/W	B0_5[23:16]								0x00	95
0x83		R/W	B0_5[15:8]								0x00	
0x84		R/W	B0_5[7:0]								0x00	
0x85	EQUALIZER BAND 5 COEFFICIENT B1	R/W	B1_5[23:16]								0x00	
0x86		R/W	B1_5[15:8]								0x00	
0x87		R/W	B1_5[7:0]								0x00	
0x88	EQUALIZER BAND 5 COEFFICIENT B2	R/W	B2_5[23:16]								0x00	
0x89		R/W	B2_5[15:8]								0x00	
0x8A		R/W	B2_5[7:0]								0x00	
0x8B	EQUALIZER BAND 5 COEFFICIENT A1	R/W	A1_5[23:16]								0x00	
0x8C		R/W	A1_5[15:8]								0x00	
0x8D		R/W	A1_5[7:0]								0x00	
0x8E	EQUALIZER BAND 5 COEFFICIENT A2	R/W	A2_5[23:16]								0x00	
0x8F		R/W	A2_5[15:8]								0x00	
0x90		R/W	A2_5[7:0]								0x00	
DAI PARAMETRIC EQUALIZER BAND 6: BIQUAD FILTER COEFFICIENT REGISTERS												
0x91	EQUALIZER BAND 6 COEFFICIENT B0	R/W	B0_6[23:16]								0x00	95
0x92		R/W	B0_6[15:8]								0x00	
0x93		R/W	B0_6[7:0]								0x00	
0x94	EQUALIZER BAND 6 COEFFICIENT B1	R/W	B1_6[23:16]								0x00	
0x95		R/W	B1_6[15:8]								0x00	
0x96		R/W	B1_6[7:0]								0x00	
0x97	EQUALIZER BAND 6 COEFFICIENT B2	R/W	B2_6[23:16]								0x00	
0x98		R/W	B2_6[15:8]								0x00	
0x99		R/W	B2_6[7:0]								0x00	
0x9A	EQUALIZER BAND 6 COEFFICIENT A1	R/W	A1_6[23:16]								0x00	
0x9B		R/W	A1_6[15:8]								0x00	
0x9C		R/W	A1_6[7:0]								0x00	
0x9D	EQUALIZER BAND 6 COEFFICIENT A2	R/W	A2_6[23:16]								0x00	
0x9E		R/W	A2_6[15:8]								0x00	
0x9F		R/W	A2_6[7:0]								0x00	

REGISTER DESCRIPTION			REGISTER CONTENTS								POR STATE	DS PAGE
ADDR	NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0		
DAI PARAMETRIC EQUALIZER BAND 7: BIQUAD FILTER COEFFICIENT REGISTERS												
0xA0	EQUALIZER BAND 7 COEFFICIENT B0	R/W	B0_7[23:16]								0x00	95
0xA1		R/W	B0_7[15:8]								0x00	
0xA2		R/W	B0_7[7:0]								0x00	
0xA3	EQUALIZER BAND 7 COEFFICIENT B1	R/W	B1_7[23:16]								0x00	
0xA4		R/W	B1_7[15:8]								0x00	
0xA5		R/W	B1_7[7:0]								0x00	
0xA6	EQUALIZER BAND 7 COEFFICIENT B2	R/W	B2_7[23:16]								0x00	
0xA7		R/W	B2_7[15:8]								0x00	
0xA8		R/W	B2_7[7:0]								0x00	
0xA9	EQUALIZER BAND 7 COEFFICIENT A1	R/W	A1_7[23:16]								0x00	83
0xAA		R/W	A1_7[15:8]								0x00	
0xAB		R/W	A1_7[7:0]								0x00	
0xAC	EQUALIZER BAND 7 COEFFICIENT A2	R/W	A2_7[23:16]								0x00	
0xAD		R/W	A2_7[15:8]								0x00	
0xAE		R/W	A2_7[7:0]								0x00	
ADC BIQUAD FILTER COEFFICIENT REGISTERS												
0xAF	ADC BIQUAD COEFFICIENT B0	R/W	ADC_B0[23:16]								0x00	83
0xB0		R/W	ADC_B0[15:8]								0x00	
0xB1		R/W	ADC_B0[7:0]								0x00	
0xB2	ADC BIQUAD COEFFICIENT B1	R/W	ADC_B1[23:16]								0x00	
0xB3		R/W	ADC_B1[15:8]								0x00	
0xB4		R/W	ADC_B1[7:0]								0x00	
0xB5	ADC BIQUAD COEFFICIENT B2	R/W	ADC_B2[23:16]								0x00	
0xB6		R/W	ADC_B2[15:8]								0x00	
0xB7		R/W	ADC_B2[7:0]								0x00	
0xB8	ADC BIQUAD COEFFICIENT A1	R/W	ADC_A1[23:16]								0x00	
0xB9		R/W	ADC_A1[15:8]								0x00	
0xBA		R/W	ADC_A1[7:0]								0x00	
0xBB	ADC BIQUAD COEFFICIENT A2	R/W	ADC_A2[23:16]								0x00	
0xBC		R/W	ADC_A2[15:8]								0x00	
0xBD		R/W	ADC_A2[7:0]								0x00	
REVISION ID REGISTER												
0xFF	REVISION ID	R	REVID[7:0]								0x42	117

Power and Performance Management

The device includes comprehensive power management to allow the disabling of unused blocks to minimize supply current. In addition to this, the available power modes provide a software configurable choice between optimized performance and reduced power consumption.

Device Performance Configuration

The Common Mode Bias Register (Table 2) selects the method used to derive the common mode reference voltage. A common mode bias created by resistive division (from the AVDD supply) facilitates lower overall power consumption (disables the bandgap reference circuit). However, this type of VCM reference has the disadvantage of scaling with the AVDD supply voltage (and thus also has reduced PSRR). When derived from a bandgap reference, VCM is constant regardless of the supply voltage but the additional circuitry does increase power consumption.

The ADC, DAC, and headphone playback all have optional high performance modes (Table 3 / Table 4). In each case, these modes trade additional power consumption for enhanced performance. The ADC also has optional dither (recommended for the cleanest spectrum), and can be configured to two different oversampling rates (see section **TBD** for additional details on ADC operation)

Table 2: Common Mode Bias Register

ADDRESS: 0x42				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	-	-	-	-
1	-	-	-	-
0	VCM_MODE	R/W	0	Select source for VCM. 0 : VCM derived from resistive division selected (default) 1 : VCM created by bandgap reference selected

Table 3: Output Power and Performance Mode Register

ADDRESS: 0x43				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	-	-	-	-
1	PERFMODE	R/W	0	Performance Mode Selects DAC to headphone playback performance mode. 1 : Low power playback mode. 0 : High performance playback mode.
0	DACHP	R/W	0	DAC High Performance Mode 0 : DAC settings optimized for lowest power consumption 1 : DAC settings optimized for best performance

Table 4: Input Power and Performance Mode Register

ADDRESS: 0x45				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	OSR128	R/W	0	ADC Oversampling Rate 0 : ADCCLK = 64*fs 1 : ADCCLK = 128*fs (default)
1	ADCDITHER	R/W	0	ADC Quantizer Dither 0 : Dither disabled 1 : Dither enabled
0	ADCHP	R/W	0	ADC High Performance Mode 0 : ADC is optimized for low power operation 1 : ADC is optimized for best performance

Device Enable Configuration

In addition to a device global shutdown control, the major input and output blocks can be independently enabled (or disabled) to optimize power consumption. The device global shutdown control is detailed in Table 5. Table 6 details the available input signal path enables (with the exception of the analog microphone inputs 1/2, which are enabled from registers 0x10 and 0x11, or Table 8 and Table 9 respectively). Table 7 details the available output signal path enables.

When the device is in global shutdown, the major input and output blocks are all disabled to conserve power. However, the I²C interface remains active and all device registers can be configured. Certain registers should only be programmed while in shutdown (detailed in Table 79). Changing these registers when the device is active could result in unexpected behavior. For optimal, minimized power consumption, only enable the stage blocks that are part of the intended signal path configuration.

Table 5: Device Global Shutdown Register

ADDRESS: 0x45				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	-	-	-	-
1	-	-	-	-
0	/SHDN	R/W	0	Device Active-low Global Shutdown Control 0 : Device is in shutdown. 1 : Device is active. Certain registers should not be written to while the device is active () .

Table 6: Input Enable Register

ADDRESS: 0x3E				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	MBEN	R/W	0	Microphone Bias Enable 0 : Disable Microphone Bias 1 : Enable Microphone Bias
3	LINEAEN	R/W	0	Enables Line A Analog Input Block 0 : Line A Input amplifier disabled 1 : Line A Input amplifier enabled
2	LINEBEN	R/W	0	Enables Line B Analog Input Block 0 : Line B Input amplifier disabled 1 : Line B Input amplifier enabled
1	ADREN	R/W	0	Right ADC Enable 0 : Right ADC disabled 1 : Right ADC enabled
0	ADLEN	R/W	0	Left ADC Enable 0 : Left ADC disabled 1 : Left ADC enabled

Table 7: Output Enable Register

ADDRESS: 0x3F				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	HPREN	R/W	0	Right Headphone Output Enable 0 : Disable Right Headphone Output 1 : Enable Right Headphone Output
6	HPLEN	R/W	0	Left Headphone Output Enable 0 : Disable Left Headphone Output 1 : Enable Left Headphone Output
5	SPREN	R/W	0	Right Class-D Speaker Output Enable 0 : Disable Right Speaker Output 1 : Enable Right Speaker Output
4	SPLEN	R/W	0	Left Class-D Speaker Output Enable 0 : Disable Left Speaker Output 1 : Enable Left Speaker Output
3	RCVLEN	R/W	0	Receiver (Earpiece) / Line Out Left Output Enable 0 : Disable Receiver / Left Line Output 1 : Enable Receiver / Left Line Output
2	RCVREN	R/W	0	Right Line Output Enable 0 : Disable Right Line Output 1 : Enable Right Line Output
1	DAREN	R/W	0	Right DAC Digital Input Enable 0 : Disable Right DAC Input 1 : Enable Right DAC Input
0	DALEN	R/W	0	Left DAC Digital Input Enable 0 : Disable Left DAC Input 1 : Enable Left DAC Input

Analog Audio Input Configuration

The device features either six (WLP package) or four (TQFN package) flexible analog inputs. Each pair can be configured as either an analog microphone input, a single ended or differential line input(s), or as a reduced power, full-scale differential analog input direct to the ADC mixer. The analog microphone and line inputs can either be routed to the stereo ADC mixer for recording or directly to any analog output mixer for playback.

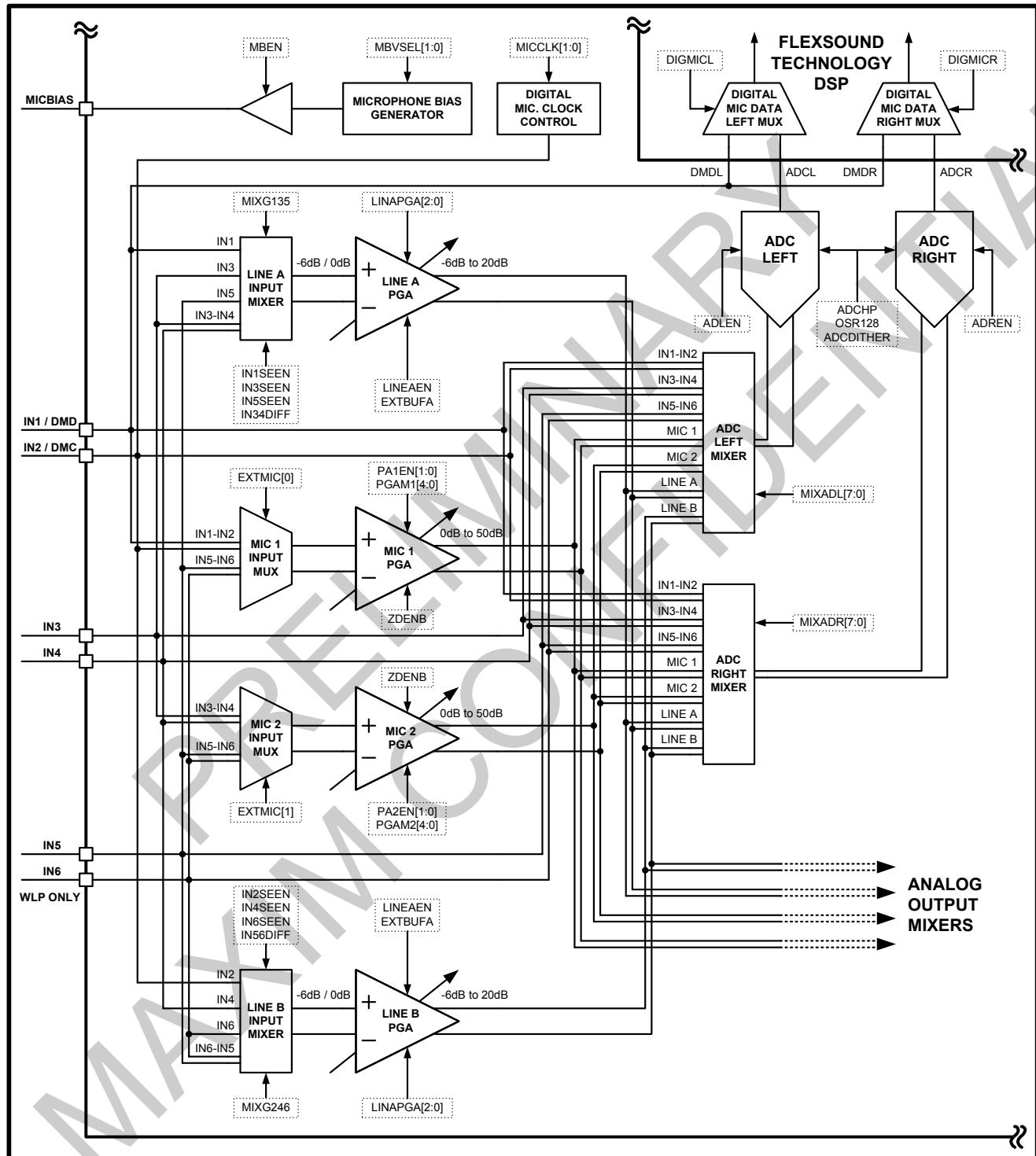


Figure 6: Analog Audio Input Functional Diagram

Analog Microphone Inputs

The device includes three differential microphone inputs (three for the WLP package and two for the TQFN package) and a programmable, low-noise microphone bias for powering a wide variety of external microphones (Figure 7). By default, analog inputs IN1 and IN2 differentially (IN1 – IN2) provide the input to microphone amplifier 1, while IN3 and IN4 differentially (IN3 – IN4) form the input to microphone amplifier 2. For the WLP package, the additional analog input pair IN5 and IN6 can be configured as a differential input (IN5 – IN6) to either microphone amplifier 1 or 2 (Table 15).

In the typical application, one microphone input is used for the handset microphone and the other is used as an accessory microphone (IN1/IN2 and IN3/IN4). In systems using a background noise microphone, IN5/IN6 (WLP only) can be retasked as another microphone input.

Analog microphone input signals are amplified by two stages of programmable gain amplifiers, and then routed to either the ADC mixer (record) or analog outputs (playback). The first, a coarse gain stage, includes the analog microphone enable, and offers selectable 0dB, 20dB, or 30dB gain settings. The second, a fine gain stage, is a programmable-gain amplifier (PGA) adjustable from 0dB to 20dB in 1dB steps (Table 8 and Table 9). Together, the two stages provide up to 50dB of signal gain for the analog microphone inputs. To maximize the signal-to-noise ratio, use the coarse gain settings of the first stage whenever possible. Zero-crossing detection is included on the PGA to minimize zipper noise while making gain changes.

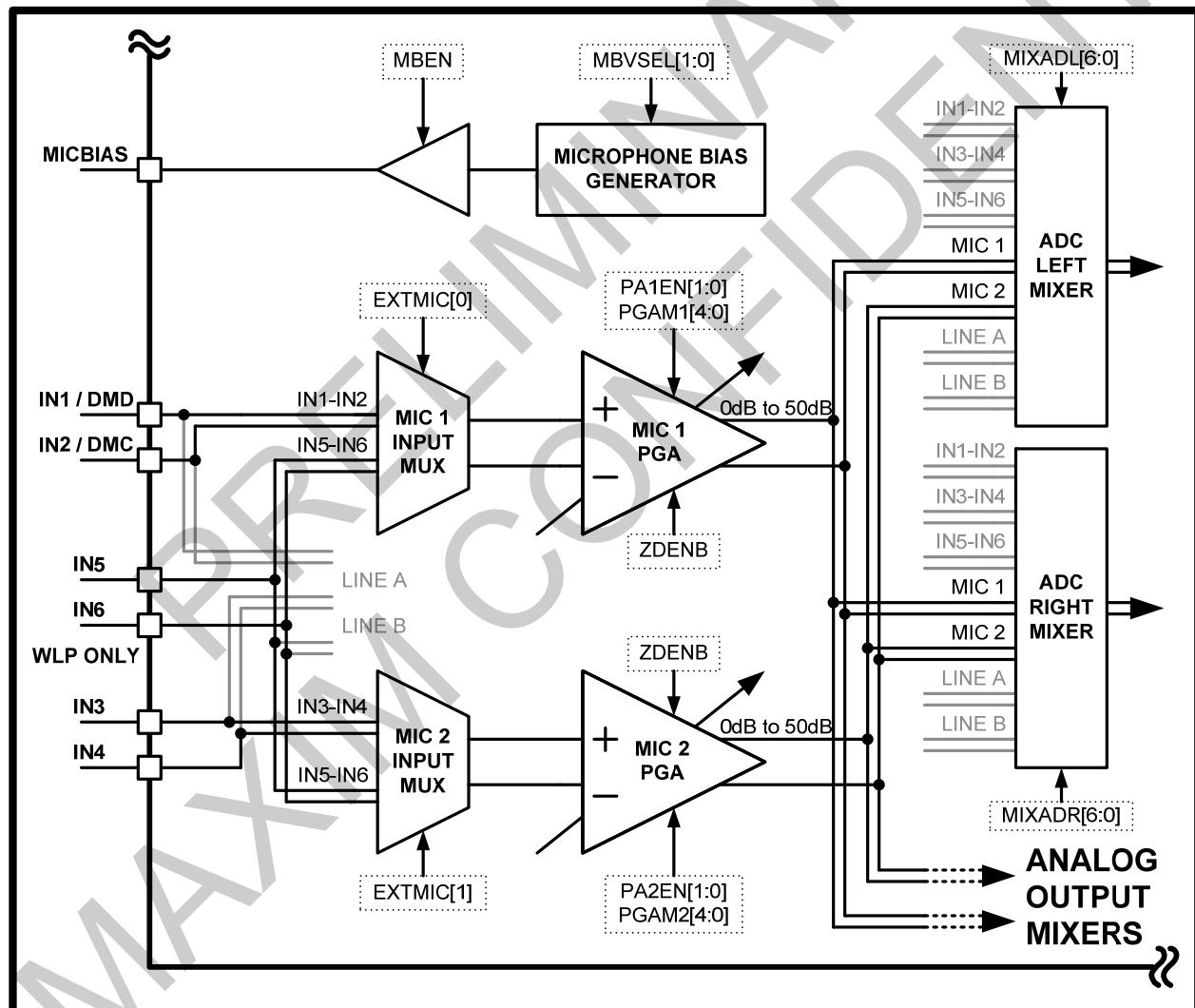


Figure 7: Analog Microphone Input Functional Diagram

Table 8: Microphone 1 Enable and Level Configuration Register

ADDRESS: 0x10				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	PA1EN[1:0]	R/W	0	Microphone 1 Input Amplifier Enable and Coarse Gain Setting 00 : Disabled 10 : 20dB 01 : 0dB 11 : 30dB
5			0	
4	PGAM1[4:0]	R/W	1	Microphone 1 Programmable Gain Amplifier Fine Adjust Configuration
3			0	0x1F : 0dB 0xE : 6dB 0x06 : 14dB : 0xD : 7dB 0x05 : 15dB
2			0	0x14 : 0dB 0xC : 8dB 0x04 : 16dB 0x13 : 1dB 0xB : 9dB 0x03 : 17dB
1			0	0x12 : 2dB 0xA : 10dB 0x02 : 18dB 0x11 : 3dB 0x9 : 11dB 0x01 : 19dB
0			1	0x10 : 4dB 0x8 : 12dB 0x00 : 20dB 0x0F : 5dB 0x7 : 13dB

Table 9: Microphone 2 Enable and Level Configuration Register

ADDRESS: 0x11				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	PA2EN[1:0]	R/W	0	Microphone 2 Input Amplifier Enable and Coarse Gain Setting 00 : Disabled 10 : 20dB 01 : 0dB 11 : 30dB
5			0	
4	PGAM2[4:0]	R/W	1	Microphone 2 Programmable Gain Amplifier Fine Adjust Configuration
3			0	0x1F : 0dB 0xE : 6dB 0x06 : 14dB : 0xD : 7dB 0x05 : 15dB
2			0	0x14 : 0dB 0xC : 8dB 0x04 : 16dB 0x13 : 1dB 0xB : 9dB 0x03 : 17dB
1			0	0x12 : 2dB 0xA : 10dB 0x02 : 18dB 0x11 : 3dB 0x9 : 11dB 0x01 : 19dB
0			1	0x10 : 4dB 0x8 : 12dB 0x00 : 20dB 0x0F : 5dB 0x7 : 13dB

Analog Microphone Bias

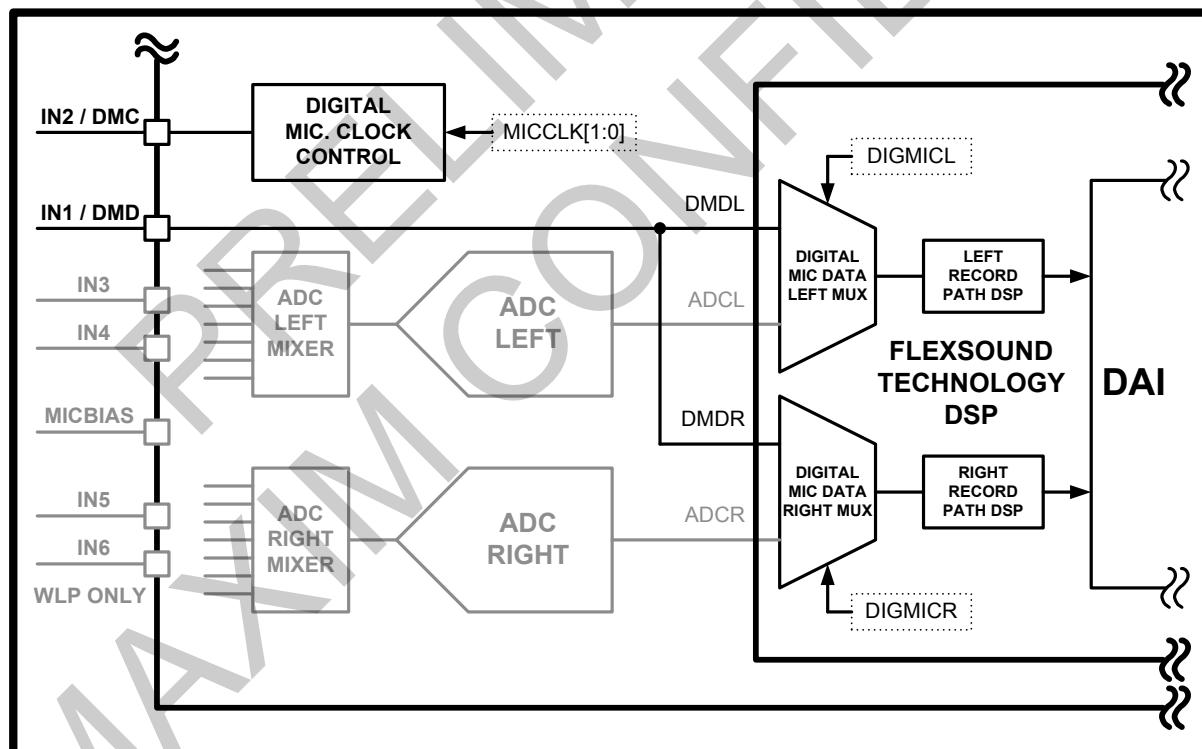
The device features a low noise microphone bias output (MICBIAS) that can be configured to power a wide range of external microphone devices. The microphone bias can be set by the software to any one of 4 voltages (2.2V, 2.4V, 2.55V, or 2.8V) by programming the Microphone Bias Level Configuration Register (Table 10).

Table 10: Microphone Bias Level Configuration Register

ADDRESS: 0x12				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	-	-	-	-
1	MBVSEL[1:0]	R/W	0	Microphone Bias Level Configuration
0			0	00 : 2.2V 10 : 2.55V 01 : 2.4V 11 : 2.8V

Digital Microphone Inputs

One microphone input, IN1/IN2, can also be configured as a digital microphone input accepting signals from two different digital microphones (Figure 8). Any two microphones, either analog or digital, can be recorded from simultaneously. Digital microphone left and right are routed through the left and right record path DSP to the DAI. The appropriate channel record path DSP is automatically switched to either of the digital microphones when they are enabled (DIGIMICR and DIGIMICL, **Error! Reference source not found.**).

**Figure 8: Digital Microphone Input Functional Diagram**

To avoid any potential clipping and minimize potential distortion, always enable the record path DC blocking filters to remove any DC offsets (AHPF, Table 25). The record path biquad filter, and digital gain and level control can also optionally be applied to digital microphone inputs.

The digital microphone clock rate can be configured to any one of 4 settings using MICCLK[1:0] (**Error! Reference source not found.**). The digital microphone clock can be derived either from a PCLK divider or a sample rater multiplier. If MICCLK is set to 1x and PCLK is not an integer multiple of the sample rate then the generated clock will potentially be jittered.

Table 11: Digital Microphone 1

ADDRESS: 0x13				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	MICCLK[2:0]	R/W	0	Digital Microphone Clock Rate Configuration 000 : $f_{DIGMICCLK} = PCLK / 2$ 100 : $f_{DIGMICCLK} = PCLK / 6$ 001 : $f_{DIGMICCLK} = PCLK / 3$ 101 : $f_{DIGMICCLK} = PCLK / 8$ 010 : $f_{DIGMICCLK} = PCLK / 4$ 110 : $f_{DIGMICCLK} = PCLK / 10$ 011 : $f_{DIGMICCLK} = PCLK / 5$ 111 : RESERVED
5			0	
4			0	
3	-	-	-	-
2	-	-	-	-
1	DIGMICR	R/W	0	Digital Microphone Right Channel Enable 0 : Right record channel uses on-chip ADC 1 : Right record channel uses digital microphone input
0	DIGMICL	R/W	0	Digital Microphone Left Channel Enable 0 : Left record channel uses on-chip ADC 1 : Left record channel uses digital microphone input

Table 12: Digital Microphone 2

ADDRESS: 0x14				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	DMIC_COMP[3:0]	R/W	0	Digital Microphone Compensation Filter Configuration 0000 - 1111 : TBD If the system clock and sample rate bits in register 0x04 / 0x05 are set, then the compensation filter configuration is automatically decoded.
6			0	
5			0	
4			0	
3	-	-	-	-
2	-	-	-	-
1	DMIC_FREQ[1:0]	R/W	0	Digital Microphone Frequency Range Configuration 00 : $f_{DIGMICCLK} < 3.5MHz$ 10 : $4.5MHz \leq f_{DIGMICCLK}$ 01 : $3.5MHz \leq f_{DIGMICCLK} < 4.5MHz$ 11 : Reserved If any of the system clock bits in register 0x04 are set, then the frequency range configuration is automatically decoded.
0			0	

Analog Line Inputs

The device includes two sets of line inputs (Figure 9). The line inputs can be configured as stereo single-ended inputs, stereo differential inputs, or multiple mixed single ended inputs. To allow the line inputs to match a wide range of input signal levels, each line input includes a coarse programmable gain amplifier (PGA) that can provide up to 6dB of attenuation or 20dB of signal gain. After the PGAs, the line inputs are then routed to either the ADC mixer (record) or analog outputs (playback).

If the line input requires a custom gain level, the external gain mode provides a trimmed feedback resistor. The line input gain is then set by using the following formula to calculate the appropriate series input resistor:

$$AV_{PGAIN} = 20 \times \log (20k\Omega/R_{IN})$$

In addition to custom gain levels, the external gain mode allows the line input PGAs to be reconfigured into a variety of different amplifier topologies. It allows for the summing of multiple signals into a single input by connecting multiple input resistors in a summing topology as shown in Figure TBD. It also allows the line inputs to accept analog input signals larger than 1V_{RMS} by creating a voltage divider and adjusting the ratio of the series input resistor to the internal feedback resistor to less than 1 ($20k\Omega/R_{IN} < 1$).

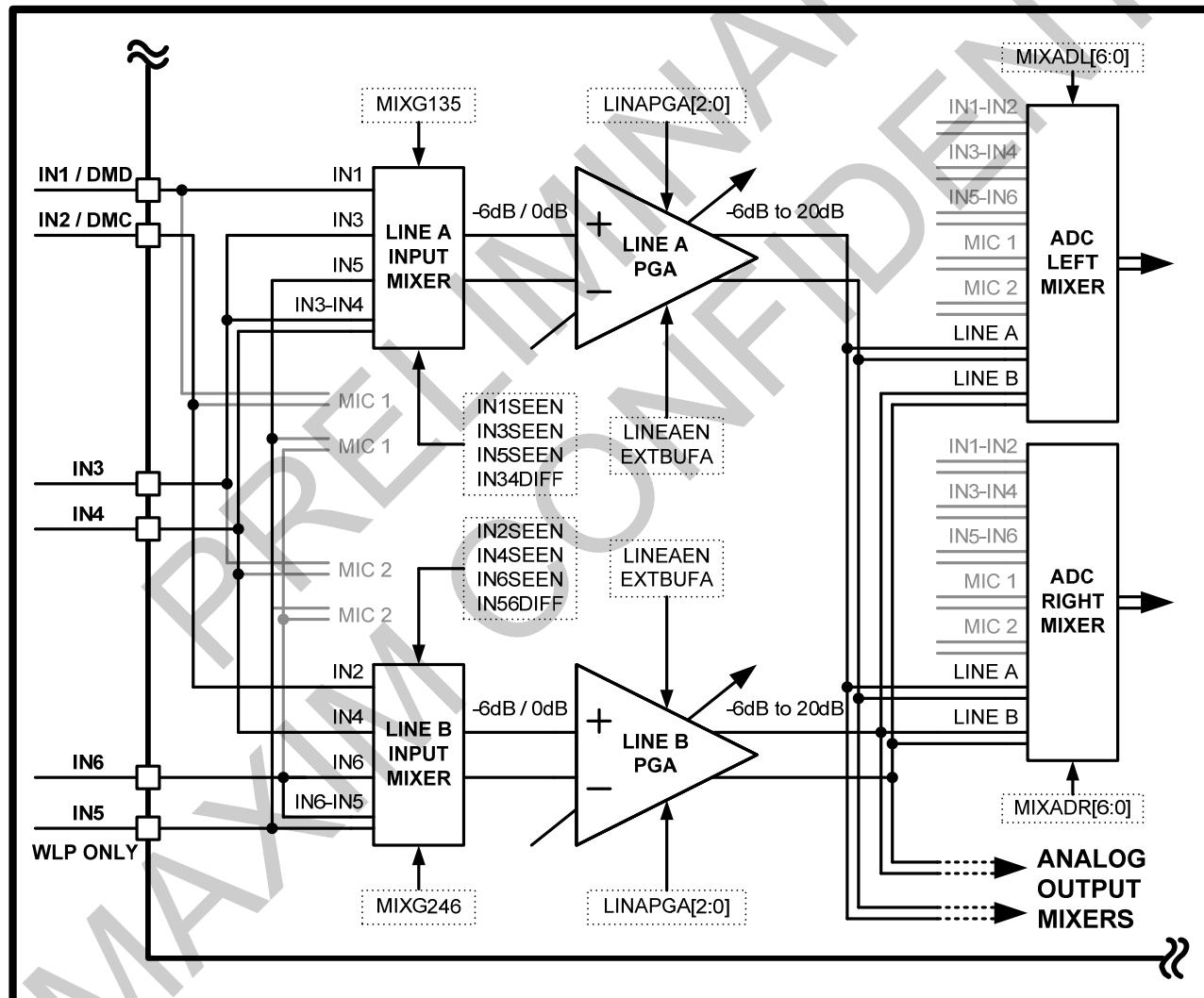


Figure 9: Analog Line Input Functional Diagram

Table 13: Line Input Mixer Configuration Register

ADDRESS: 0x0D				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	IN34DIFF	R/W	0	Selects IN3-IN4 Differentially as an Input to the Line A Mixer
6	IN56DIFF	R/W	0	Selects IN6-IN5 Differentially as an Input to the Line B Mixer (WLP Only)
5	IN1SEEN	R/W	0	Selects IN1 Single Ended as an Input to the Line A Mixer
4	IN2SEEN	R/W	0	Selects IN2 Single Ended as an Input to the Line B Mixer
3	IN3SEEN	R/W	0	Selects IN3 Single Ended as an Input to the Line A Mixer
2	IN4SEEN	R/W	0	Selects IN4 Single Ended as an Input to the Line B Mixer
1	IN5SEEN	R/W	0	Selects IN5 Single Ended as an Input to the Line A Mixer (WLP Only)
0	IN6SEEN	R/W	0	Selects IN6 Single Ended as an Input to the Line B Mixer (WLP Only)

Table 14: Line Input Level Configuration Register

ADDRESS: 0x0E				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	MIXG135	R/W	0	Enable for a -6dB Reduction for Multiple Single Ended Line A Mixer Inputs 0 : Normal Line A Mixer Operation 1 : Gain is Reduced by -6dB when Multiple Single Ended Inputs are selected
6	MIXG246	R/W	0	Enable for a -6dB Reduction for Multiple Single Ended Line B Mixer Inputs 0 : Normal Line B Mixer Operation 1 : Gain is Reduced by -6dB when Multiple Single Ended Inputs are selected
5	LINAPGA[2:0]	R/W	0	Line Input A Programmable Internal Preamp Gain Configuration
4			1	000 : 20dB 010 : 3dB 100 : -3dB
3			1	001 : 14dB 011 : 0dB 101, 110, 111 : -6dB
2	LINBPGA[2:0]	R/W	0	Line Input B Programmable Internal Preamp Gain Configuration
1			1	000 : 20dB 010 : 3dB 100 : -3dB
0			1	001 : 14dB 011 : 0dB 101, 110, 111 : -6dB

Table 15: Line Input Mode and Source Configuration Register

ADDRESS: 0x0F				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	EXTBUFA	R/W	0	Selects External Resistor Gain Mode for Line Input A
6	EXTBUFB	R/W	0	Selects External Resistor Gain Mode for Line Input B
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	-	-	-	-
1	EXTMIC[1:0]	R/W	0	External Microphone (IN6-IN5) Input Control Configuration (WLP Only) 00 : EXT_MIC not selected 10 : EXT_MIC selected on MIC 2
0			0	01 : EXT_MIC selected on MIC 1 11 : EXT_MIC not selected

Analog Full-Scale Direct to ADC Mixer Inputs

The analog inputs can also be configured to accept and route differential analog signals directly to the ADC mixers (record, Figure 10). By disabling and bypassing the analog microphone and line input gain stages, this mode provides a reduced power configuration for full-scale (up to $1V_{RMS}$) analog input signals. Unlike the analog microphone and line input configurations, this mode does not allow the input signals to be routed directly to the analog output mixers (playback).

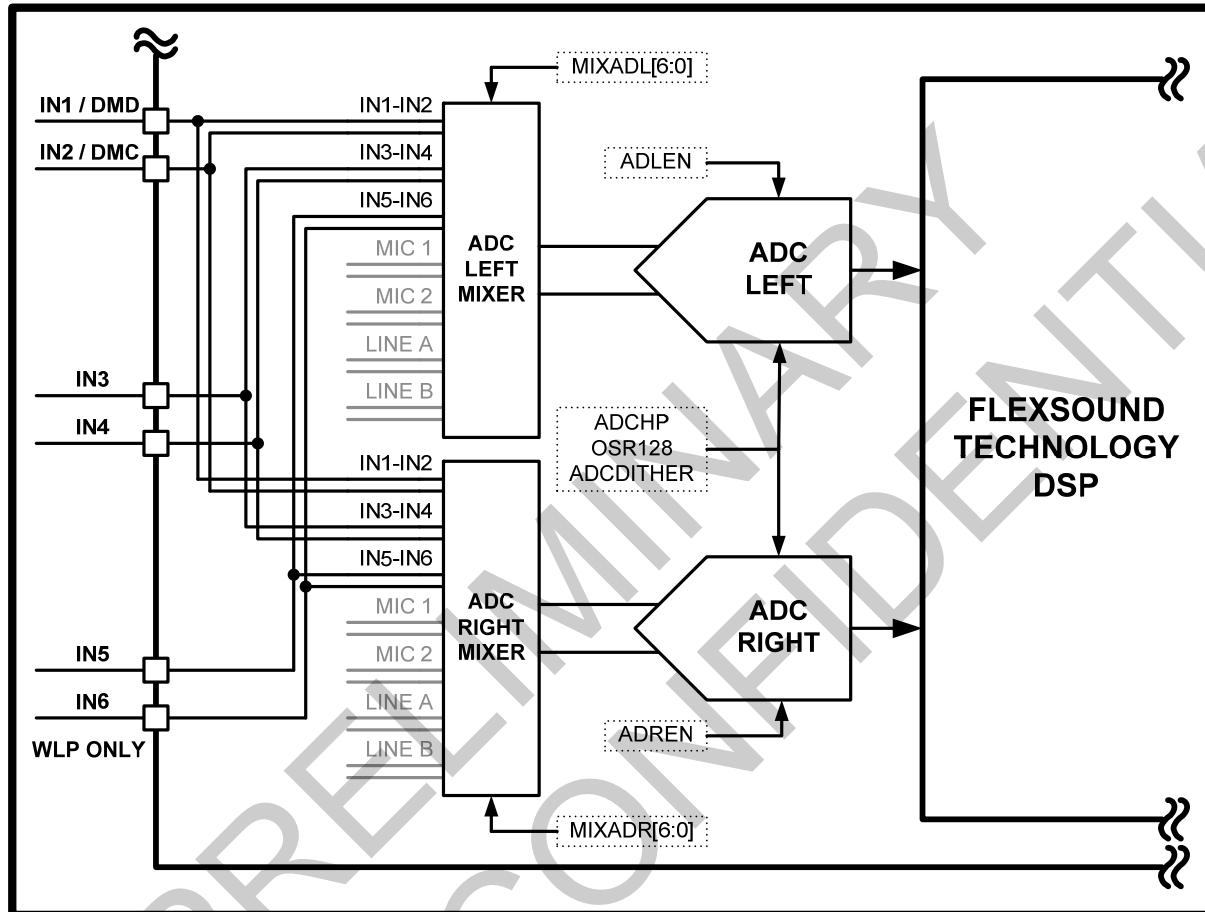


Figure 10: Analog Direct to ADC Mixer Input Functional Diagram

Analog Input to Analog Output Loopback

Analog to Digital Converter (ADC) Configuration
ADC Input Mixer Configuration

Table 16: Left ADC Mixer Input Configuration Register

ADDRESS: 0x15				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	MIXADL[6:0]	R/W	0	Select IN1-IN2 Differential Input Direct to Left ADC Mixer
6		R/W	0	Select IN3-IN4 Differential Input Direct to Left ADC Mixer
5		R/W	0	Select IN6-IN5 Differential Input Direct to Left ADC Mixer (WLP Only)
4		R/W	0	Select Line Input A to Left ADC Mixer
3		R/W	0	Select Line Input B to Left ADC Mixer
2		R/W	0	Select Microphone Input 1 to Left ADC Mixer
1		R/W	0	Select Microphone Input 2 to Left ADC Mixer
0		-	-	-

Table 17: Right ADC Mixer Input Configuration Register

ADDRESS: 0x16				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	MIXADR[6:0]	R/W	0	Select IN1-IN2 Differential Input Direct to Right ADC Mixer
6		R/W	0	Select IN3-IN4 Differential Input Direct to Right ADC Mixer
5		R/W	0	Select IN6-IN5 Differential Input Direct to Right ADC Mixer (WLP Only)
4		R/W	0	Select Line Input A to Right ADC Mixer
3		R/W	0	Select Line Input B to Right ADC Mixer
2		R/W	0	Select Microphone Input 1 to Right ADC Mixer
1		R/W	0	Select Microphone Input 2 to Right ADC Mixer
0		-	-	-

ADC Output Digital Gain

The IC includes separate digital level control for the left and right ADC outputs (Figure 13). To optimize dynamic range, use analog gain to adjust the signal level and set the digital level control to 0dB whenever possible. Digital level control is primarily used when adjusting the record level for digital microphones.

Table 18: Left ADC Digital Level Configuration Register

ADDRESS: 0x17				DESCRIPTION			
BIT	NAME	TYPE	PoR				
7	-	-	-	-			
6	AVLG[2:0]	R/W	0	Left ADC Digital Coarse Gain Configuration			
5			0	000 : 0dB	010 : +12dB	100 : +24dB	110 : +36dB
4			0	001 : +6dB	011 : +18dB	101 : +30dB	111 : +42dB
3	AVL[3:0]	R/W	0	Left ADC Digital Fine Adjust Gain Configuration			
2			0	0x0 : +3dB	0x4 : -1dB	0x8 : -5dB	0xC : -9dB
1			1	0x1 : +2dB	0x5 : -2dB	0x9 : -6dB	0xD : -10dB
0			1	0x2 : +1dB	0x6 : -3dB	0xA : -7dB	0xE : -11dB
				0x3 : +0dB	0x7 : -4dB	0xB : -8dB	0xF : -12dB

Table 19: Right ADC Digital Level Configuration Register

ADDRESS: 0x18				DESCRIPTION			
BIT	NAME	TYPE	PoR				
7	-	-	-	-			
6	AVRG[2:0]	R/W	0	Right ADC Digital Coarse Gain Configuration			
5			0	000 : 0dB	010 : +12dB	100 : +24dB	110 : +36dB
4			0	001 : +6dB	011 : +18dB	101 : +30dB	111 : +42dB
3	AVR[3:0]	R/W	0	Right ADC Digital Fine Adjust Gain Configuration			
2			0	0x0 : +3dB	0x4 : -1dB	0x8 : -5dB	0xC : -9dB
1			1	0x1 : +2dB	0x5 : -2dB	0x9 : -6dB	0xD : -10dB
0			1	0x2 : +1dB	0x6 : -3dB	0xA : -7dB	0xE : -11dB
				0x3 : +0dB	0x7 : -4dB	0xB : -8dB	0xF : -12dB

ADC Output Sidetone

Enable sidetone during full-duplex operation to add a low-level copy of the recorded audio signal to the playback audio signal (Figure 14). Sidetone is commonly used in telephony to allow the speaker to hear himself speak, providing a more natural user experience. The IC implements sidetone digitally. Doing so helps prevent unwanted feedback into the playback signal path and better matches the playback audio signal.

Table 20: ADC Sidetone Configuration Register

ADDRESS: 0x1A				DESCRIPTION			
BIT	NAME	TYPE	PoR				
7	DSTS[1:0]		0	ADC Sidetone Enable and Digital Source Configuration			
6			0	00 : No sidetone selected	10 : Right ADC	01 : Left ADC	11 : Left + Right ADC
5	-	-	-	-			
4	DVST[4:0]	R/W	0	ADC Sidetone Digital Gain Configuration			
3			0	0x00 : OFF	0x08 : -14.5dB	0x10 : -30.5dB	0x18 : -46.5dB
2			0	0x01 : -0.5dB	0x09 : -16.5dB	0x11 : -32.5dB	0x19 : -48.5dB
1			0	0x02 : -2.5dB	0x0A : -18.5dB	0x12 : -34.5dB	0x1A : -50.5dB
0			0	0x03 : -4.5dB	0x0B : -20.5dB	0x13 : -36.5dB	0x1B : -52.5dB
				0x04 : -6.5dB	0x0C : -22.5dB	0x14 : -38.5dB	0x1C : -54.5dB
				0x05 : -8.5dB	0x0D : -24.5dB	0x15 : -40.5dB	0x1D : -56.5dB
				0x06 : -10.5dB	0x0E : -26.5dB	0x16 : -42.5dB	0x1E : -58.5dB
				0x07 : -12.5dB	0x0F : -28.5dB	0x17 : -44.5dB	0x1F : -60.5dB

ADC Output Biquad Filter**Table 21: ADC Biquad Digital Preamplifier Level Configuration Register**

ADDRESS: 0x18				DESCRIPTION			
BIT	NAME	TYPE	PoR				
7	-	-	-				
6	-	-	-				
5	-	-	-				
4	-	-	-				
3	AVBQ[3:0]	R/W	0	ADC Biquad Digital Preamplifier Gain Configuration			
2			0	0x0 : +0dB	0x4 : -4dB	0x8 : -8dB	0xC : -12dB
1			0	0x1 : -1dB	0x5 : -5dB	0x9 : -9dB	0xD : -13dB
0			0	0x2 : -2dB	0x6 : -6dB	0xA : -10dB	0xE : -14dB
				0x3 : -3dB	0x7 : -7dB	0xB : -11dB	0xF : -15dB

Table 22: DSP Biquad Filter Enable Register

ADDRESS: 0x41				DESCRIPTION			
BIT	NAME	TYPE	PoR				
7	-	-	-				
6	-	-	-				
5	-	-	-				
4	-	-	-				
3	ADCBQEN	R/W	0	Enable Biquad filter in ADC path. 0 : biquad filter not used 1 : biquad filter used in ADC path			
2	EQ3BANDEN	R/W	0	Enable 3 Band EQ in DAC path. Bands 4 through 7 are not used. 0 : 3 band EQ disabled 1 : 3 band EQ enabled. Only valid if EQ7BANDEN == 0 and EQ5BANDEN == 0.			
1	EQ5BANDEN	R/W	0	Enable 5 Band EQ in DAC path. Bands 6 & 7 are not used. 0 : 5 band EQ disabled 1 : 5 band EQ enabled. Only valid if EQ7BANDEN == 0			
0	EQ7BANDEN	R/W	0	Enable 7 Band EQ in DAC path. 0 : 7 band EQ disabled. 1 : 7 band EQ enabled. This makes EQ5BANDEN and EQ3BANDEN redundant.			

Table 23: ADC Biquad Filter Coefficient

ADDRESS RANGE			NAME	TYPE	PoR	COEFFICIENT SEGMENT		
0xAF	0xB0	0xB1	ADC BIQUAD COEFFICIENT B0	R/W	0x00	ADC_B0[23:16]	ADC_B0[15:8]	ADC_B0[7:0]
0xB2	0xB3	0xB4	ADC BIQUAD COEFFICIENT B1	R/W	0x00	ADC_B1[23:16]	ADC_B1[15:8]	ADC_B1[7:0]
0xB5	0xB6	0xB7	ADC BIQUAD COEFFICIENT B2	R/W	0x00	ADC_B2[23:16]	ADC_B2[15:8]	ADC_B2[7:0]
0xB8	0xB9	0xBA	ADC BIQUAD COEFFICIENT A1	R/W	0x00	ADC_A1[23:16]	ADC_A1[15:8]	ADC_A1[7:0]
0xBB	0xBC	0xBD	ADC BIQUAD COEFFICIENT A2	R/W	0x00	ADC_A2[23:16]	ADC_A2[15:8]	ADC_A2[7:0]

Digital Audio Interface (DAI) Configuration
Digital Data Path

Table 24: Digital Audio Interface (DAI) Input / Output Configuration Register

ADDRESS: 0x25				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	LTEN	R/W	0	Enables Data Loop Through from the ADC Output to the DAC Input 1 : ADC to DAC loop-through enabled. 0 : ADC to DAC loop-through disabled.
4	LBEN	R/W	0	Enables Data Loop Back from the SDIEN Input to the SDOEN Output 1 : DAI SDIN used as SDOUT data source 0 : ADC used as SDOUT data source.
3	DMONO	R/W	0	Enables DAC Mono Mode where SDIN L/R are Mixed and Input to DAC L/R 1 : The left and right channel SDIN input data are mixed together and input to both the left and right DAC channel signal paths. 0 : The SDIN DAC input data is treated as left/right stereo signal data processed separately. When operating in mono voice mode (MODE=1) stereo data may still be input via SDIN and optionally mixed using DMONO=1.
2	HIZOFF	R/W	0	Disables Hi-Z Mode for SDOUT 1 : The SDOUT pin drives a valid logic level after all data bits have been transferred out of the part. 0 : The SDOUT pin goes to a high impedance state after all 16 ADC data bits have been transferred out of the part, allowing the SDOUT line to be shared to the destination by other devices
1	SDOEN	R/W	0	Enables the Serial Data Output 1 : Serial data output enabled. 0 : Serial data output disabled.
0	SDIEN	R/W	0	Enables the Serial Data Input 1 : Serial data input enabled. 0 : Serial data input disabled.

Digital Filtering**Table 25: Digital Audio Interface (DAI) Filter Configuration Register**

ADDRESS: 0x26				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	MODE	R/W	1	Enables the CODEC DSP FIR Music filters (Default IIR Voice Filters) 0 : The CODEC DSP filters operate in IIR Voice mode with stop band frequencies below the $fs/2$ Nyquist rate. The Voice mode filters are optimized for 8kHz or 16kHz voice application use. 1 : The CODEC DSP filters operate in a linear phase FIR Audio mode with optional DC blocking that may be enabled using the AHPF and DHPF I2C bits. The Audio mode filters are optimized to maintain stereo imaging and operate at higher fs rates while utilizing lower power.
6	AHPF	R/W	0	Enables the ADC DC Blocking Filter 0 : DC blocking filter disabled 1 : DC blocking filter enabled
5	DHPF	R/W	0	Enables the DAC DC Blocking Filter 0 : DC blocking filter disabled 1 : DC blocking filter enabled
4	DHF	R/W	0	Enables the DAC High Sample Rate Mode (LRCLK > 50kHz, FIR Only) 1 : LRCLK is greater than 50kHz. 4x FIR interpolation filter used. 0 : LRCLK is less than 50kHz. 8x FIR interpolation filter used.
3	-	-	-	-
2	-	-	-	-
1	-	-	-	-
0	-	-	-	-

DAI Clock Control

The digital signal paths in the IC require a master clock (MCLK) between 10MHz and 60MHz to function. The MAX98090 requires an internal clock between 10MHz and 20MHz. A prescaler divides MCLK by 1, 2, or 4 to create the internal clock (PCLK). PCLK is used to clock all portions of the IC. The MAX98089 includes a digital audio signal path, capable of supporting any sample rate from 8kHz to 96kHz.

Table 26: Master Mode Clock Configuration Register

ADDRESS: 0x21				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	MAS	R/W	0	Master Mode Enable 1 : Master mode (LRCLK and BCLK timing signals generated internally; LRCLK and BCLK configured as outputs). 0 : Slave mode (LRCLK and BCLK accepted from external source; LRCLK and BCLK configured as inputs).
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	BSEL[2:0]	R/W	0	Bit Clock (BCLK) Rate Configuration (Master Mode Only) 000 : off 100 : PCLK / 2 001 : 32 x fs 101 : PCLK / 4 010 : 48 x fs 110 : PCLK / 8 011 : 64 x fs 111 : PCLK / 16
1			0	
0			0	

Table 27: Digital Audio Interface (DAI) Format Configuration Register

ADDRESS: 0x22				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	RJ	R/W	0	Configures the DAI for Right Justified Mode (No Data Delay) 0 : left justified mode with optional data delay 1 : right justified mode. DLY register is not used. Note: TDM has priority over RJ.
4	WCI	R/W	0	Configures the DAI for Frame Clock (LRCLK) Inversion TDM1 = 0: 1 : Right-channel data is transmitted while LRCLK is low. 0 : Left-channel data is transmitted while LRCLK is low. TDM1 = 1: 0 : Start of a new frame is signified by the rising edge of the LRCLK pulse. 1 : Start of a new frame is signified by the falling edge of the LRCLK pulse.
3	BCI	R/W	0	Configures the DAI for Bit Clock (BCLK) Inversion 1 : SDIN is accepted on the falling edge of BCLK. 0 : SDIN is accepted on the rising edge of BCLK. Master Mode: 1 : LRCLK transitions occur on the rising edge of BCLK. 0 : LRCLK transitions occur on the falling edge of BCLK.
2	DLY	R/W	0	Configures the DAI for Data Delay (I2S Standard) 1 : The most significant bit of an audio word is latched at the second BCLK edge after the LRCLK transition. 0 : The most significant bit of an audio word is latched at the first BCLK edge after the LRCLK transition. Set DLY1/DLY2 = 1 to conform to the I2S standard. DLY1/DLY2 are only effective when TDM1/TDM2 = 0.
1	WS[1:0]	R/W	0	DAI Input Data Word Size If RJ = 1: 00 : 16-bits 01 : 20-bits 10 : 24-bits 11 : Reserved
0			0	If RJ = 0: 00 : 16-bits 01, 10, 11 : 20-bits

Slave Mode
Master Mode

Clock Configuration**Table 28: System Master Clock (MCLK) Prescaler Configuration Register**

ADDRESS: 0x1B				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	PSCLK[1:0]	R/W	0	Master Clock (MCLK) Prescaler Configuration 00 : Disabled 01 : MCLK / 1, 10MHz <= MCLK <= 20MHz 10 : MCLK / 2, 20MHz < MCLK <= 40MHz 11 : MCLK / 4, 40MHz < MCLK <= 60MHz
4			0	
3	-	-	-	-
2	-	-	-	-
1	-	-	-	-
0	-	-	-	-

Table 29: Clock Mode Configuration Register

ADDRESS: 0x1B				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	FREQ1[3:0]	R/W	0	Exact Integer Sampling Frequency (LRCLK) Configuration Allows integer sampling on DAI1 for specific PCLK frequencies in 8kHz or 16kHz voice modes. All modes 0x8 – 0xF are available in either Master or Slave modes of operation. If the exact indicated PCLK/LRCLK ratio cannot be guaranteed by the user, AnyClock mode (0x0) should be used. Any FREQ setting other than 0x0 overrides the PLL and NI settings.
6			0	
5			0	
4			0	
3	-	-	-	-
2	-	-	-	-
1	-	-	-	-
0	USE_MI1	R/W	0	Set the PLL to use MI1[15:0] to set a More Accurate Frequency Ratio 0 : M = 65536 1 : M is set by PLLM register.

Frequency Ratio

The NI and MI registers are used to set up the clock generation counter in Master Mode. They can be used under the following conditions:

- Master Mode (MAS = 1)
- All of the System Clock Quick Setup bits (Index 0x04) are set to 0
- FREQ1 bit is set to 0

To set the NI/MI values follow the following method:

1. Choose Over Sampling Rate (OSR). If $f_{PCLK} \geq 256 \times SR$, then OSR = 128 (otherwise OSR = 64).
2. Calculate $f_{OSR} = SR \times OSR$
3. Choose MI. This is $f_{PCLK}/GCD(f_{PCLK}, f_{OSR})$
4. Choose NI. This is $f_{OSR} \times MI/f_{PCLK}$

Table 30: Any Clock Configuration Register 1 (NI1 MSBs)

ADDRESS: 0x1D				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	Upper Half of the PLL N Value used in Master Mode Clock Generation to Calculate the Frequency Ratio (Integer or NI Master Mode).
6	NI1[14:8]	R/W	0	
5			0	
4			0	
3			0	
2			0	
1			0	
0			0	

Table 31: Any Clock Configuration Register 2 (NI1 LSBs)

ADDRESS: 0x1E				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	NI1[7:0]	R/W	0	Lower Half of the PLL N Value used in Master Mode Clock Generation to Calculate the Frequency Ratio (Integer or NI Master Mode).
6			0	
5			0	
4			0	
3			0	
2			0	
1			0	
0			0	

Table 32: Any Clock Configuration Register 3 (MI1 MSBs)

ADDRESS: 0x1F				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	MI1[15:8]	R/W	0	
6			0	
5			0	
4			0	
3			0	
2			0	
1			0	
0			0	

Table 33: Any Clock Configuration Register 4 (MI1 LSBs)

ADDRESS: 0x20				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	MI1[7:0]	R/W	0	
6			0	
5			0	
4			0	
3			0	
2			0	
1			0	
0			0	

DAI TDM Mode**Table 34: Digital Audio Interface (DAI) TDM Format Register 1**

ADDRESS: 0x23				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	-	-	-	-
1	FSW	R/W	0	Configures the DAI Frame Sync Pulse Width 1 : Frame sync pulse extended to the width of the entire data word. (TDM1/TDM2 = 1 only) 0 : Frame sync pulse is one bit wide
0	TDM	R/W	0	Enables the DAI for Time Division Multiplex (TDM) Mode 1 : Enables time-division multiplex mode and configures the audio interface to accept PCM data. 0 : Disables time-division multiplex mode.

Table 35: Digital Audio Interface (DAI) TDM Format Register 2

ADDRESS: 0x24				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	SLOTL[1:0]	R/W	0	Selects the Time Slot to use for Left Channel Data in TDM Mode 00 : Time Slot 1 10 : Time Slot 3 01 : Time Slot 2 11 : Time Slot 4
6			0	
5	SLOTR[1:0]	R/W	0	Selects the Time Slot to use for Right Channel Data in TDM Mode 00 : Time Slot 1 10 : Time Slot 3 01 : Time Slot 2 11 : Time Slot 4
4			0	
3	SLOTDLY[3:0]	R/W	0	Enables Data Delay for Slot 4 in TDM Mode
2			0	Enables Data Delay for Slot 3 in TDM Mode
1			0	Enables Data Delay for Slot 2 in TDM Mode
0			0	Enables Data Delay for Slot 1 in TDM Mode

Digital to Analog Converter (DAC) Configuration
DAC Input Digital Level
Voice Gain
Playback Level

Table 36: Digital Audio Interface (DAI) Playback Level Configuration Register

ADDRESS: 0x27				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	DV1M	R/W	0	Enables the DAI DAC Data Input Mute
6	-	-	-	-
5	DV1G[1:0]	R/W	0	DAI Digital Input Coarse Adjust Gain Configuration 00 : 0dB 10 : +12dB
4			0	01 : +6dB 11 : +18dB
3	DV1[3:0]	R/W	0	DAI Digital Input Fine Adjust Gain Configuration
2			0	0x0 : 0dB 0x4 : -4dB 0x8 : -8dB 0xC : -12dB
1			1	0x1 : -1dB 0x5 : -5dB 0x9 : -9dB 0xD : -13dB
0			1	0x2 : -2dB 0x6 : -6dB 0xA : -10dB 0xE : -14dB
				0x3 : -3dB 0x7 : -7dB 0xB : -11dB 0xF : -15dB

Automatic Level Control**Table 37: Automatic Level Control (ALC) Timing Register**

ADDRESS: 0x33				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	ALCEN	R/W	0	DAC ALC Enable 0 : ALC disabled 1 : ALC enabled
6	ALCRLS[2:0]	R/W	0	DAC ALC Release Time Configuration
5		R/W	0	0x0 : 8s 0x2 : 2s 0x4 : 0.5s 0x6 : 0.125s
4		R/W	0	0x1 : 4s 0x3 : 1s 0x5 : 0.25s 0x7 : 0.0625s
3	-	-	-	-
2	ALCATK[2:0]	R/W	0	DAC ALC Attack Time Configuration
1		R/W	0	0x0 : 0.5ms 0x2 : 5ms 0x4 : 25ms 0x6 : 100ms
0		R/W	0	0x1 : 1ms 0x3 : 10ms 0x5 : 50ms 0x7 : 200ms

Table 38: Automatic Level Control (ALC) Compressor Register

Table 39: Automatic Level Control (ALC) Expander Register

ADDRESS: 0x35				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	ALCEXP[2:0]	R/W	0	DAC ALC Expansion Ratio Configuration 0x0 : 1:1 0x1 : 2:1 0x2 : 3:1
6			0	
5			0	
4	ALCTHC[4:0]	R/W	0	DAC ALC Expansion Threshold Configuration
3			0	0x00 : -35dB 0x08 : -43dB 0x10 : -51dB 0x18 : -59dB
2			0	0x01 : -36dB 0x09 : -44dB 0x11 : -52dB 0x19 : -60dB
1			0	0x02 : -37dB 0x0A : -45dB 0x12 : -53dB 0x1A : -61dB
0			0	0x03 : -38dB 0x0B : -46dB 0x13 : -54dB 0x1B : -62dB
			0	0x04 : -39dB 0x0C : -47dB 0x14 : -55dB 0x1C : -63dB
			0	0x05 : -40dB 0x0D : -48dB 0x15 : -56dB 0x1D : -64dB
				0x06 : -41dB 0x0E : -49dB 0x16 : -57dB 0x1E : -65dB
				0x07 : -42dB 0x0F : -50dB 0x17 : -58dB 0x1F : -66dB

Table 40: Automatic Level Control (ALC) Gain Configuration Register

ADDRESS: 0x36				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	DAC ALC Make-Up Gain Configuration
6	-	-	-	
5	-	-	-	
4	ALCG[4:0]	R/W	0	
3			0	0x0 : +0dB 0x4 : +4dB 0x8 : +8dB 0xC : +12dB
2			0	0x1 : +1dB 0x5 : +5dB 0x9 : +9dB 0xD : reserved
1			0	0x2 : +2dB 0x6 : +6dB 0xA : +10dB 0xE : reserved
0			0	0x3 : +3dB 0x7 : +7dB 0xB : +11dB 0xF : reserved

DAC Input Parametric Equalizer**Table 41: DSP Biquad Filter Enable Register**

ADDRESS: 0x41				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	ADCBQEN	R/W	0	Enable Biquad filter in ADC path. 0 : biquad filter not used 1 : biquad filter used in ADC path
2	EQ3BANDEN	R/W	0	Enable 3 Band EQ in DAC path. Bands 4 through 7 are not used. 0 : 3 band EQ disabled 1 : 3 band EQ enabled. Only valid if EQ7BANDEN == 0 and EQ5BANDEN == 0.
1	EQ5BANDEN	R/W	0	Enable 5 Band EQ in DAC path. Bands 6 & 7 are not used. 0 : 5 band EQ disabled 1 : 5 band EQ enabled. Only valid if EQ7BANDEN == 0
0	EQ7BANDEN	R/W	0	Enable 7 Band EQ in DAC path. 0 : 7 band EQ disabled. 1 : 7 band EQ enabled. This makes EQ5BANDEN and EQ3BANDEN redundant.

Table 42: Parametric Equalizer Playback Level Configuration Register

ADDRESS: 0x28				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	/EQCLP\	R/W	0	Enables DAI Digital Input Equalizer Clipping Detection 1 : Equalizer Clip detect disabled 0 : Equalizer Clip detect enabled
3	DVEQ[3:0]	R/W	0	DAI Digital Input Equalizer Attenuation Level Configuration
2			0	
1			0	
0			0	
				0x0 : +0dB 0x4 : -4dB 0x8 : -8dB 0xC : -12dB 0x1 : -1dB 0x5 : -5dB 0x9 : -9dB 0xD : -13dB 0x2 : -2dB 0x6 : -6dB 0xA : -10dB 0xE : -14dB 0x3 : -3dB 0x7 : -7dB 0xB : -11dB 0xF : -15dB

Table 43: Parametric Equalizer Band N (1-7) Biquad Filter Coefficient Registers

ADDRESS RANGE (BY BAND)							NAME	TYPE	PoR	COEFFICIENT SEGMENT
1	2	3	4	5	6	7				
0x46	0x55	0x64	0x73	0x82	0x91	0xA0	EQUALIZER BAND N COEFFICIENT B0	R/W	0x00	B0_N[23:16]
0x47	0x56	0x65	0x74	0x83	0x92	0xA1		R/W	0x00	B0_N[15:8]
0x48	0x57	0x66	0x75	0x84	0x93	0xA2		R/W	0x00	B0_N[7:0]
0x49	0x58	0x67	0x76	0x85	0x94	0xA3	EQUALIZER BAND N COEFFICIENT B1	R/W	0x00	B1_N[23:16]
0x4A	0x59	0x68	0x77	0x86	0x95	0xA4		R/W	0x00	B1_N[15:8]
0x4B	0x5A	0x69	0x78	0x87	0x96	0xA5		R/W	0x00	B1_N[7:0]
0x4C	0x5B	0x6A	0x79	0x88	0x97	0xA6	EQUALIZER BAND N COEFFICIENT B2	R/W	0x00	B2_N[23:16]
0x4D	0x5C	0x6B	0x7A	0x89	0x98	0xA7		R/W	0x00	B2_N[15:8]
0x4E	0x5D	0x6C	0x7B	0x8A	0x99	0xA8		R/W	0x00	B2_N[7:0]
0x4F	0x5E	0x6D	0x7C	0x8B	0x9A	0xA9	EQUALIZER BAND N COEFFICIENT A1	R/W	0x00	A1_N[23:16]
0x50	0x5F	0x6E	0x7D	0x8C	0x9B	0xAA		R/W	0x00	A1_N[15:8]
0x51	0x60	0x6F	0x7E	0x8D	0x9C	0xAB		R/W	0x00	A1_N[7:0]
0x52	0x61	0x70	0x7F	0x8E	0x9D	0xAC	EQUALIZER BAND N COEFFICIENT A2	R/W	0x00	A2_N[23:16]
0x53	0x62	0x71	0x80	0x8F	0x9E	0xAD		R/W	0x00	A2_N[15:8]
0x54	0x63	0x72	0x81	0x90	0x9F	0xAE		R/W	0x00	A2_N[7:0]

Analog Audio Output Configuration

The device features three different integrated flexible analog audio output drivers. The receiver / line output driver can be configured either as a differential receiver output (optimal for a 32Ω earpiece speaker) or as a stereo single ended line output driver. The stereo speaker output drivers are filterless class D amplifiers capable of driving both 4Ω and 8Ω speakers. The headphone output drivers utilize Maxim's DirectDrive architecture with an integrated charge pump, and provide configurable headphone and headset jack detection. Each analog audio output driver has an individual programmable gain mixer and amplifier. Each output mixer accepts any combination of signals from both the integrated DAC, and the analog microphone and line input drivers.

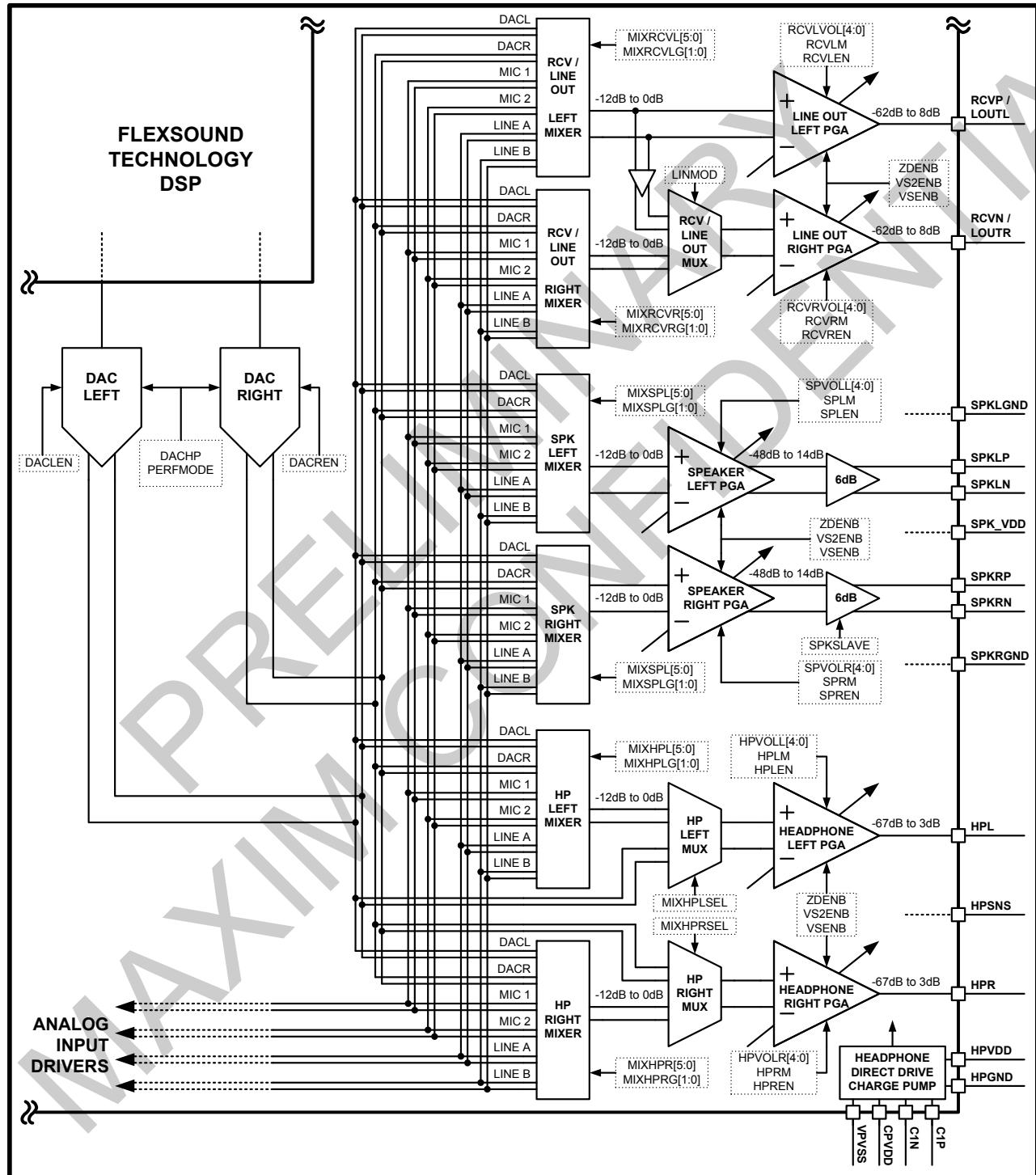


Figure 11: Analog Audio Output Functional Diagram

Analog Receiver (Earpiece) Output

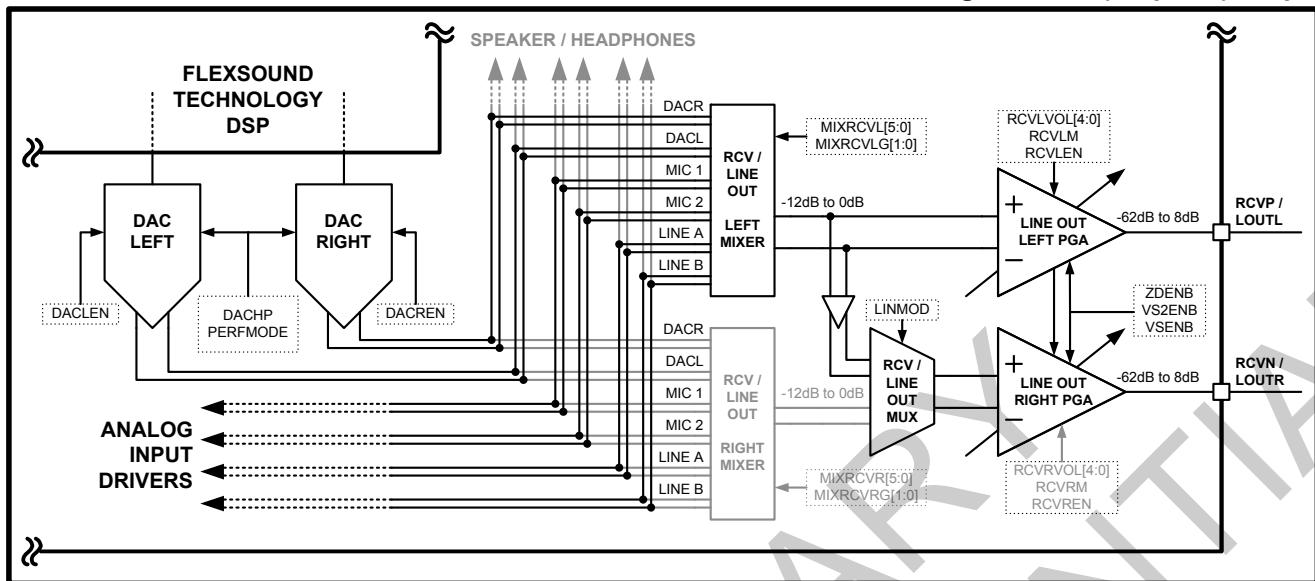


Figure 12: Receiver Output Functional Diagram

Table 44: Receiver and Left Line Output Mixer Source Configuration Register

ADDRESS: 0x37				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	MIXRCVL[5:0]	R/W	0	Selects DAC Left as the Input to the Receiver / Line Out Left Mixer
4			0	Selects DAC Right as the Input to the Receiver / Line Out Left Mixer
3			0	Selects Line A as the Input to the Receiver / Line Out Left Mixer
2			0	Selects Line B as the Input to the Receiver / Line Out Left Mixer
1			0	Selects MIC 1 as the Input to the Receiver / Line Out Left Mixer
0			0	Selects MIC 2 as the Input to the Receiver / Line Out Left Mixer

Table 45: Receiver and Left Line Output Mixer Level Control Register

ADDRESS: 0x38				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	-	-	-	-
1	MIXRCVLG[1:0]	R/W	0	Receiver / Line Output Left Mixer Gain Configuration. 00 : 0dB 01 : -6dB 10 : -9.5dB 11 : -12dB
0			0	Note: these gains are relative to the maximum output signal. In Line Output Mode this is 1Vpk, while in receiver BTL mode it is 1Vrms differential.

Table 46: Receiver and Left Line Output Volume Control Register

ADDRESS: 0x39				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	RCVLM	R/W	0	Receiver / Line Output Left Mute 0 : not muted 1 : muted
6	-	-	-	-
5	-	-	-	-
4	RCVLVOL[4:0]	R/W	1	Receiver / Line Output Left PGA Volume Configuration
3			0	0x1F : +8dB 0x17 : +2dB 0x0F : -12dB 0x07 : -35dB 0x1E : +7.5dB 0x16 : +1dB 0x0E : -14dB 0x06 : -38dB
2			1	0x1D : +7dB 0x15 : +0dB 0x0D : -17dB 0x05 : -42dB 0x1C : +6.5dB 0x14 : -2dB 0x0C : -20dB 0x04 : -46dB
1			0	0x1B : +6dB 0x13 : -4dB 0x0B : -23dB 0x03 : -50dB 0x1A : +5dB 0x12 : -6dB 0x0A : -26dB 0x02 : -54dB
0			1	0x19 : +4dB 0x11 : -8dB 0x09 : -29dB 0x01 : -58dB 0x18 : +3dB 0x10 : -10dB 0x08 : -32dB 0x00 : -62dB

*Receiver Gain Control
Receiver Output Mixer*

The IC's receiver amplifier accepts input from the stereo DAC, the line inputs (single-ended or differential), and the MIC inputs. Configure the mixer to mix any combination of the available sources. When more than one signal is selected, the mixed signal can be configured to attenuate 6dB, 9.5dB, or 12dB.

Analog Speaker Output

The IC integrates a stereo filterless Class D amplifier that offers much higher efficiency than Class AB without the typical disadvantages.

The high efficiency of a Class D amplifier is due to the switching operation of the output stage transistors. In a Class D amplifier, the output transistors act as current steering switches and consume negligible additional power. Any power loss associated with the Class D output stage is mostly due to the I₂R loss of the MOSFET on-resistance, and quiescent current overhead.

The theoretical best efficiency of a linear amplifier is 78%, however, that efficiency is only exhibited at peak output power. Under normal operating levels (typical music reproduction levels), efficiency falls below 30%, whereas the IC's Class D amplifier still exhibits 80% efficiency under the same conditions.

Traditional Class D amplifiers require the use of external LC filters or shielding to meet EN55022B and FCC electromagnetic-interference (EMI) regulation standards. Maxim's patented active emissions limiting edge-rate control circuitry reduces EMI emissions, allowing operation without any output filtering in typical applications.

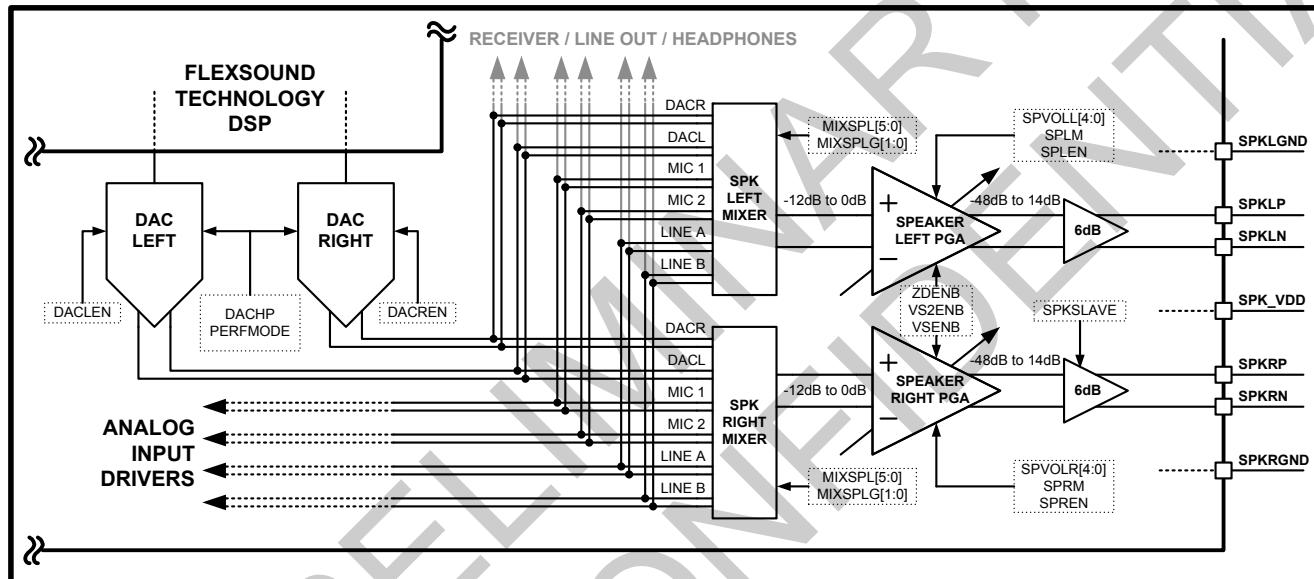


Figure 13: Class D Speaker Output Functional Diagram

**Speaker Class-D Output Amplifier
Speaker Gain Control**
Table 47: Left Speaker Amplifier Volume Control Register

ADDRESS: 0x31				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	SPLM	R/W	0	Left Speaker Output Mute Enable 1 : Left Speaker output muted. 0 : Speaker output volume set by the volume control bits. When going into mute, the volume will slew to full attenuation, after which mute will be asserted. When coming out of mute, the volume will slew from full attenuation to the current SPVOLL / SPVOLR setting.
6	-	-	-	-
5	SPVOLL[5:0]	R/W	1	Left Speaker Output Amplifier Volume Control Configuration
4			0	0x3F : +14dB 0x35 : +9dB 0x2B : -1dB 0x21 : -17dB 0x3E : +13.5dB 0x34 : +8dB 0x2A : -2dB 0x20 : -20dB
3			1	0x3D : +13dB 0x33 : +7dB 0x29 : -3dB 0x1F : -23dB 0x3C : +12.5dB 0x32 : +6dB 0x28 : -4dB 0x1E : -26dB
2			1	0x3B : +12dB 0x31 : +5dB 0x27 : -5dB 0x1D : -29dB 0x3A : +11.5dB 0x30 : +4dB 0x26 : -6dB 0x1C : -32dB
1			0	0x39 : +11dB 0x2F : +3dB 0x25 : -8dB 0x1B : -36dB 0x38 : +10.5dB 0x2E : +2dB 0x24 : -10dB 0x1A : -40dB
0			0	0x37 : +10dB 0x2D : +1dB 0x23 : -12dB 0x19 : -44dB 0x36 : +9.5dB 0x2C : +0dB 0x22 : -14dB 0x18 : -48dB

Table 48: Right Speaker Amplifier Volume Control Register

ADDRESS: 0x32				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	SPRM	R/W	0	Right Speaker Output Mute Enable 1 : Right Speaker output muted. 0 : Speaker output volume set by the volume control bits. When going into mute, the volume will slew to full attenuation, after which mute will be asserted. When coming out of mute, the volume will slew from full attenuation to the current SPVOLL / SPVOLR setting.
6	-	-	-	-
5	SPVOLR[5:0]	R/W	1	Right Speaker Output Amplifier Volume Control Configuration
4			0	0x3F : +14dB 0x35 : +9dB 0x2B : -1dB 0x21 : -17dB 0x3E : +13.5dB 0x34 : +8dB 0x2A : -2dB 0x20 : -20dB
3			1	0x3D : +13dB 0x33 : +7dB 0x29 : -3dB 0x1F : -23dB 0x3C : +12.5dB 0x32 : +6dB 0x28 : -4dB 0x1E : -26dB
2			1	0x3B : +12dB 0x31 : +5dB 0x27 : -5dB 0x1D : -29dB 0x3A : +11.5dB 0x30 : +4dB 0x26 : -6dB 0x1C : -32dB
1			0	0x39 : +11dB 0x2F : +3dB 0x25 : -8dB 0x1B : -36dB 0x38 : +10.5dB 0x2E : +2dB 0x24 : -10dB 0x1A : -40dB
0			0	0x37 : +10dB 0x2D : +1dB 0x23 : -12dB 0x19 : -44dB 0x36 : +9.5dB 0x2C : +0dB 0x22 : -14dB 0x18 : -48dB

Speaker Output Mixer

The IC's speaker amplifiers accept input from the stereo DAC, the line inputs (single-ended or differential), and the MIC inputs. Configure the mixer to mix any combination of the available sources. When more than one signal is selected, the mixer can be configured to attenuate the signal by 6dB, 9dB or 12dB.

Table 49: Left Speaker Mixer Configuration Register

ADDRESS: 0x2E				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	R/W
6	-	-	-	
5	MIXSPL[5:0]	R/W	0	Select Left DAC Output to Left Speaker Mixer
4			0	Select Right DAC Output to Left Speaker Mixer
3			0	Select Line Input A to Left Speaker Mixer
2			0	Select Line Input B to Left Speaker Mixer
1			0	Select Microphone Input 1 to Left Speaker Mixer
0			0	Select Microphone Input 2 to Left Speaker Mixer

Table 50: Right Speaker Mixer Configuration Register

ADDRESS: 0x2F				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	R/W
6	SPK_SLAVE	-	-	
5	MIXSPR[5:0]	R/W	0	Speaker Slave Mode Enable 0 : right channel clock always generated independently 1 : right channel speaker uses left channel speaker clock if both speaker channels are enabled
4			0	Select Left DAC Output to Right Speaker Mixer
3			0	Select Right DAC Output to Right Speaker Mixer
2			0	Select Line Input A to Right Speaker Mixer
1			0	Select Line Input B to Right Speaker Mixer
0			0	Select Microphone Input 1 to Right Speaker Mixer

Table 51: Speaker Mixer Gain Register

ADDRESS: 0x30				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	R/W
6	-	-	-	
5	-	-	-	
4	-	-	-	
3	MIXSPRG[1:0]	R/W	0	Right Speaker Mixer Gain Configuration 00 : +0dB 10 : -9.5dB
2			0	01 : -6dB 11 : -12dB
1	MIXSPLG[1:0]	R/W	0	Left Speaker Mixer Gain Configuration 00 : +0dB 10 : -9.5dB
0			0	01 : -6dB 11 : -12dB

Analog Headphone Output

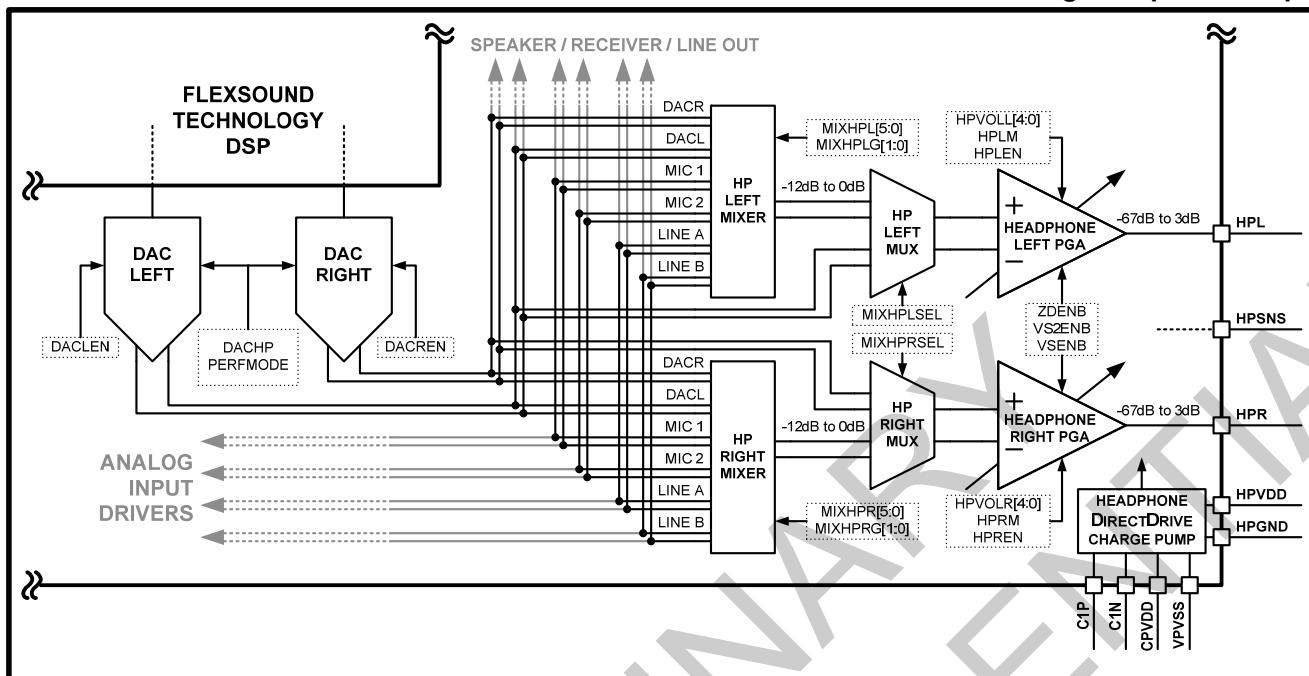


Figure 14: DirectDrive Headphone Output Functional Diagram

Table 52: Left Headphone Mixer Configuration Register

ADDRESS: 0x29				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	R/W
6	-	-	-	
5	MIXHPL[5:0]	0		
4	0			
3	0			
2	0			
1	0			
0	0			

Table 53: Right Headphone Mixer Configuration Register

ADDRESS: 0x2A				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	R/W
6	-	-	-	
5	MIXHPR[5:0]	0		
4	0			
3	0			
2	0			
1	0			
0	0			

Table 54: Headphone Mixer Control and Gain Register

ADDRESS: 0x2B				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	MIXHPRSEL	R/W	0	Select Headphone Mixer as Right Input Source (Default DAC Right Direct) 0 : DAC only source (best dynamic range and power consumption) 1 : Headphone mixer source
4	MIXHPLSEL	R/W	0	Select Headphone Mixer as Left Input Source (Default DAC Left Direct) 0 : DAC only source (best dynamic range and power consumption) 1 : Headphone mixer source
3	MIXHPRG[1:0]	R/W	0	Right Headphone Mixer Gain Configuration 00 : +0dB 10 : -9.5dB 01 : -6dB 11 : -12dB
2			0	
1	MIXHPLG[1:0]	R/W	0	Left Headphone Mixer Gain Configuration 00 : +0dB 10 : -9.5dB 01 : -6dB 11 : -12dB
0			0	

Table 55: Left Headphone Amplifier Volume Control Register

ADDRESS: 0x2C				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	HPLM	R/W	0	Left Headphone Output Mute Enable 1 : Headphone output muted. 0 : Headphone output volume set by the volume control bits. When going into mute, the volume will slew to full attenuation, after which mute will be asserted. When coming out of mute, the volume will slew from full attenuation to the current HPVOLL / HPVOLR setting.
6	-	-	-	-
5	-	-	-	-
4	HPVOLL[4:0]	R/W	1	Left Headphone Output Amplifier Volume Control Configuration
3			1	0x1F : +3dB 0x17 : -3dB 0x0F : -17dB 0x07 : -40dB 0x1E : +2.5dB 0x16 : -4dB 0x0E : -19dB 0x06 : -43dB
2			0	0x1D : +2dB 0x15 : -5dB 0x0D : -22dB 0x06 : -47dB
1			1	0x1C : +1.5dB 0x14 : -7dB 0x0C : -25dB 0x04 : -51dB 0x1B : +1dB 0x13 : -9dB 0x0B : -28dB 0x03 : -55dB
0			0	0x1A : +0dB 0x12 : -11dB 0x0A : -31dB 0x02 : -59dB 0x19 : -1dB 0x11 : -13dB 0x09 : -34dB 0x01 : -63dB 0x18 : -2dB 0x10 : -15dB 0x08 : -37dB 0x00 : -67dB

Table 56: Right Headphone Amplifier Volume Control Register

ADDRESS: 0x2D				DESCRIPTION			
BIT	NAME	TYPE	PoR				
7	HPRM	R/W	0	Right Headphone Output Mute Enable 1 : Headphone output muted. 0 : Headphone output volume set by the volume control bits. When going into mute, the volume will slew to full attenuation, after which mute will be asserted. When coming out of mute, the volume will slew from full attenuation to the current HPVOLL / HPVOLR setting.			
6	-	-	-	-			
5	-	-	-	-			
4	HPVOLR[4:0]	R/W	1	Right Headphone Output Amplifier Volume Control Configuration			
3			1	0x1F : +3dB	0x17 : -3dB	0x0F : -17dB	0x07 : -40dB
2			0	0x1E : +2.5dB	0x16 : -4dB	0x0E : -19dB	0x06 : -43dB
1			1	0x1D : +2dB	0x15 : -5dB	0x0D : -22dB	0x06 : -47dB
			0	0x1C : +1.5dB	0x14 : -7dB	0x0C : -25dB	0x04 : -51dB
0			0	0x1B : +1dB	0x13 : -9dB	0x0B : -28dB	0x03 : -55dB
				0x1A : +0dB	0x12 : -11dB	0x0A : -31dB	0x02 : -59dB
				0x19 : -1dB	0x11 : -13dB	0x09 : -34dB	0x01 : -63dB
				0x18 : -2dB	0x10 : -15d	0x08 : -37dB	0x00 : -67dB

DirectDrive Headphone Amplifier

Traditional single-supply headphone amplifiers have outputs biased at a nominal DC voltage (typically half the supply). Large coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both headphone and headphone amplifier.

Maxim's second-generation DirectDrive architecture uses a charge pump to create an internal negative supply voltage. This allows the headphone outputs of the ICs to be biased at GND while operating from a single supply (Figure TBD). Without a DC component, there is no need for the large DC-blocking capacitors. Instead of two large (220 μ F typ.) capacitors, the IC's charge pump requires 3 small ceramic capacitors, conserving board space, reducing cost, and improving the frequency response of the headphone amplifier.

Class H Operation

A Class H amplifier uses a Class AB output stage with power supplies that are modulated by the output signal. In the case of the ICs, two nominal power-supply differentials of 1.8V (+0.9V to -0.9V) and 3.6V (+1.8V to -1.8V) are available from the charge pump. Figure TBD shows the operation of the output-voltage-dependent power supply.

Charge Pump

The dual-mode charge pump generates both the positive and negative power supply for the headphone amplifier. To maximize efficiency, both the charge pump's switching frequency and output voltage change based on signal level.

When the input signal level is less than 10% of PVDD, the switching frequency is reduced to a low rate. This minimizes switching losses in the charge pump. When the input signal exceeds 10% of PVDD, the switching frequency increases to support the load current.

For input signals below 25% of PVDD, the charge pump generates Q(PVDD/2) to minimize the voltage drop across the amplifier's power stage and thus improve efficiency. Input signals that exceed 25% of PVDD cause the charge pump to output QPVDD. The higher output voltage allows for full output power from the headphone amplifier.

To prevent audible glitches when transitioning from the Q(PVDD/2) output mode to the QPVDD output mode, the charge pump transitions very quickly. This quick change draws significant current from PVDD for the duration of the transition. The bypass capacitor on PVDD supplies the required current and prevents droop on PVDD.

The charge pump's dynamic switching mode can be turned off through the I₂C interface. The charge pump can then be forced to output either Q(PVDD/2) or QPVDD regardless of input signal level

***Headphone Gain Control
Headphone Ground Sense***

HPSNS senses the ground return for the headphone load. For optimal performance, connect HPSNS to the ground pole of the jack through an isolated trace, as shown in Figure TBD. If HPSNS is not used, connect to the analog ground plane.

Headphone Output Mixer

The headphone amplifier mixer accepts input from the stereo DAC, the line inputs (single-ended or differential), and the MIC inputs. Configure the mixer to mix any combination of the available sources. When more than one signal is selected, the mixer can be configured to attenuate the signal by 6dB, 9.5dB, or 12dB. The stereo DAC can bypass the headphone mixers, and be connected directly to the headphone amplifiers to provide lower power consumption.

Analog Line Outputs

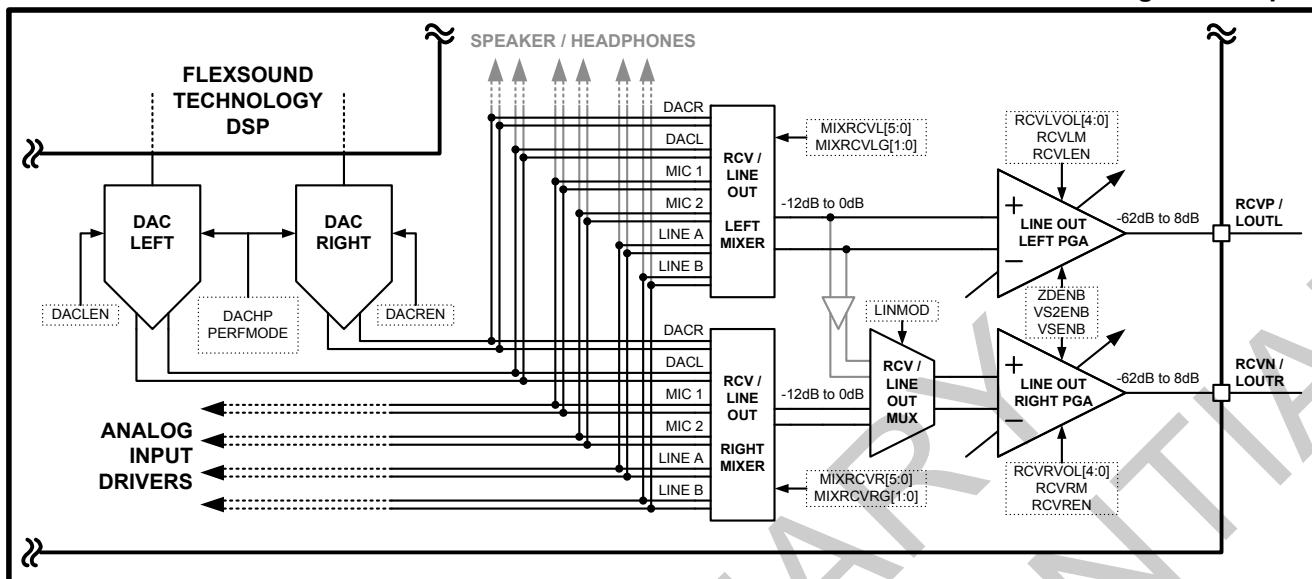


Figure 15: Stereo Single-Ended Line Output Functional Diagram

Table 57: Receiver and Left Line Output Mixer Source Configuration Register

ADDRESS: 0x37				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	MIXRCVL[5:0]	R/W	0	Selects DAC Left as the Input to the Receiver / Line Out Left Mixer
4			0	Selects DAC Right as the Input to the Receiver / Line Out Left Mixer
3			0	Selects Line A as the Input to the Receiver / Line Out Left Mixer
2			0	Selects Line B as the Input to the Receiver / Line Out Left Mixer
1			0	Selects MIC 1 as the Input to the Receiver / Line Out Left Mixer
0			0	Selects MIC 2 as the Input to the Receiver / Line Out Left Mixer

Table 58: Receiver and Left Line Output Mixer Level Control Register

ADDRESS: 0x38				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	Receiver / Line Output Left Mixer Gain Configuration. R/W Note: these gains are relative to the maximum output signal. In Line Output Mode this is 1Vpk, while in receiver BTL mode it is 1Vrms differential.
6	-	-	-	
5	-	-	-	
4	-	-	-	
3	-	-	-	
2	-	-	-	
1	MIXRCVLG[1:0]	R/W	0	00 : 0dB 10 : -9.5dB 01 : -6dB 11 : -12dB
0			0	

Table 59: Receiver and Left Line Output Volume Control Register

ADDRESS: 0x39				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	RCVLM	R/W	0	Receiver / Line Output Left Mute 0 : not muted 1 : muted
6	-	-	-	-
5	-	-	-	-
4	RCVLVOL[4:0]	R/W	1	Receiver / Line Output Left PGA Volume Configuration
3			0	0x1F : +8dB 0x17 : +2dB 0x0F : -12dB 0x07 : -35dB 0x1E : +7.5dB 0x16 : +1dB 0x0E : -14dB 0x06 : -38dB
2			1	0x1D : +7dB 0x15 : +0dB 0x0D : -17dB 0x05 : -42dB 0x1C : +6.5dB 0x14 : -2dB 0x0C : -20dB 0x04 : -46dB
1			0	0x1B : +6dB 0x13 : -4dB 0x0B : -23dB 0x03 : -50dB 0x1A : +5dB 0x12 : -6dB 0x0A : -26dB 0x02 : -54dB
0			1	0x19 : +4dB 0x11 : -8dB 0x09 : -29dB 0x01 : -58dB 0x18 : +3dB 0x10 : -10dB 0x08 : -32dB 0x00 : -62dB

Table 60: Right Line Output Mixer Source Configuration Register

ADDRESS: 0x3A				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	LINMOD	R/W	0	Selects Between Receiver BTL mode and Line Output mode 1 : LINEOUT mode. Receiver output is a stereo pair of line outputs. All control of the Receiver output is from the left control bits. 0 : BTL mode. All control of the Receiver output is from the left control bits.
6	-	-	-	-
5	MIXRCVR[5:0]	R/W	0	Selects DAC Left as the Input to the Line Out Right Mixer
4			0	Selects DAC Right as the Input to the Line Out Right Mixer
3			0	Selects Line A as the Input to the Line Out Right Mixer
2			0	Selects Line B as the Input to the Line Out Right Mixer
1			0	Selects MIC 1 as the Input to the Line Out Right Mixer
0			0	Selects MIC 2 as the Input to the Line Out Right Mixer

Table 61: Right Line Output Mixer Level Control Register

ADDRESS: 0x3B				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	-	-	-	-
1	MIXRCVRG[1:0]	R/W	0	Line Output Right Mixer Gain Configuration. 00 : 0dB 10 : -9.5dB

0		0	01 : -6dB Note: these gains are relative to the maximum output signal. In Line Output Mode this is 1Vpk, while in receiver BTL mode it is 1Vrms differential.	11 : -12dB
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Table 62: Right Line Output Volume Control Register

ADDRESS: 0x3C				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	RCVRM	R/W	0	Line Output Right Mute 0 : not muted 1 : muted
6	-	-	-	-
5	-	-	-	-
4	RCVRVOL[4:0]	R/W	1	Line Output Right PGA Volume Configuration
3			0	0x1F : +8dB 0x17 : +2dB 0x0F : -12dB 0x07 : -35dB
2			1	0x1E : +7.5dB 0x16 : +1dB 0x0E : -14dB 0x06 : -38dB
1			0	0x1D : +7dB 0x15 : +0dB 0x0D : -17dB 0x05 : -42dB
0			1	0x1C : +6.5dB 0x14 : -2dB 0x0C : -20dB 0x04 : -46dB
				0x1B : +6dB 0x13 : -4dB 0x0B : -23dB 0x03 : -50dB
				0x1A : +5dB 0x12 : -6dB 0x0A : -26dB 0x02 : -54dB
				0x19 : +4dB 0x11 : -8dB 0x09 : -29dB 0x01 : -58dB
				0x18 : +3dB 0x10 : -10dB 0x08 : -32dB 0x00 : -62dB

**Line Output Gain Control
Line Output Mixer**

Click-and-Pop Reduction

The IC includes extensive click-and-pop reduction circuitry. The circuitry minimizes clicks and pops at turn-on, turn-off, and during volume changes.

Zero-crossing detection is implemented on all analog PGAs and volume controls to prevent large glitches when volume changes are made. Instead of making a volume change immediately, the change is made when the audio signal crosses the midpoint. If no zero-crossing occurs within the timeout window, the change is forced.

Volume slewing breaks up large volume changes into the smallest available step size and the steps through each step between the initial and final volume setting. When enabled, volume slewing also occurs at device turn-on and turn-off. During turn-on the volume is set to mute before the output is enabled. Once the output is on, the volume ramps to the desired level. At turn-off the volume is ramped to mute before the outputs are disabled.

When there is no audio signal zero-crossing detection can prevent volume slewing from occurring. Enable enhanced volume slewing to prevent the volume controller from requesting another volume level until the previous one has been set. Each step in the volume ramp then occurs after a zero crossing has occurred in the audio signal or the timeout window has expired. During turn-off, enhance volume slewing is always disabled.

Table 63: Zero-Crossing Detection and Volume Smoothing Configuration Register

ADDRESS: 0x40				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	/ZDEN\	R/W	0	<p>Zero-Crossing Detection</p> <p>1 : Volume changes made immediately upon request. 0 : Volume changes made only at zero crossings in the audio waveform or after approximately 100ms.</p> <p>The following register bits are affected by /ZDEN: PGAM1, PGAM2, HPVOLL, HPVOLR, RECVOLL, RECVOLR, SPVOLL, SPVOLR</p>
1	/VS2EN\	R/W	0	<p>Enhanced Volume Smoothing</p> <p>/VS2EN enhances the volume slew and is only used when /VSEN = 0.</p> <p>1 : Enhancement disabled. 0 : Slewed volume changes wait until the previous volume step has been applied to the output before changing to the next step.</p> <p>The following register bits are affected by /VS2EN: HPVOLL, HPVOLR, RECVOLL, RECVOLR, SPVOLL, SPVOLR</p>
0	/VSEN\	R/W	0	<p>Volume Adjustment Smoothing</p> <p>1 : Volume changes made by bypassing intermediate settings. 0 : Volume changes smoothed by stepping through intermediate values at a rate of one setting every 1ms.</p> <p>The following register bits are affected by /VSEN: HPVOLL, HPVOLR, RECVOLL, RECVOLR, SPVOLL, SPVOLR</p>

Jack Detection

The device features a software configurable jack detection block that can both sense the insertion and removal of a jack, as well as identify the type of load inserted (headphone or headset). Figure 16 shows the typical application circuit configuration for jack detection (and is the assumed configuration for the following sections)

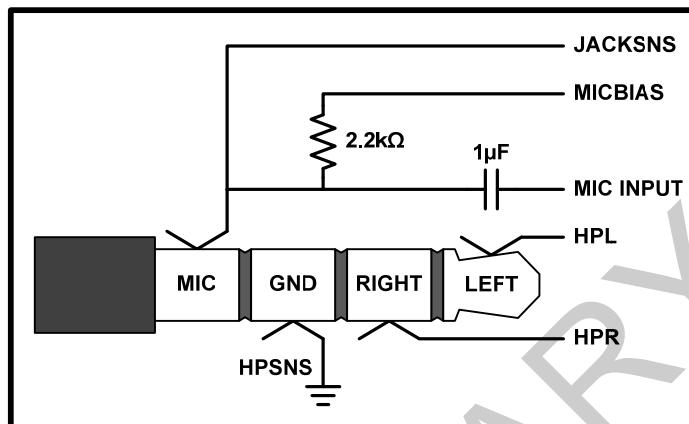


Figure 16: Typical Application Circuit for Jack Detection

To detect a jack insertion/removal, the device must be powered (but may be operating in or out of shutdown mode). Set JDETEN to enable the jack detection circuitry. When the device is in shutdown mode or the microphone bias is disabled (MICBIAS is high impedance), an internal pull-up is enabled on JACKSNS, and is referenced to the SPKLVDD supply. When the device is not in shutdown and the microphone bias is enabled, the internal pull-up is disabled (JACKSNS is high impedance). In this state, successful jack detection requires an external pull-up on JACKSNS to MICBIAS (Figure 16).

The device has both a strong and weak internal pull-up option. When JDWK is low (default, Table 64), the strong internal pull-up is used (approximately 2.2kΩ referenced to SPKLVDD). This configuration is capable of detecting and identifying both headphone and headset insertion. When JDWK is high, the weak internal pull-up (approximately 5μA to SPKLVDD) is used. This minimizes the supply current however the weak internal pull-up cannot identify headset insertion or accessory buttons.

Jack Insertion and Removal

The device detects jack insertion and removal by monitoring the voltage on JACKSNS with two internal comparators. The output of these comparators is used to set the state of the Jack Status Register bits (LSNS and JKSNS, Table 65). These comparators are only active when the JDETEN is set high. When the device is in shutdown and JDETEN is low, LSNS and JKSNS will retain their previous state regardless of the jack status.

When JDETEN is set high, LSNS and JKSNS can report three possible jack states (Table **TBD**). When LSNS = JKSNS = 1, jack detection is reporting that no jack is currently inserted. When LSNS = JKSNS = 0, jack detection is reporting that a jack is inserted, but that no microphone load was detected (headset). When LSNS = 0 and JKSNS = 1, jack detection is reporting that a jack is inserted and that a microphone load is present (Headset detection). If the weak internal pull-up is used, and the microphone bias is disabled, the jack detection block will not be able to identify a microphone load and will report the headphone detection state even if a headset is inserted.

When jack insertion or removal is detected (any change of state for LSNS and JKSNS), the Jack detection change flag is set (JDET, Table 66). In addition to this, an interrupt on /IRQ\ (to alert the microcontroller of the event) can also be triggered if IJDET is set (Table 67).

Accessory Button Detection

After jack insertion, the MAX98089 can detect button presses on accessories that include a microphone and a switch that shorts the microphone signal to ground. Set JDETEN to enable jack detection circuitry. Button presses can be detected either when MICBIAS is enabled or if it is disabled and the strong internal pull-up is used (JDWK = 0). A button press will change the state of JKSNS from 1 to 0 until the button is released, and this change in state will generate an event on the jack detection change flag (JDET).

Table 64: Jack Detect Configuration Register

ADDRESS: 0x3D				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	JDETEN	R/W	0	Jack Detect Enable 0 : Jack Detect Circuitry Disabled 1 : Jack Detect Circuitry Enabled
6	JDWK	R/W	0	JACKSNS Pull-up Configuration 0 : 2.4kΩ resistor to SPKLVDD (allows microphone detection) 1 : 5uA to SPKLVDD (minimizes supply current) When JDWK = 1, JACKSNS is slow to increase in voltage. Set JDWK = 0 before setting JDETEN = 1 to prevent false detection. Valid when MBIAS = 0 or /SHDN = 0.
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	-	-	-	-
1	JDEB[1:0]	R/W	0	Jack Detect Debounce Configures the jack detect debounce time
0			0	00 : 25ms 10 : 100ms 01 : 50ms 11 : 200ms

Table 65: Jack Status Register

ADDRESS: 0x02				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	LSNS	R	0	Microphone Load Sense (Valid only if JDETEN = 1) 0 : $V_{JACKSNS} \leq 0.95V \times V_{SUPPLY}$ 1 : $V_{JACKSNS} > 0.95V \times V_{SUPPLY}$ V_{SUPPLY} is determined by the state of MBEN and /SHDN such that: MBEN = 0 or /SHDN = 0 : $V_{SUPPLY} = V_{SPKLVDD}$ (Internal) MBEN = 1 and /SHDN = 1 : $V_{SUPPLY} = V_{MICBIAS}$ (Configuration of Figure 16)
1	JKSNS	R	0	Jack Connection Sense (Valid only if JDETEN = 1) 0 : $V_{JACKSNS} < 0.1V \times V_{SUPPLY}$ 1 : $V_{JACKSNS} \geq 0.1V \times V_{SUPPLY}$ V_{SUPPLY} is determined by the state of MBEN and /SHDN such that: MBEN = 0 or /SHDN = 0 : $V_{SUPPLY} = V_{SPKLVDD}$ (Internal) MBEN = 1 and /SHDN = 1 : $V_{SUPPLY} = V_{MICBIAS}$ (Configuration of Figure 16)
	-	-	-	-

Device Status Flags

The device uses register 0x01 (Table 66) and /IRQ\ to report the status of various device functions. The status register bits are set when their respective events occur, and cleared upon reading the register. Device status can be determined either by poling register 0x01, or by configuring /IRQ\ to pull low when specific events occur. /IRQ\ is an open-drain output that requires a pull-up resistor (10kΩ to **TBD**) for proper operation.

Table 66: Device Status Interrupt Register

ADDRESS: 0x01				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	CLD	CoR	0	Clipping Detect Flag 0 : No clipping has occurred. 1 : DAC or ADC clipping has occurred. CLD reports that the DAC input data or ADC output data is clipping due to excessive signal amplitude in the digital signal path. To resolve a clip condition in the signal path, the DAC gain settings and analog input gain settings should be lowered. As the CLD bit does not indicate where the overload has occurred, identify the source by lowering gains individually.
6	SLD	CoR	0	Slew Level Detect Flag 0 : No volume slewing sequences have completed. 1 : Volume slewing complete. SLD reports that any one of the programmable-gain arrays or volume controllers has completed slews from a previous setting to a new programmed setting. If multiple gain arrays or volume controllers are changed at the same time, in either the analog or digital domain, SLD flag will be set after the last slew adjusting in each domain. SLD also reports when the serial interface soft-start or soft-stop process has completed.
5	ULK	CoR	0	Digital PLL Unlock Flag 0 : PLL is locked if enabled and operating properly. 1 : When enabled, either of the PLL is not locked. ULK reports that the digital audio phase-locked loop for either interface became unlocked and input digital signal data is unreliable.
4	-	-	-	-
3	-	-	-	-
2	JDET	CoR	0	Jack Configuration Change Flag 0 : No change in jack configuration. 1 : Jack configuration has changed. JDET reports changes to any bits in the Jack Status register. Changes to the Jack Status bits are debounced before setting JDET. The debounce period is programmable using the JDEB bits.
1	ALCACT	CoR	0	ALC Compression Flag 0 : The ALC is either disabled or not in the compression region. 1 : The ALC is operating in the compression region.
0	ALCCLP	CoR	0	ALC Clipping Flag 0 : The ALC is either disabled or no clipping has occurred. 1 : ALC clipping has occurred.

Status Flag Masking

Register 0x03, the device status interrupt mask register (Table 67) determines which bits in the device status interrupt register (Table 66) can trigger a hardware interrupt on /IRQ\ (assert low). By default, all of the device status interrupts (except JDET) will only set the corresponding status bit and will not generate a hardware interrupt. Set the corresponding bit high in the mask register to enable hardware interrupts.

Table 67: Device Status Interrupt Mask Register

ADDRESS: 0x03				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	ICLD	R/W	0	Clipping Detect Interrupt Enable 0 : Clipping detection only sets CLD (0x01[7]). 1 : Clipping detection triggers /IRQ\ and sets CLD (0x02[7]).
6	ISLD	R/W	0	Slew Level Detect Interrupt Enable 0 : Slew level detection only sets SLD (0x01[6]). 1 : Slew level detection triggers /IRQ\ and sets SLD (0x02[6]).
5	IULK	R/W	0	Digital PLL Unlock Interrupt Enable 0 : PLL Unlock Condition only sets ULK (0x01[5]). 1 : PLL Unlock Condition triggers /IRQ\ and sets ULK (0x02[5]).
4	-	-	-	-
3	-	-	-	-
2	IJDET	R/W	1	Jack Configuration Change Interrupt Enable 0 : Changes in headset configuration only sets JDET (0x01[2]). 1 : Changes in headset configuration triggers /IRQ\ and sets JDET (0x01[2]).
1	IALCACT	R/W	0	ALC Compression Interrupt Enable 0 : ALC compression only sets ALCACT (0x01[1]). 1 : ALC compression triggers /IRQ\ and sets ALCACT (0x01[1]).
0	IALCCLP	R/W	0	ALC Clipping Interrupt Enable 0 : ALC clipping only sets ALCCLP (0x01[0]). 1 : ALC clipping triggers /IRQ\ and sets ALCCLP (0x01[0]).

Quick Setup Configuration**Table 68: System Clock Quick Setup Register**

ADDRESS: 0x04				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	26M	W	0	Setup Device for Operation with a 26MHz Master Clock (MCLK)
6	19P2M	W	0	Setup Device for Operation with a 19.2MHz Master Clock (MCLK)
5	13M	W	0	Setup Device for Operation with a 13MHz Master Clock (MCLK)
4	12P288M	W	0	Setup Device for Operation with a 12.288MHz Master Clock (MCLK)
3	12M	W	0	Setup Device for Operation with a 12MHz Master Clock (MCLK)
2	11P2896M	W	0	Setup Device for Operation with a 11.2896MHz Master Clock (MCLK)
1	-	-	-	-
0	256Fs	W	0	Setup Device for Operation with a 256 x fS MHz Master Clock (MCLK)

Table 69: Sample Rate Quick Setup Register

ADDRESS: 0x05				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	SR_96K	W	0	Setup Clocks and Filters for a 96kHz Sample Rate
4	SR_32K	W	0	Setup Clocks and Filters for a 32kHz Sample Rate
3	SR_48K	W	0	Setup Clocks and Filters for a 48kHz Sample Rate
2	SR_44K1	W	0	Setup Clocks and Filters for a 44.1kHz Sample Rate
1	SR_16K	W	0	Setup Clocks and Filters for a 16kHz Sample Rate
0	SR_8K	W	0	Setup Clocks and Filters for an 8kHz Sample Rate

Table 70: Digital Audio Interface (DAI) Quick Setup Register

ADDRESS: 0x06				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	-	-	-	-
6	-	-	-	-
5	RJ_M	W	0	Setup DAI for Right Justified Master Mode Operation
4	RJ_S	W	0	Setup DAI for Right Justified Slave Mode Operation
3	LJ_M	W	0	Setup DAI for Left Justified Master Mode Operation
2	LJ_S	W	0	Setup DAI for Left Justified Slave Mode Operation
1	I2S_M	W	0	Setup DAI for I2S Master Mode Operation
0	I2S_S	W	0	Setup DAI for I2S Slave Mode Operation

Table 71: Digital to Analog Converter (DAC) Path Quick Setup Register

ADDRESS: 0x07				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	DIG2_HP	W	0	Setup the DAC to Headphone Path
6	DIG2_EAR	W	0	Setup the DAC to Receiver Path
5	DIG2_SPK	W	0	Setup the DAC to Speaker Path
4	DIG2_LOUT	W	0	Setup the DAC to Line Out Path
3	-	-	-	-
2	-	-	-	-
1	-	-	-	-
0	-	-	-	-

Table 72: Microphone / Direct to Analog to Digital Converter (ADC) Path Quick Setup Register

ADDRESS: 0x08				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	IN12_MIC1	W	0	Setup the IN1-IN2 to Microphone 1 to ADCL Path
6	IN34_MIC2	W	0	Setup the IN3-IN4 to Microphone 2 to ADCR Path
5	IN56_MIC1	W	0	Setup the IN6-IN5 to Microphone 1 to ADCL Path (WLP Only)
4	IN56_MIC2	W	0	Setup the IN6-IN5 to Microphone 2 to ADCR Path (WLP Only)
3	IN12_DADC	W	0	Setup the IN1-IN2 Direct to ADCL Path
2	IN34_DADC	W	0	Setup the IN3-IN4 Direct to ADCR Path
1	IN56_DADC	W	0	Setup the IN6-IN5 Direct to ADCL Path (WLP Only)
0	-	-	-	-

Table 73: Line Input to Analog to Digital Converter (ADC) Path Quick Setup Register

ADDRESS: 0x09				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	IN12S_AB	W	0	Setup Stereo Single Ended Record: IN1/IN2 to Line In A/B to ADCL/R
6	IN34S_AB	W	0	Setup Stereo Single Ended Record: IN3/IN4 to Line In A/B to ADCL/R
5	IN56S_AB	W	0	Setup Stereo Single Ended Record: IN5/IN6 to Line In A/B to ADCL/R (WLP Only)
4	IN34D_A	W	0	Setup Mono Differential Record: IN3-IN4 to Line In A to ADCL
3	IN56D_B	W	0	Setup Mono Differential Record: IN6-IN5 to Line In B to ADCR (WLP Only)
2	-	-	-	-
1	-	-	-	-
0	-	-	-	-

Table 74: Analog Microphone Input to Analog Output Loop Quick Setup Register

ADDRESS: 0x0A				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	IN12_M1HPL	W	0	Setup the IN1-IN2 Differential to Microphone 1 to Headphone Left Path
6	IN12_M1SPKL	W	0	Setup the IN1-IN2 Differential to Microphone 1 to Speaker Left Path
5	IN12_M1EAR	W	0	Setup the IN1-IN2 Differential to Microphone 1 to Receiver Path
4	IN12_M1LOUTL	W	0	Setup the IN1-IN2 Differential to Microphone 1 to Lineout Left Path
3	IN34_M2HPR	W	0	Setup the IN3-IN4 Differential to Microphone 2 to Headphone Left Path
2	IN34_M2SPKR	W	0	Setup the IN3-IN4 Differential to Microphone 2 to Speaker Left Path
1	IN34_M2EAR	W	0	Setup the IN3-IN4 Differential to Microphone 2 to Receiver Path
0	IN34_M2LOUTR	W	0	Setup the IN3-IN4 Differential to Microphone 2 to Lineout Left Path

Table 75: Analog Line Input to Analog Output Loop Quick Setup Register

ADDRESS: 0x0B				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	IN12S_ABHP	W	0	Setup the IN1/IN2 Single Ended to Line In A/B to Headphone L/R Path
6	IN34D_ASPLK	W	0	Setup the IN3-IN4 Differential to Line In A to Speaker Left Path
5	IN34D_AEAR	W	0	Setup the IN3-IN4 Differential to Line In A to Receiver Path
4	IN12S_ABLOUT	W	0	Setup the IN1/IN2 Single Ended to Line In A/B to Lineout L/R Path
3	IN34S_ABHP	W	0	Setup the IN3/IN4 Single Ended to Line In A/B to Headphone L/R Path
2	IN56D_BSPKR	W	0	Setup the IN6-IN5 Differential to Line In B to Speaker Right Path (WLP Only)
1	IN56D_BEAR	W	0	Setup the IN6-IN5 Differential to Line In B to Receiver Path (WLP Only)
0	IN34S_ABLOUT	W	0	Setup the IN3/IN4 Single Ended to Line In A/B to Lineout L/R Path

Software Reset

The device provides a software reset (SWRESET, Table 76) that is used to return most registers to their default (PoR) states (The ADC Biquad and DAC Equalizer coefficient registers are not reset). The software reset register is a pushbutton, write only register. As a result, a read of this register always returns 0x00. Writing a logic high to SWRESET triggers a software register reset, while writing a logic low to SWRESET has no effect.

Table 76: Software Reset Register

ADDRESS: 0x00				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	SWRESET	W	0	Pushbutton Software Device Reset 0 : Writing a logic low to SWRESET has no effect. 1 : Reset all registers to their default PoR values. This excludes the ADC Biquad and DAC Equalizer filter coefficients (Table 23).
6	-	-	-	-
5	-	-	-	-
4	-	-	-	-
3	-	-	-	-
2	-	-	-	-
1	-	-	-	-
0	-	-	-	-

Device Revision Identification

The device provides a Revision ID Number register to allow the software to identify the current version of the device. The current device revision ID value is 0x42.

Table 77: Revision ID Number Register

ADDRESS: 0x45				DESCRIPTION
BIT	NAME	TYPE	PoR	
7	REV_ID[7:0]	R	0	Read back the revision ID of the device
6			1	
5			0	
4			0	
3			0	
2			0	
1			1	
0			0	

I²C Serial Interface

The MAX98090 features an I²C/SMBus™-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the MAX98090 and the master at clock rates up to 400kHz. Error! Reference source not found.TBD shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX98090 by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX98090 is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX98090 transmits the proper slave address followed by a series of nine SCL pulses. The MAX98090 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not acknowledge, and a STOP (P) condition. SDA operates as both an input and an open-drain output. A pull-up resistor, typically greater than 500Ω, is required on SDA. SCL operates only as an input. A pull-up resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX98090 from high voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the START and STOP Conditions section).

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 17). A START condition from the master signals the beginning of a transmission to the MAX98090. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

Early STOP Conditions

The MAX98090 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the read/write bit. For the MAX98090A, the seven most significant bits are 0010000. Setting the read/write bit to 1 (slave address = 0x21) configures the MAX98090A for read mode. Setting the read/write bit to 0 (slave address = 0x20) configures the MAX98090A for write mode. The address is the first byte of information sent to the MAX98090 after the START condition. Similarly, for the MAX98090B, the seven most significant bits are 0010001. Setting the read/write bit to 1 (slave address = 0x23) configures the MAX98090B for read mode. Setting the read/write bit to 0 (slave address = 0x22) configures the MAX98090B for write mode.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX98090_{_} uses to handshake receipt each byte of data when in write mode (Figure 18). The MAX98090_{_} pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master will retry communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX98090_{_} is in read mode. An acknowledgement is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the MAX98090_{_}, followed by a STOP condition.

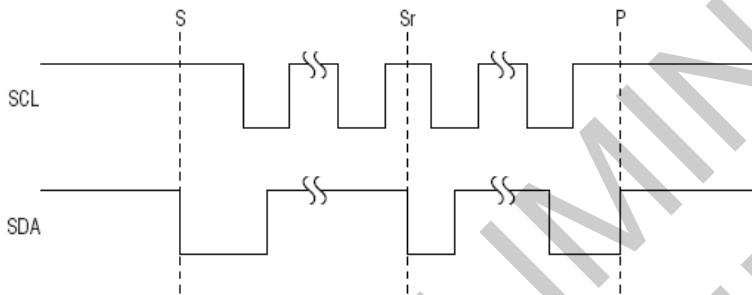


Figure 17: START, STOP, and REPEATED START Conditions

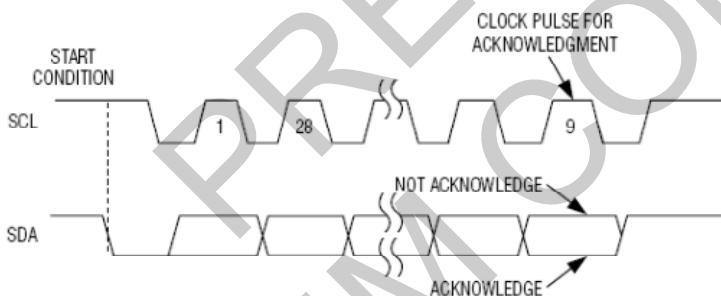


Figure 18: Acknowledge

Write Data Format

A write to the MAX98090_{_} includes transmission of a START condition, the slave address with the R/W\ bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 19 illustrates the proper frame format for writing one byte of data to the MAX98090_{_}. Figure 20 illustrates the frame format for writing n-bytes of data to the MAX98090_{_}.

The slave address with the R/W\ bit set to 0 indicates that the master intends to write data to the MAX98090. The MAX98090_{_} acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

The second byte transmitted from the master configures the MAX98090_{_}'s internal register address pointer. The pointer tells the MAX98090_{_} where to write the next byte of data. An acknowledge pulse is sent by the MAX98090 upon receipt of the address pointer data.

The third byte sent to the MAX98090_ contains the data that will be written to the chosen register. An acknowledge pulse from the MAX98090_ signals receipt of the data byte. The address pointer auto increments to the next register address after each received data byte. This auto-increment feature allows a master to write to sequential registers within one continuous frame. The master signals the end of transmission by issuing a STOP condition. Register addresses greater than 0xE7 are reserved. Do not write to these addresses.

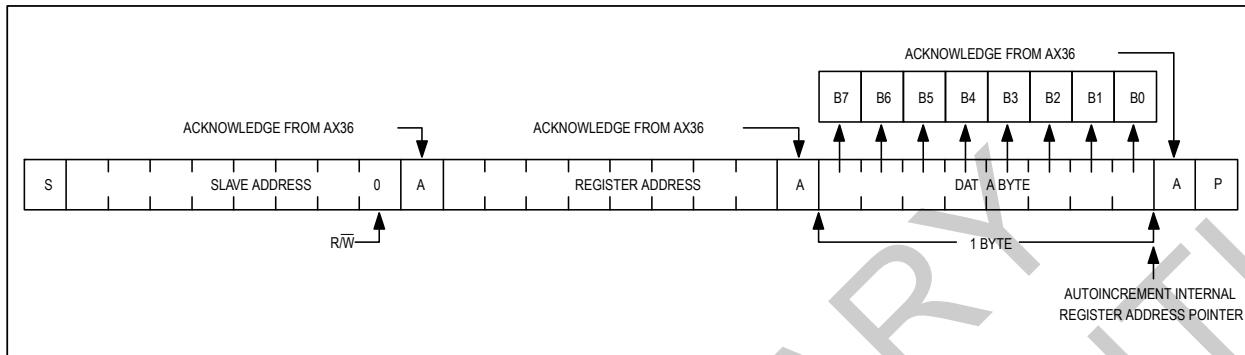


Figure 19: Writing One Byte of Data to the MAX98090.

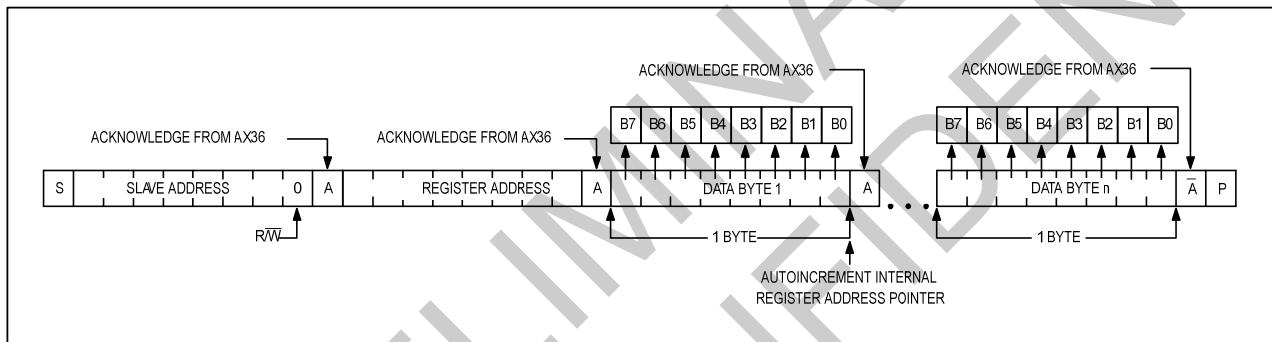


Figure 20: Writing n-Bytes of Data to the MAX98090

Read Data Format

Send the slave address with the R/W bit set to 1 to initiate a read operation. The MAX98090_ acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the MAX98090_ will be the contents of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer auto-increments after each read data byte. This auto-increment feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read will be from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the MAX98090's slave address with the R/W bit set to 0 followed by the register address. A REPEATED START condition is then sent followed by the slave address with the R/W bit set to 1. The MAX98090_ then transmits the contents of the specified register. The address pointer auto-increments after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 21 illustrates the frame format for reading one byte from the MAX98090_. Figure 22 illustrates the frame format for reading multiple bytes from the MAX98090_.

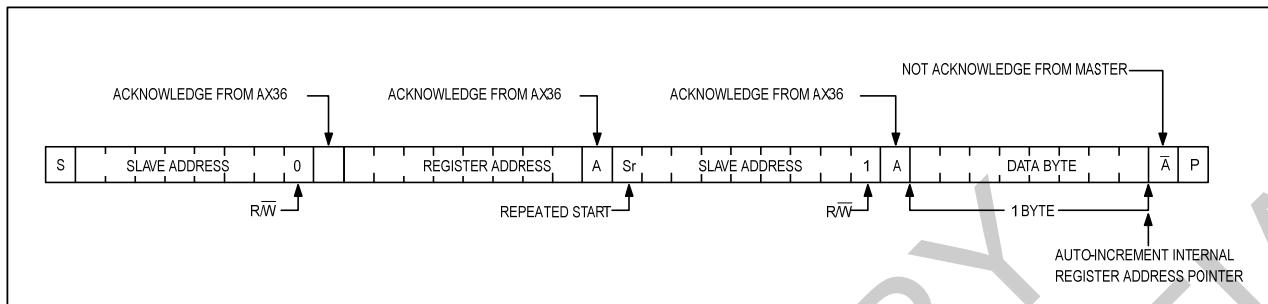


Figure 21: Reading One Byte of Data from the MAX98090_

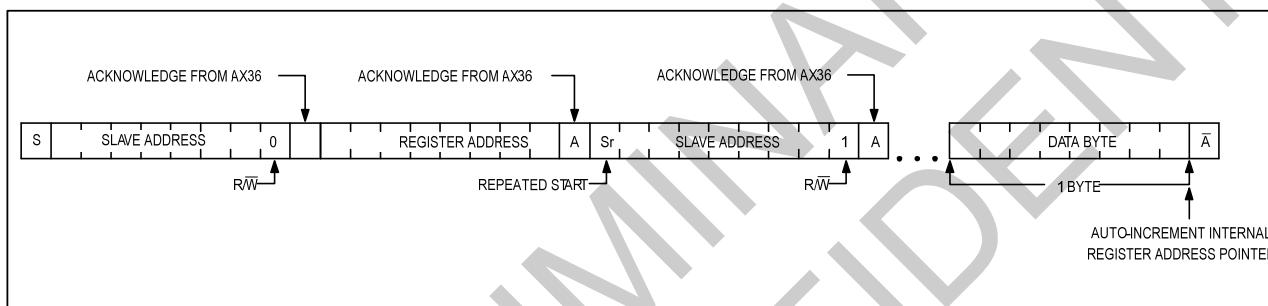


Figure 22: Reading n-Bytes of Data from the MAX98090_

APPLICATIONS INFORMATION**Typical Application Circuits**

Figures are two example application circuits for the device. The external components shown are the minimum required for the device to operate. Additional application specific components may be required.

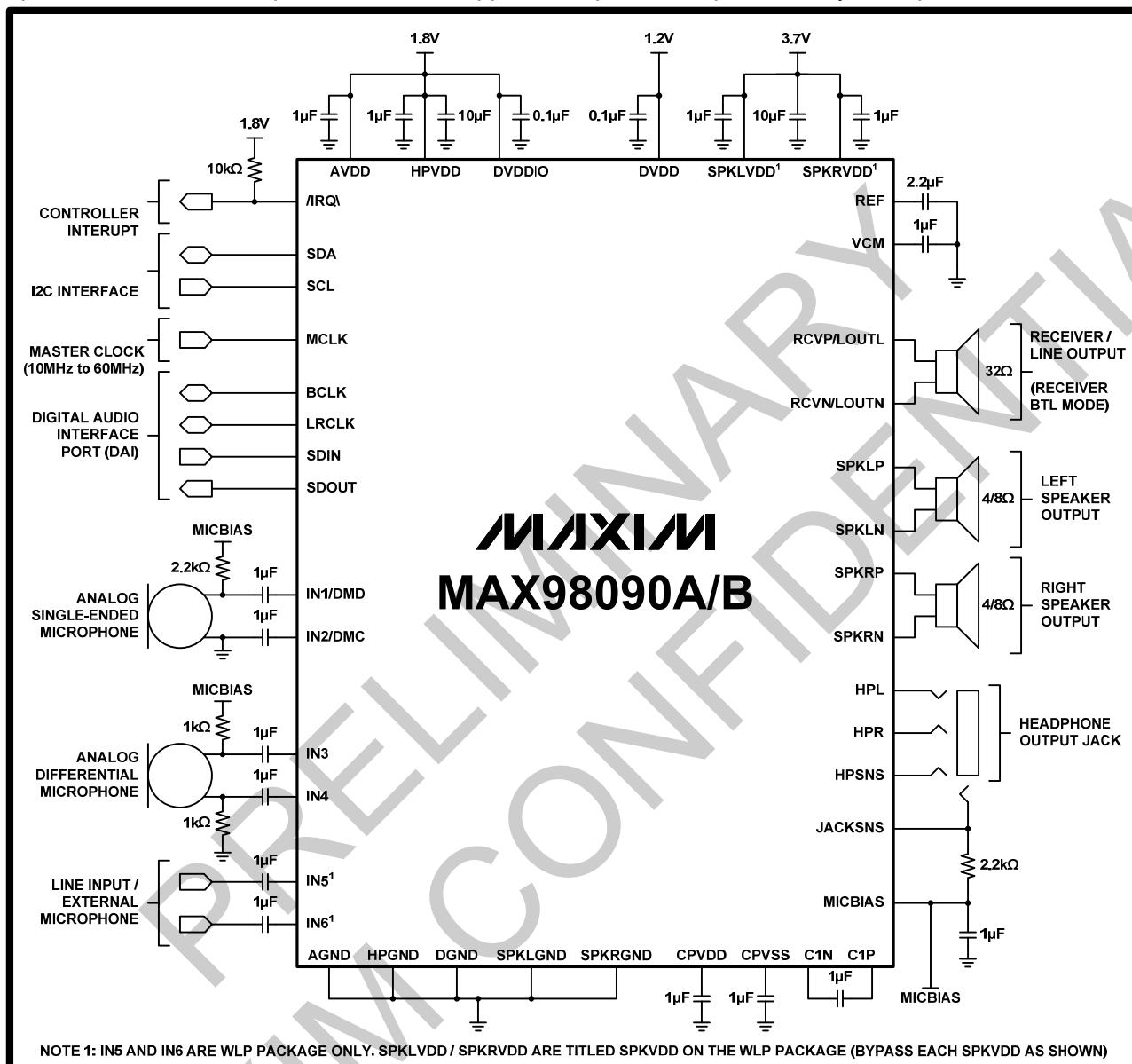


Figure 23: Typical Application Circuit with Analog Microphone Inputs and Receiver Output

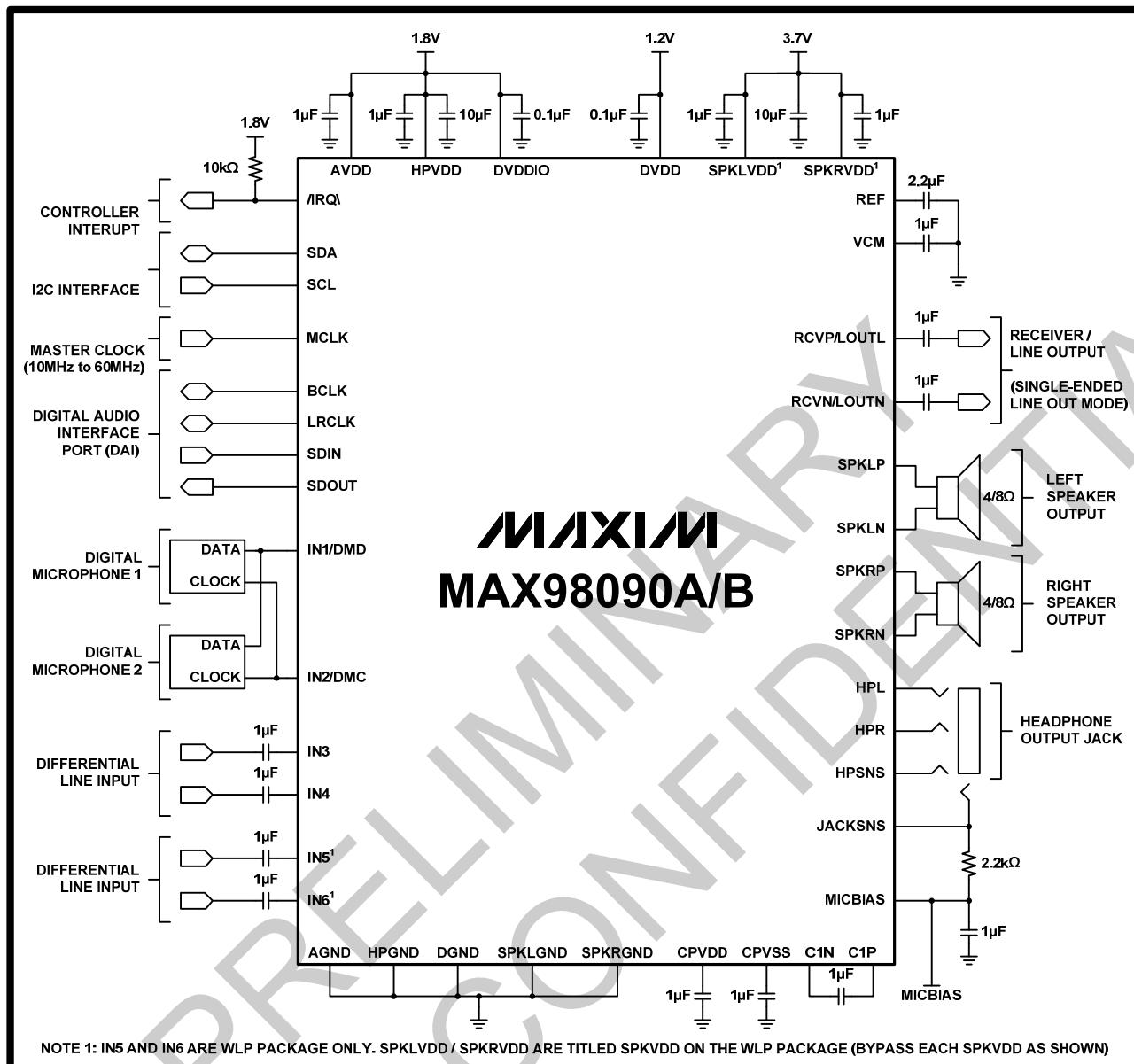


Figure 24: Typical Application Circuit with Digital Microphone Input and Stereo Line Outputs

Startup / Shutdown Register Sequencing

To ensure proper device initialization and minimal click-and-pop, program the devices control registers in the correct order. To shutdown the MAX98090, simply set /SHDN\ = 0. Table 78 details an example startup sequence for the device. To minimize click and pop on the analog output drivers (headphones, speakers, receiver, and line outputs), the output drivers should be powered using the following sequence:

1. Prior to powering the device (/SHDN\ = 0) and before enabling the outputs, the output driver mute(s) should be enabled and the PGA gain(s) should be set to their lowest setting.
2. After all configuration settings are complete, power up the device (/SHDN\ = 1).
3. Enable any analog outputs that are part of the desired configuration.
4. Disable the mute on each respective analog output.

Ramp the volume up, one register step at a time, from the minimum setting until the desired volume (gain) is reached (this sequence is part of the example in Table 78).

Table 78: Device Startup Sequence

SEQUENCE	DESCRIPTION	REGISTERS
1	Set /SHDN\ = 0	0x45 (Default PoR State)
2	Configure Clocks	0x1B to 0x21
3	Configure Digital Audio Interface (DAI)	0x22 to 0x25
4	Configure Digital Signal processing (DSP)	0x17 to 0x1A, 0x26 to 0x28, 0x33 to 0x36, 0x41
5	Load Coefficients	0x46 to 0xBD
6	Configure Power and Bias Mode	0x42 to 0x44
7	Configure Analog Mixers	0x0D, 0x15, 0x16, 0x29, 0x2A, 0x2B, 0x2E, 0x2F, 0x37, 0x3A
8	Configure Analog Gain and Volume Controls. To Minimize Click and Pop for Analog Outputs, Enable Mute and Set the Output PGAs to the minimum gain setting.	0x0E to 0x11, 0x2B to 0x2D, 0x30 to 0x32, 0x38, 0x39, 0x3B, 0x3C
9	Configure Miscellaneous Functions	0x03, 0x12, 0x13, 0x14, 0x40
11	Set /SHDN\ = 1 (Power Up)	0x45
10	Enable Desired Functions	0x3D to 0x3F
11	Disable Mute on Analog Output Drivers	0x2C, 0x2D, 0x31, 0x32, 0x39, 0x3C
12	For all Analog Output Drivers, Ramp the Gain up One Volume Step per Write until the Desired Gain is Reached	0x30 to 0x32, 0x38, 0x39, 0x3B, 0x3C

While many configuration options and settings can be changed while the device is operating (/SHDN\ = 1), some registers should only be adjusted with the device in shutdown (/SHDN\ = 0). Table 79 lists the registers that should not be changed during active operation.

Table 79: Register Changes that Require /SHDN\ = 0

DESCRIPTION	REGISTER
Clock Control Registers	0x04, 0x05, 0x1B to 0x20
Bias Control	0x42 to 0x44
Digital Signal Processing Coefficients	0x46 to 0xBD

Component Selection

AC Coupling Capacitors

An input capacitor, C_{IN} , in conjunction with the input impedance of the MAX98090 line inputs forms a high pass filter that removes the DC bias from an incoming analog signal. The AC coupling capacitor allows the amplifier to automatically bias the signal to an optimum DC level. Assuming very low source impedance (comparatively), the -3dB point of the high pass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi \cdot R_{IN} \cdot C_{IN}}$$

Choose C_{IN} such that f_{-3dB} is well below the lowest frequency of interest. For best audio quality use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies. If needed, line output AC coupling capacitor values can be calculated in similar fashion by using the input resistance of the output stage connected to the line output drivers.

Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. Most surface mount ceramic capacitors satisfy the ESR requirement. For best performance over the extended temperature range, select capacitors with an X7R dielectric.

The value of the flying capacitor (connected between C1N and C1P) affects the output resistance of the charge pump. A value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of the flying capacitor reduces the charge-pump output resistance to an extent. Above 1μF, the on-resistance of the internal switches and the ESR of external charge pump capacitors dominate.

The holding capacitor (bypassing HPVSS) value and ESR directly affect the ripple at HPVSS. Increasing the capacitor's value reduces output ripple. Likewise, decreasing the ESR reduces both ripple and output resistance. Lower capacitance values can be used in systems with low maximum output power levels. See the Output Power vs. Load Resistance graph in the Typical Operating Characteristics for more information.

Filterless Class D Speaker Operation

Traditional Class D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filters add cost, increase the solution size of the amplifier, and can decrease efficiency and THD+N performance. The traditional PWM scheme uses large differential output swings (2 x SPKVDD peak to peak) and causes large ripple currents. Any parasitic resistance in the filter components results in a loss of power, lowering the efficiency.

The IC does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. Eliminating the output filter results in a smaller, less costly, and more efficient solution.

Because the frequency of the IC's output is well beyond the bandwidth of most speakers, voice coil movement due to the square-wave frequency is very small. Although this movement is small, a speaker not designed to handle the additional power can be damaged. For optimum results, use a speaker with a series inductance > 10μH. Typical 8Ω speakers exhibit series inductances in the 20μH to 100μH range.

EMI Considerations and Optional Ferrite Bead Filter

Reducing trace length minimizes radiated EMI. On the PCB, route SPKLP/SPKLN and SPKRP/SPKRN as differential pairs with the shortest trace lengths possible. This will minimize trace loop area, and thereby the inductance of the circuit. If filter components are used on the speaker outputs, minimize the trace length from any ground tied passive components to SPK_GND to further minimize radiated EMI.

In applications where speaker leads exceed 20mm, additional EMI suppression can be achieved by using a filter constructed from a ferrite bead and a capacitor to ground (Figure 25). Use a ferrite bead with low DC resistance, high frequency (>600MHz) impedance between 100Ω and 600Ω, and rated for at least 1A. The capacitor value varies based on the ferrite bead chosen and the actual speaker lead length. Select a capacitor less than 1nF, with the value based upon optimizing EMI performance.

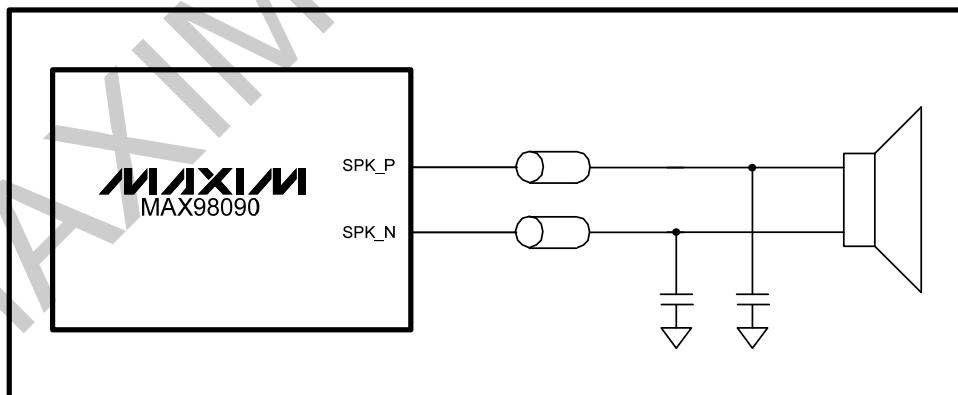


Figure 25. Optional Class D Ferrite Bead Filter

RF Susceptibility

GSM radios transmit using time-division multiple access (TDMA) with 217Hz intervals. The result is an RF signal with strong amplitude modulation at 217Hz and its harmonics that is easily demodulated by audio amplifiers. The MAX98090 is designed specifically to reject RF signals; however, PCB layout has a large impact on the susceptibility of the end product.

In RF applications, improvements to both layout and component selection decreases the MAX98090's susceptibility to RF noise and prevent RF signals from being demodulated into audible noise. Trace lengths should be kept below 1/4 of the wavelength of the RF frequency of interest. Minimizing the trace lengths prevents them from functioning as antennas and coupling RF signals into the MAX98090. The wavelength (λ) in meters is given by: $\lambda = c / f$ where $c = 3 \times 10^8$ m/s, and f = the RF frequency of interest.

Route audio signals on middle layers of the PCB to allow ground planes above and below to shield them from RF interference. Ideally the top and bottom layers of the PCB should primarily be ground planes to create effective shielding.

Additional RF immunity can also be obtained by relying on the self-resonant frequency of capacitors, as it exhibits a frequency response similar to a notch filter. Depending on the manufacturer, 10pF to 20pF capacitors typically exhibit self resonance at RF frequencies. These capacitors, when placed at the input pins, can effectively shunt the RF noise at the inputs of the MAX98090. For these capacitors to be effective, they must have a low-impedance, low-inductance path to the ground plane. Avoid using micro-vias to connect to the ground plane as these vias do not conduct well at RF frequencies.

Supply Bypassing, Layout, and Grounding

Proper layout and grounding are essential for optimum performance. When designing a PCB for the MAX98090, partition the circuitry so that the analog sections of the MAX98090 are separated from the digital sections. This ensures that the analog audio traces are not routed near digital traces.

Use a large continuous ground plane on a dedicated layer of the PCB to minimize loop areas. Connect AGND, DGND, and HPGND directly to the ground plane using the shortest trace length possible. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents any digital noise from coupling into the analog audio signals.

Ground the bypass capacitors on MICBIAS, VCM and REF directly to the ground plane with minimum trace length. Also be sure to minimize the path length to AGND, and bypass AVDD directly to AGND. Connect all digital I/O termination to the ground plane with minimum path length to DGND, and bypass DVDD and DVDDIO directly to DGND.

Place the capacitor between C1P and C1N as close to the MAX98090 as possible to minimize trace length from C1P to C1N. Inductance and resistance added between C1P and C1N reduce the output power of the headphone amplifier. Bypass HPVDD, CPVDD and CPVSS with capacitors located close to the pin with short trace lengths to HPGND. Close decoupling of CPVDD and CPVSS minimizes supply ripple and maximizes output power from the headphone amplifier.

HPSNS senses ground noise on the headphone jack and adds the same noise to the output audio signal, thereby making the output (headphone output – ground) noise free. Connect HPSNS to the headphone jack shield to ensure accurate pickup of headphone ground noise.

Bypass SPK_VDD to SPK_GND with the shortest trace length possible and connect SPKLP, SPKLN, SPKRP, and SPKRN to the stereo speakers using the shortest traces possible. If filter components are used on the speaker outputs, be sure to locate them as close to the MAX98090 as possible to ensure maximum effectiveness.

Route microphone signals from the microphone to the MAX98090 as a differential pair, ensuring that the positive and negative signals follow the same path as closely as possible with equal trace length. When using single-ended microphones or other single-ended audio sources, ground the negative microphone input as near to the audio source as possible and then treat the positive and negative traces as differential pairs.

An evaluation kit (EV Kit) is available to provide an example layout for the MAX98090. The EV Kit allows quick setup of the MAX98090 and includes easy-to-use software allowing all internal registers to be controlled.

Recommended PCB Routing

The IC uses a 49-bump WLP package. Figure 26 provides an example of how to connect to all active bumps using 3 layers of the PCB. To ensure uninterrupted ground returns, use layer 2 as a connecting layer between layer 1 and layer 2 and flood the remaining area with ground.

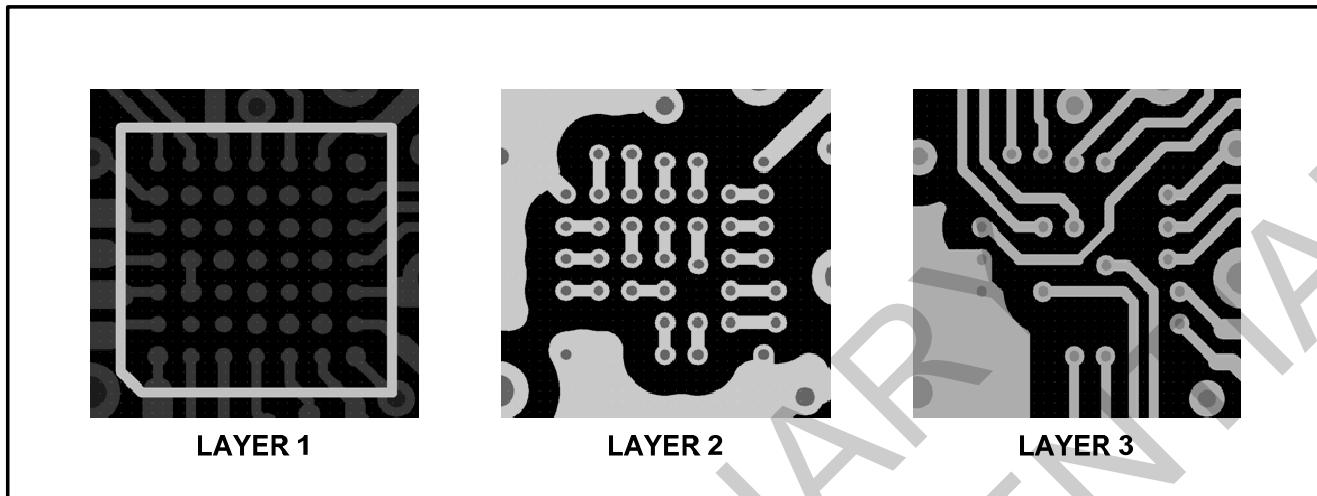


Figure 26: WLP Package Suggested Routing for MAX98090

Unused Pins

Table TBD shows how to connect the IC pins when circuit blocks are unused.

WLP Applications Information

For the latest application details on WLP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the *Application Note: UCSP - A Wafer-Level Chip-Scale Package* on Maxim's website at www.maxim-ic.com/ucsp. Figure 27 shows the dimensions of the WLP balls used on the MAX98090.

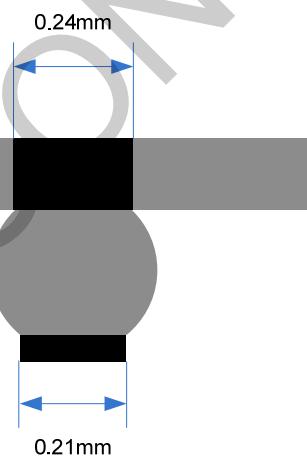
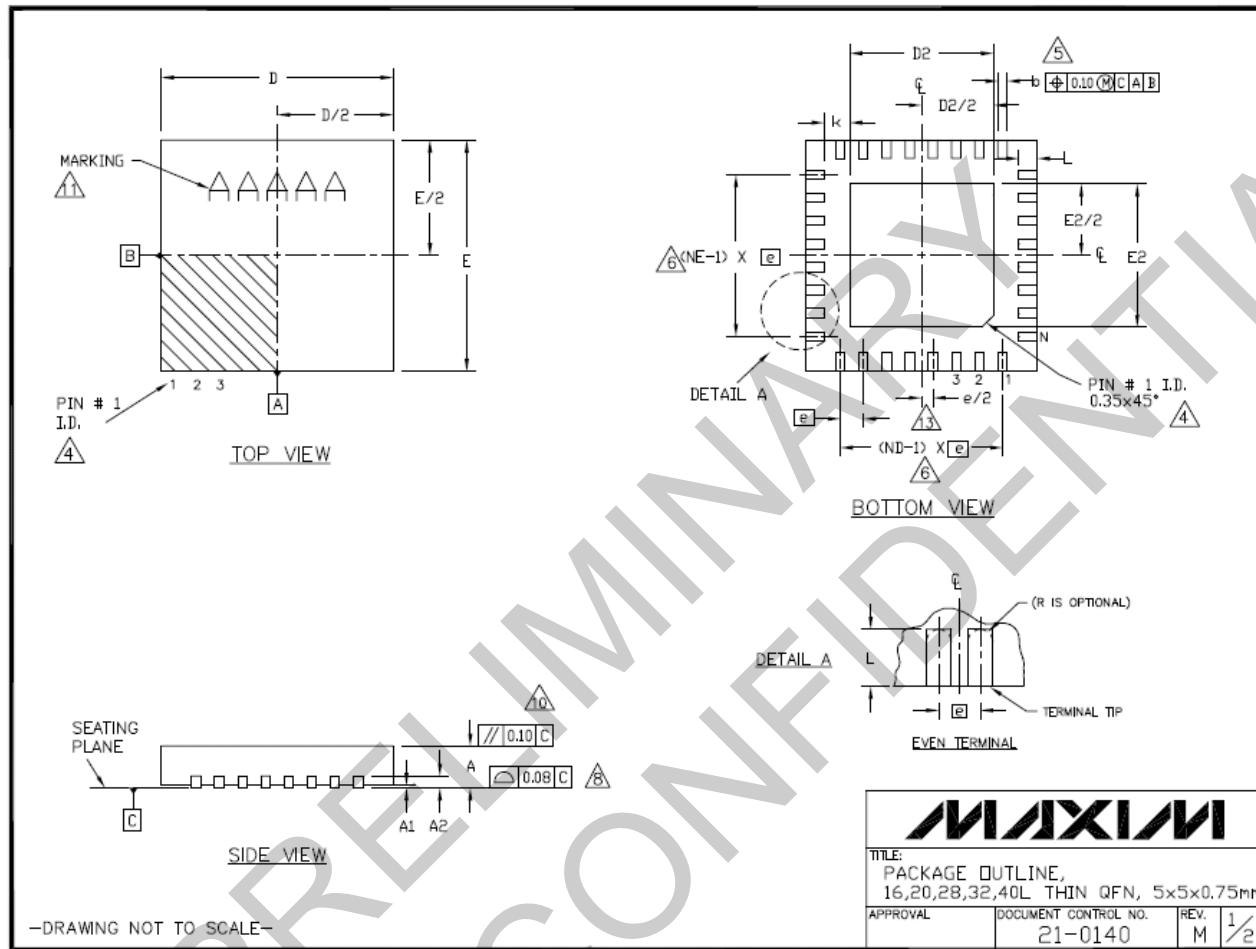


Figure 27: MAX98090 WLP Ball Dimensions

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
49 - WLP	W493B3+2	21-0443
40 - TQFN	T4055+1	21-0140



COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.												
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20	REF.	0.20	REF.	0.20	REF.	0.20	REF.	0.20	REF.	0.20	REF.	0.20	REF.	0.20
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80	BSC	0.65	BSC	0.50	BSC	0.50	BSC	0.40	BSC	0.40	BSC	0.40	BSC	0.40
K	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

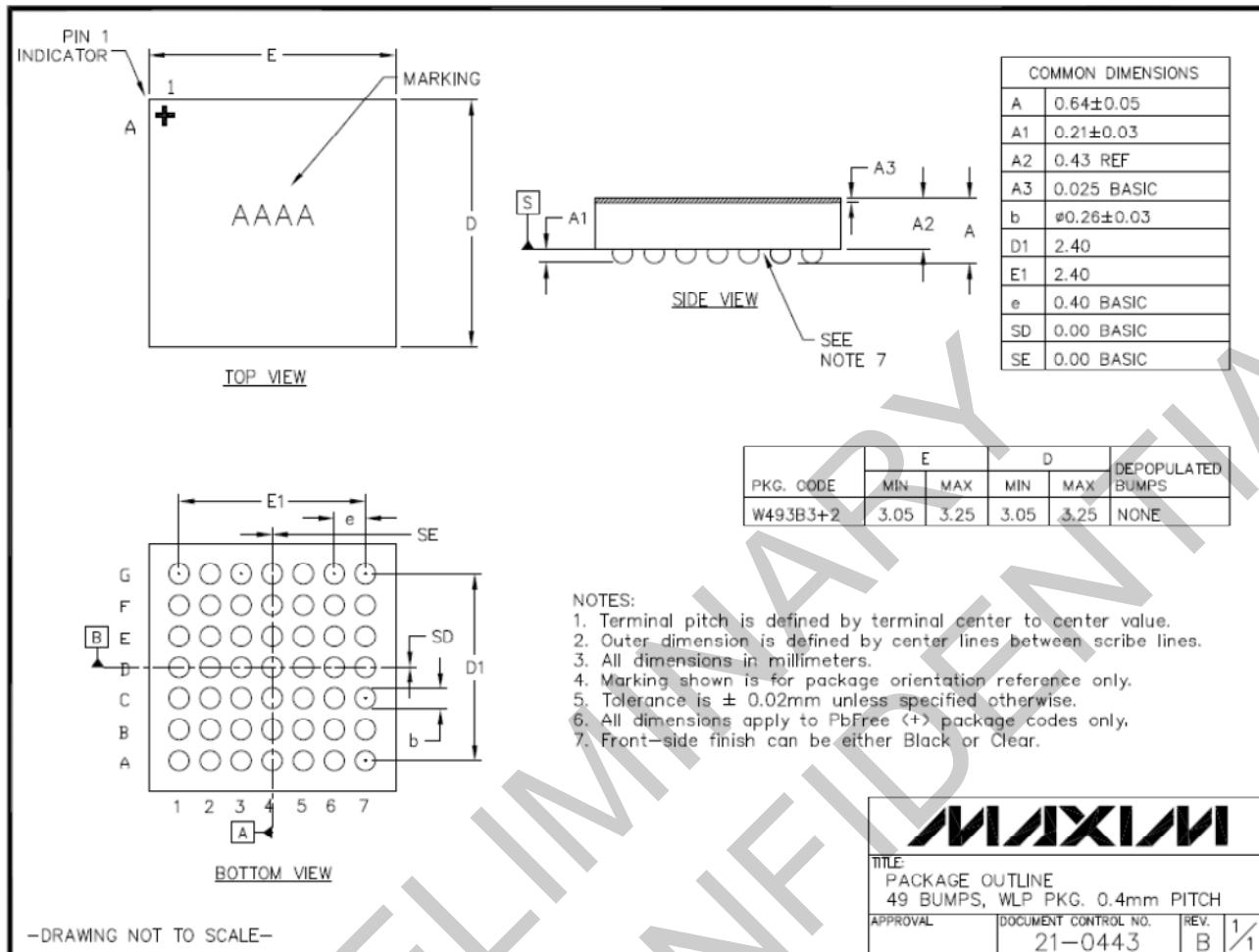
NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

EXPOSED PAD VARIATIONS						
PKG. CODES	D2		E2			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655-4	2.19	2.29	2.39	2.19	2.29	2.39
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.45	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055N-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

MAXIM	
TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.75mm	
APPROVAL	DOCUMENT CONTROL NO.
	REV. M
	21-0140
	2/2



REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0.1		Initial draft release	—
0.5		Second draft release	Significant updates
0.6		Third draft release	Significant updates
0.7		Fourth draft release	Significant updates
0.8		Fifth draft release (Front Page, EC table, TOC, Register Map and Description, Applications Information, Etc. Updates)	Significant updates

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