A Voltage Variable Attenuator Using Silicon PIN Diodes and a Passive GaAs MMIC in a Plastic SMT Package

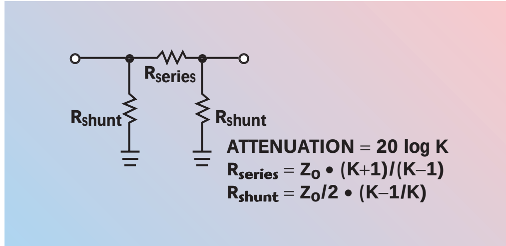
A unique voltage variable attenuator (VVA) has been developed for the commercial wireless market. The device has linear operating power and intercept points higher than GaAs FET-based VVAs. The design uses mixed technology, a gallium arsenide MMIC and silicon PIN diodes. The operating frequency is selected in the 900 to 2500 MHz frequency band by defining the length of a quarter-wave-long transmission line. The entire assembly is manufactured in a plastic, SO-8, surface-mount package.

VVA OPERATION

The attenuator has one input and output with the capability to select any attenuation level within its dynamic range. The level of attenuation is determined by the voltage and current supplied to the device. The attenuator is absorptive, has low SWR versus attenuation, and is linear and monotonic.

The basic π attenuator, along with its design equations, are shown in ***Figure 1***. In the following equations, K is defined as the input to output voltage ratio and Z_o is the system characteristic impedance. The values of the resistors for common values of attenuation in a 50 Ω

Fig. 1 Ideal π attenuator.



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system have been calculated and are listed in ***Table 1***.

If the fixed resistors in the ideal π attenuator are replaced with variable resistors a variable attenuator is obtained. This concept is shown in ***Figure 2*** where the series resistor is replaced by a PIN diode and the shunt resistors are replaced by a series resistor and PIN diode. The attenuator basically functions as a continuously variable π pad with the diodes acting as the resistors. When the diode's series resistance changes the resulting impedance provides the equivalent of a variable π attenuator from 0 to 20 dB.

The operation of the circuit is explained by an example where the desired attenuation value is equal to 20 dB. The diodes are forward biased to a level where their series resistance R_s is equal to approximately 247 Ω. If this impedance is normalized to the system impedance of 50 Ω, plotted on a Smith Chart and rotated the length of the quarter-wave transmission line, 90°, the resulting normalized impedance is 0.20 Ω. If the value is un-normalized and added to the 50 Ω circuit resistor the equivalent shunt impedance of 60 Ω is obtained. The same methodology is used for all the resistor values. When the diodes are forward biased the maximum value of attenuation is limited by the value of the fixed resistor.

Since the series-shunt diode R_s impedance combination does not always equal the ideal π attenuator impedance values, some degradation in return loss occurs through the attenuation range. This degradation can be observed in the following plots where the best return loss occurs at the attenuation levels that closely match the ideal circuit values. ***Figure 3*** shows the attenuation for an ideal attenuator versus the attenuation for the equivalent π attenuator using PIN diodes. ***Figure 4*** shows the return loss for the equivalent PIN diode π attenuator for the various attenuation levels.

When a forward current of 10 mA is applied, the diode's R_s is low, the R_{series} attenuator value is less than 1 Ω, the shunt impedance is very high and the VVA is in the insertion loss state. With zero volts applied the diode behaves as a high impedance, the R_{series} impedance is high and the VVA demonstrates high attenuation. Similarly the diode shunt impedance is high, reflecting as a low impedance to ground at the circuit resistors. With the input and output terminated in essentially 50 Ω the attenuator SWR is low.

TABLE I

IDEAL π ATTENUATOR RESISTOR VALUES

Attenuation (dB)	R_{series} (Ω)	R_{shunt} (Ω)
3	17.6	292.4
6	37.4	150.5
10	71.2	96.3
15	136.1	71.6
20	247.5	61.1
25	443.2	55.9

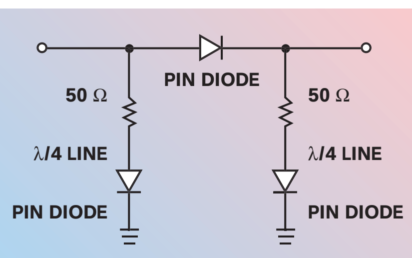

Fig. 2 Equivalent PIN diode π attenuator.

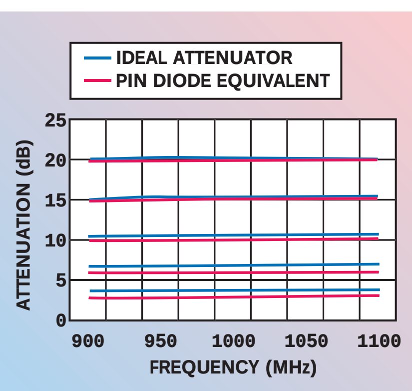

Fig. 3 Attenuator levels for ideal π attenuator vs. PIN diode equivalent π attenuator.

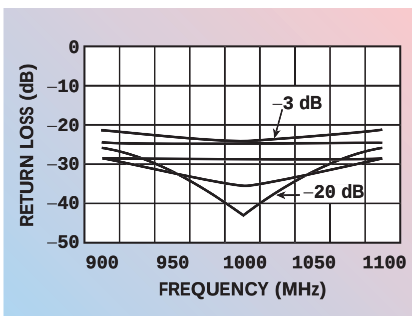

Fig. 4 Return loss for PIN diode equivalent π attenuator vs. attenuation levels.

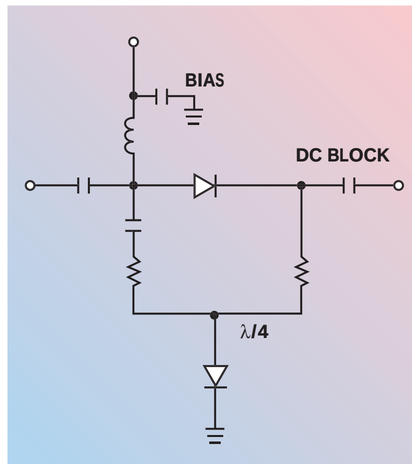

Fig. 5 Final VVA schematic.

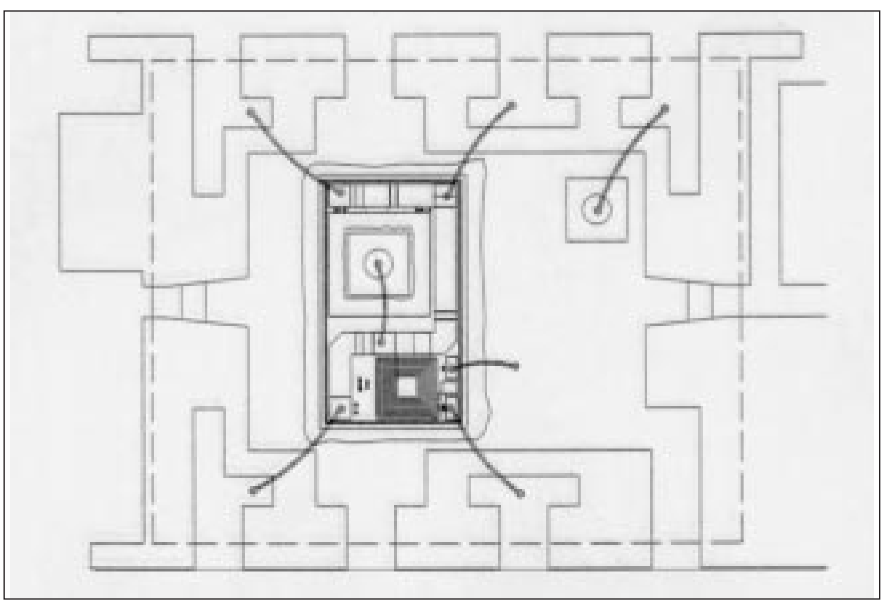

Fig. 6 VVA plastic package assembly.

The final VVA circuit shown in ***Figure 5*** was implemented. DC blocks have been added to the circuit to isolate the bias from other parts of the system. The capacitor values must be large enough to minimize the RF loss yet small enough to be realizable as part of the MMIC. The inductor and bypass capacitor combine to form the bias network. The inductance must be large enough to prevent loss of RF energy in the bias circuit and to minimize reflection losses. Its size also has a direct impact on the size of the MMIC. The quarter-wave component is a 50 Ω coplanar waveguide grounded transmission line placed external to the package.

The plastic packaged assembly of the VVA is shown in ***Figure 6***. The MMIC is a 250 μm thick passive GaAs circuit consisting of the capacitors, resistors and inductor. The lead frame is an eight-lead small outline package per JEDEC specification MS-012AA. The PIN diodes and MMIC are epoxy die attached to the lead frame. The components are interconnected with bonded gold wire.

The PIN diodes were selected to obtain high third-order intercept (IP3) performance, an attribute attractive to multi-channel communications system architecture. The key parameters of the diode are a thick intrinsic region, long carrier lifetime and low series resistance.

The quarter-wave transmission line required to set the operating frequency consists of a portion of the MMIC, the bond wire length, the lead frame and the coplanar waveguide (CPW) line on the printed circuit board. The actual printed line is not 90° but 90° minus the plastic packaged internal components. To determine the electrical length of the plastic packaged internal components and leads the following methodology was used. A VVA was mounted on the printed circuit board shown in ***Figure 7*** and the frequency where the maximum attenuation occurred measured as a function of the physical length of the CPW line. The electrical length of the printed transmission line was computed and the graph shown in ***Figure 8*** generated. The plot shows the equivalent electrical length of the internal components across the operating band.

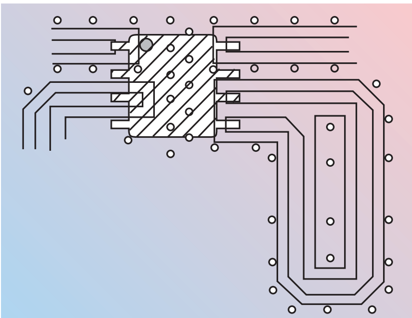

Fig. 7 VVA test board.

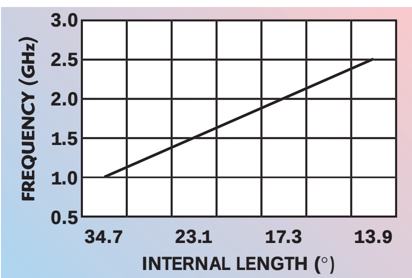

Fig. 8 Internal package electrical length vs. operating frequency.

TABLE II

VVA TEST BOARD DATA, FREQUENCY 1.9 GHz, BANDWIDTH ±5%

Parameter	Test Conditions	Minimum	Typical	Maximum
Insertion loss (dB)	10 mA	—	1.2	1.5
SWR	0 to 20 dB	—	1.8	2.0
Attenenuation vs. bias (dB)	30 to 880 μA, 0 V	25	28 (see Figure 9)	
Attenuation flatness (dB)			0.15	0.30
Switching speed (μs)	50% control to 90% RF	—	2	5
Linear operation (dBm)	0 to 20 dB	—	+17	+15
Input IP3 (dBm)	two tone inputs to –5 dBm	+40	see Figure 10	

MEASURED PERFORMANCE

The VVAs were characterized using the test board. A summary of the parameters and test data is listed in ***Table 2*** across a 10 percent bandwidth. Key performance parameters of the VVA are shown in ***Figures 9*** and ***10***. The input IP3 point is 15 to 20 dB higher than commercially available FET-based VVAs based on a survey of suppliers.

CONCLUSION

A unique voltage variable attenuator, part number AT65-0008, has been developed for the commercial wireless market using mixed technology, a GaAs MMIC and silicon PIN diodes, to achieve high intercept points. The VVA has intercept points higher than GaAs FET-based VVAs. The methodology of selecting the operating frequency by defining the length of a quarter-wave transmission line has been described. The SO-8 SMT assembly has been illustrated and test data presented with the VVA mounted on a soft substrate printed wiring board.

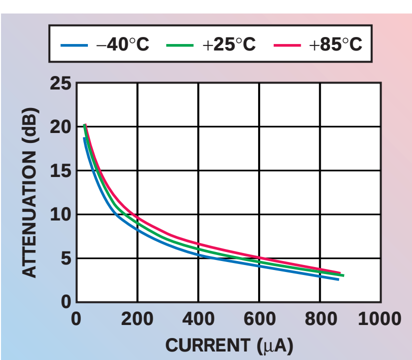

Fig. 9 Attenuation vs. current and temperature at center frequency.

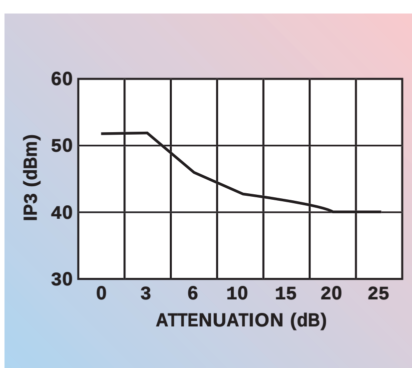

Fig. 10 Intercept point vs. attenuation.

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