APPENDIX - A

PIN DIODE PHYSICS

NOTES

APPENDIX A INTRODUCTION

Appendix A addresses a variety of PIN diode physics topics that may be of interest to circuit designers who wish to probe more thoroughly into such issues as: how a PIN diode controls large values RF current with relatively small values of d-c current (sometimes referred to as "current gain"), what is minority carrier lifetime and how is it related to stored charge (Qs), why might the turn-off time (TRF) of a PIN diode be longer than the "turn-on" time (TFR), and why is the large signal operation of a PIN diode different in the microwave bands than in HF band?

Chapter 1 contains just enough preliminary information about PIN diodes so that Chapters 2 through 5 can be understood. Chapters 2 through 5 are written so that the circuit designer can focus on the specific control circuit function being described. It was felt that the introduction of some of these physics topics in Chapters 2 through 5, would distract many readers from the main focus of a particular chapter.

Appendix A is not meant to be a substitute for a text on semiconductor device physics. The treatment of the above topics varies in thoroughness, but references to the literature are given for those who wish to delve more deeply into a particular issue. Some physics topics are discussed in other appendices also.

Appendix B compares PIN diode circuit characteristics to those of pn-junction devices.

Appendix E discusses the topic of signal distortion in PIN diodes.

I SOME CHARACTERISTICS OF THE PIN DIODE I-REGION

Since the presence of the relatively wide intrinsic layer in a PIN diode is responsible for its unique properties, it is worthwhile discussing the I-layer first and then its characteristics, such as lifetime and stored charge. In fact, the equivalent circuit parameters, the switching times, and the distortion characteristics of the PIN diode are dependent on the properties of the I-layer as well.

Ideally, it is desirable for the I-layer to be intrinsic (the Silicon crystal structure is completely free of chemical impurities or crystal growth imperfections). With an intrinsic I-layer, the RF loss of the PIN diode under reverse bias would be minimized and its Capacitance would vary the least with reverse bias or frequency.

In reality, a truly intrinsic layer is not achievable within a PIN diode structure because it is not feasible to maintain intrinsic resistivity in the I-layer throughout the processing steps of the diode. Thus the concept of p+ and n+ layers separated by an intrinsic layer is somewhat artificial. Microsemi P-I-N diodes have I-layer resistivities of 8,0000 to 12,000 Ohm-cm, either slightly p-type (π) or slightly n-type (ν). These are much lower loss devices than competitive devices with much lower values of I-layer resistivity.

The ideal PIN diode has no impurities in its I-layer. Thus, at zero bias, the I-layer is already depleted of carriers. Since there are no mobile carriers in the I-layer to support current flow, the diode is an open circuit to RF signals and its Capacitance does not vary with reverse voltage or frequency.

A practical PIN diode has some space charge in its I-region, due to the presence of impurities. Some reverse bias is required to deplete its I-region of mobile charge. The value of reverse bias at which the space charge in depleted is referred to as the swept-out or "punch through" voltage. It is important to bias a PIN diode beyond the swept-out voltage for most RF applications, since current flow by these mobile carriers constitute an unwanted source of signal loss and noise.

The desired electrical parameters from the use of "intrinsic" silicon are off set by the difficulty of passivating such high resistivity silicon. The impurity level of 10,000 Ohm-cm P-type silicon is 1 impurity atom in approximately 30 billon silicon atoms and it has to be boron (P-type)! This is what makes the passivation process so difficult.

II MINORITY CARRIER LIFETIME

The volume or bulk lifetime in semiconductor is defined [1] as the average time interval between the generation and the recombination of minority carriers in a homogeneous semiconductor. Carriers are constantly being generated thermally in the bulk Silicon [2]. The generation rate is a function of the ambient temperature of the Silicon. Carriers can also be introduced into the bulk Silicon by connecting a Voltage source across the PIN diode junctions. There are two recombination mechanisms that determine the effective lifetime of a semiconductor device.

III RECOMBINATION PROCESSES

BULK RECOMBINATION

The fundamental effect that limits the lifetime in the bulk Silicon is the thermal-equilibrium condition, $pn = n_i^2$, where n_i is the free carrier density in the bulk Silicon at the ambient temperature. The basic recombination process is band-to-band recombination where an electron-hole pair recombines. Some bulk recombination also occurs via recombination centers or traps [2].

SURFACE RECOMBINATION

On the surfaces of the Silicon, nearly the entire recombination process is due to the presence of surface states or traps on the surface. Surface recombination velocity determines the minority carrier lifetime near the Silicon surfaces. Effective device lifetime is determined by the relationship

$$1 / \tau_{effective} = 1 / \tau_{bulk} + 1 / \tau_{surface}$$

IV CHIP GEOMETRY

The PIN diode chip structure is shown in Figure A.1. When the PIN diode wafer is processed, the bulk I-layer may have a minority carrier lifetime [1] somewhere in the range of 1 μs to perhaps 10 ms. This wide range of possible values of lifetime (τ) is related to the particular details of the Silicon wafer processing steps. The lifetime of a PIN diode obtained from the wafer will be much less than that of the wafer.

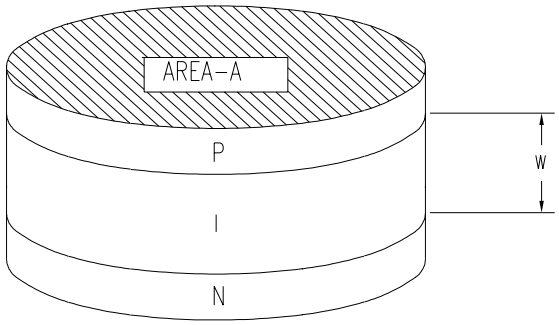

Figure A.1 PIN Diode Chip Structure

The geometry (ie, volume) of the I-region determines the bulk lifetime and is a major factor affecting the effective lifetime of a finished device [3]. The I-region is cylindrical in shape (Figure A.1). The areas of the outer surface also degrade (decrease) minority carrier lifetime. Because the periodicity of the I-region Silicon stops at these surfaces, the rate at which electrons and holes recombine is higher at these surfaces than at the center of the I-region. Figure A.2 shows contours of effective lifetime in Silicon as a function of the mesa (I-region) diameter.

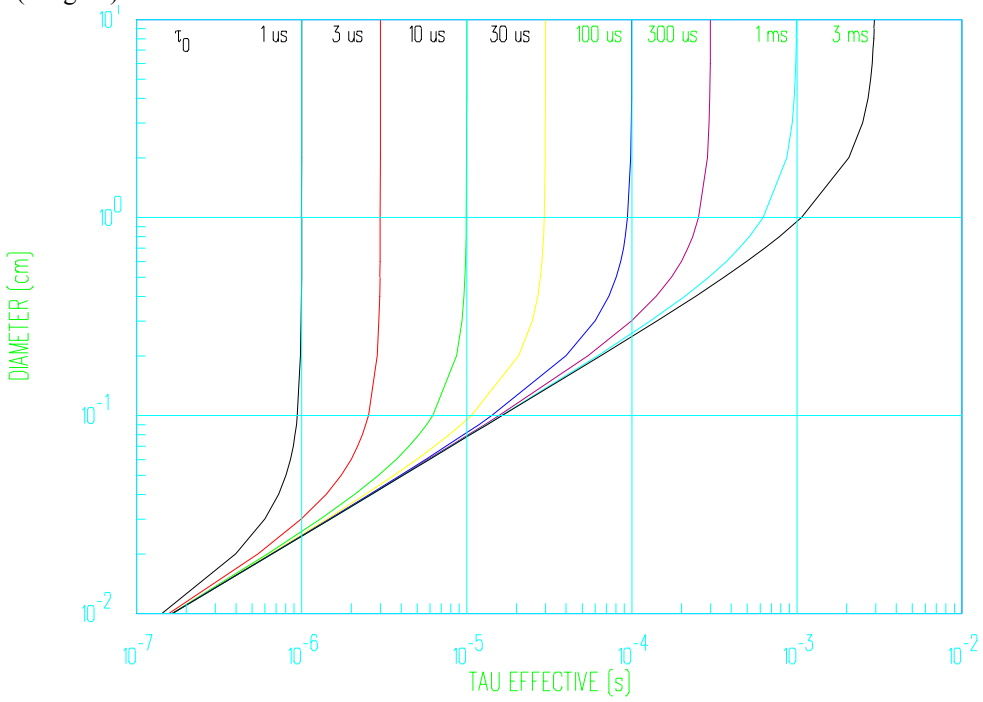

Figure A2. Effective Lifetime vs Mesa Diameter

V STORED CHARGE

When the PIN diode is forward biased, electrons and holes are injected into the I-region, where they have a finite lifetime before they recombine. The charge density in the intrinsic region and its geometry determine the resistance of the device. Lifetime determines the approximate low frequency limit of useful operation.

The diode's resistance is proportional to the stored charge. The charge is related to the diode current by

$$I_f = dQ/dt + Q/\tau$$

where I_f = diode forward current, Q = charge stored in the diode, and ☺ = effective recombination lifetime

If the diode is biased with only a constant current, the stored charge is constant and is equal to

$$Q = I_f \tau$$

At frequencies below $f_O = 1/2\pi\tau$ the RF signal modulates the stored charge the same as the dc bias and the PIN diode behaves as an ordinary PN diode.

VI FORWARD BIAS SERIES RESISTANCE (R_S)

The forward biased PIN diode behaves as a current controlled resistor that presents a linear resistance to the flow of RF current through the diode. This is the property of a PIN diode that enables the device to be used as the RF power control element in linear attenuators and modulators.

The forward bias equivalent circuit of a PIN diode, Figure A.3, consists of the forward bias resistance (Rs) in series with a fixed series inductor (Ls). Rs can be varied over a range of a few tenths of an Ohm to 100,000 Ohms by a direct or low frequency control current.

Figure A.3 Forward Bias Equivalent Circuit

The ideal diode equation, with any external voltage due to R_S subtracted from the junction voltage, is

$$I = I_O[e^{-q\,(V-IRs)\,/nkt} - 1] \quad \text{“ideal diode equation”}$$

where n = 1 if the diode's space charge is diffusion limited and n = 2 if the space charge is recombination limited. Typical rectifiers have n = 1.0 to 1.5 and typical PIN diodes have n = 1.8 to 2.0.

The dc forward voltage characteristics of rectifiers have been extensively treated by Herlet, Benda, and Spenke [4,5]. Both articles do not provide a closed form solution similar to the “ideal diode equation”; however computer programs have been written to utilize their solutions.

At low frequency the resistance of the diode is

$$R_j = nkT/qI_{dc} \quad \text{Ohms}$$

where n = 2 for a well constructed PIN diode.

At room temperature

$$R_j = 52/I_{dc(mA)} \quad \text{Ohms}$$

The total resistance of a PIN diode is made up of R_j and any other series resistance contained in the chip (Ohmic contacts, diffusion layers, or substrate resistance) and resistance of the package and its leads. At frequencies above the dielectric cutoff frequency ($f > f_o$), the PIN diode I-layer's resistance is nearly linear [Appendices B & E]. The resistance of the I-layer is given by [6]

$$R_I = W^2/(2\mu_{a\,p}\tau\, I_f)$$

where $\mu_{a\,p}$ is the ambipolar diffusion constant, W is the I-layer width, and τ is the lifetime in the I-layer

R_I does not contain the I region area explicitly but only the I-layer width. Since τ is a parameter that is I-layer geometry dependent, the I-layer resistance implicitly depends on the area as well.

VII CAPACITANCE

The reverse bias equivalent circuit, Figure A.4, consists of the shunt combination of the I-layer capacitance (Ct) and parallel resistance (Rp) in series with the inductance (Ls). The reactance and resistance of the depleted I-layer are represented by Ct and Rp. Ct contains the stray capacitance due to the effects of the diode's package structure as well as the junction capacitance (Cj).

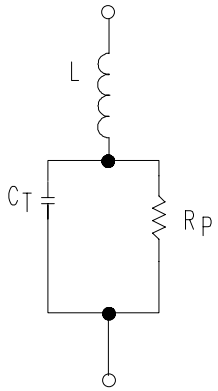

Figure A.4 Reverse Bias Equivalent Circuit

Due to the structure of a N+ and P+ section separated by an I-layer, the N+ and P+ sections accumulate charge. A thin depleted layer with no charge occurs. This layer acts as a parallel plate capacitor (Cj).

$$Cj = \varepsilon_r \varepsilon_o A / W$$

where W varies with the reverse bias voltage.

A well designed low frequency PIN diode will have a flat Capacitance versus Reverse Voltage curve even at low frequency. Figure A.5 shows such a PIN diode with a flat curve to below 4 MHz.

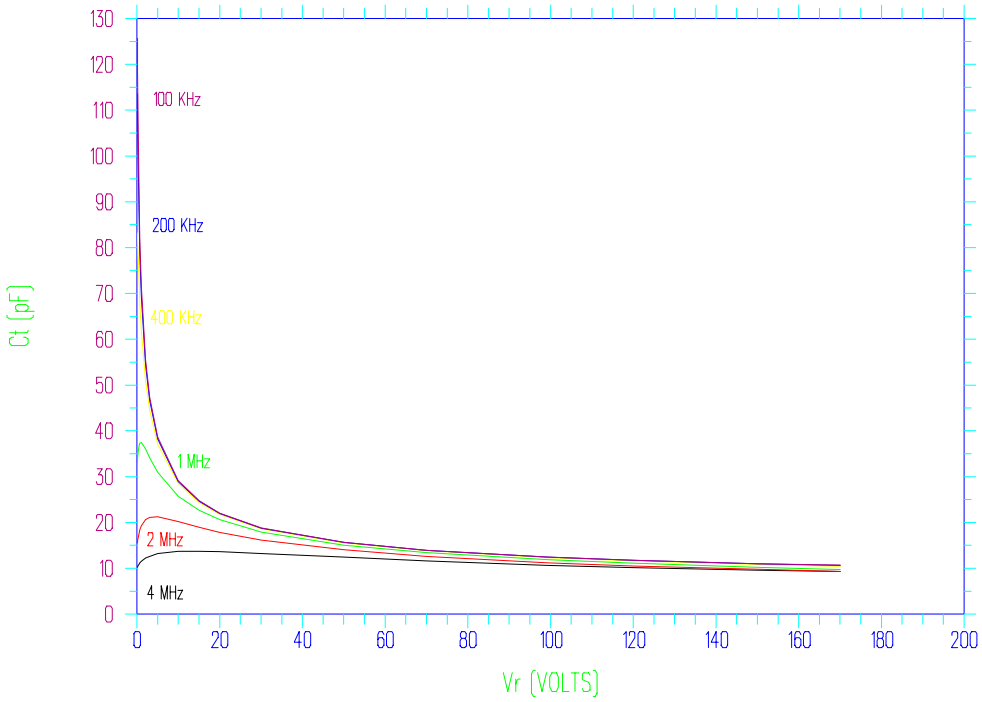

Figure A.5 PIN Diode Capacitance vs Reverse Bias Voltage and Frequency

VIII REVERSE BIAS PARALLEL RESISTANCE (Rp)

The reverse bias equivalent circuit, Figure A.4 shows the shunt loss element (Rp) associated with the PIN diode's total capacitance (Ct). This is the industry's conventional representation of the loss element of a reverse biased capacitor. So zero bias shunt loss is represented by an Rp whose value is infinity (ie, an open-circuit).
A series representation would serve just as well as the shunt representation, and might lend some intuitive insight (zero loss would be represented by a series element whose value is zero!). Reference [7] is an authoritative text on Varactor Applications. Varactors are only useful devices when reverse biased. The main premise of reference [7] is the ease with Varactor circuits can be analyzed if the series representation of the Varactor loss is used.
An ideal PIN structure (Section I, above) would have no shunt loss, because there are no mobile carriers in the I-layer to support conductive current. In practical PIN diode structures, Rp is highly dependent on the wafer processing steps and on passivation of the cylindrical surface of the diode chip prior to packaging. A well passivated PIN diode would have an Rp in excess of 50,000 Ohms when back biased beyond the punch through voltage.

IX REVERSE BIAS EQUIVALENT CIRCUIT

Figure A.6 gives the reader an intuitive feel for the connection between the PIN diode chip model and the reverse bias equivalent circuit. It also shows both the high frequency (microwave bands) and the low frequency (HF band) paths through the model [8].

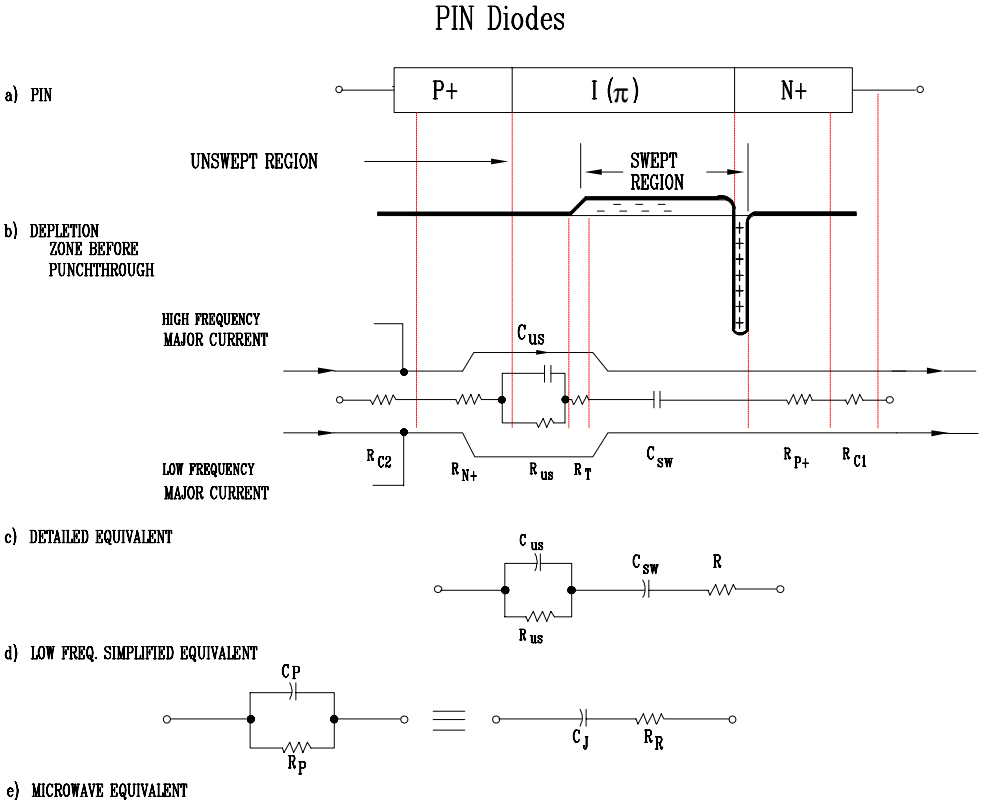

Figure A.6 Reverse Bias Equivalent Circuit

Microsemi's unique passivation process produces very low leakage and very stable reverse characteristics in which the device may be driven hard into reverse breakdown. In a 2 us pulse form currents

as large as 100 mA at approximately 3000 volts may be safely handled. Figure A.7 is a typical passivated high voltage PIN.

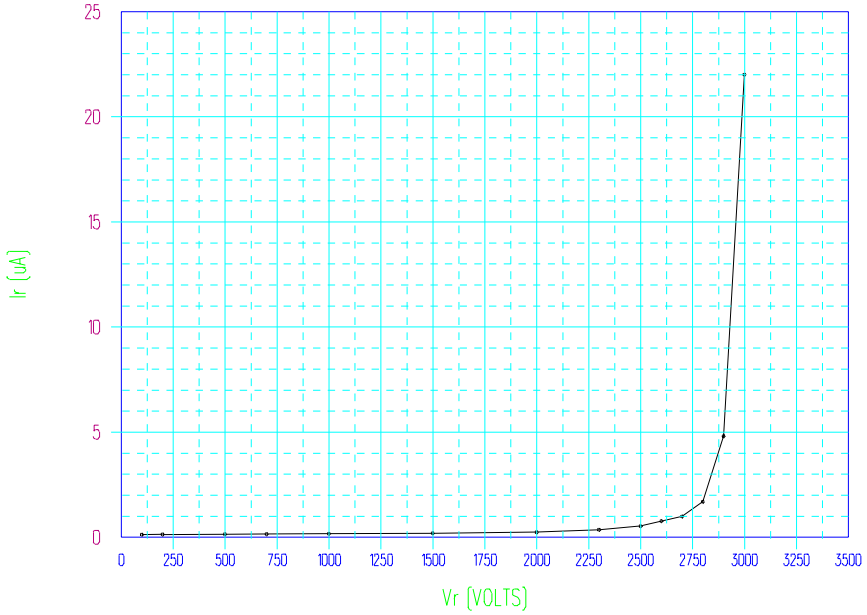

Figure A.7 TYPICAL PASSIVATED HIGH VOLTAGE PIN

X SWITCHING

Up to now the forward and reverse characteristics have been discussed separately. What happens when the PIN diode is switched[9,10]?

REVERSE BIAS TO FORWARD BIAS

The PIN diode, with sufficient reverse voltage to fully deplete the I-layer, will be depleted of mobile carriers. This depletion region will collapse almost instantly and the injection of carriers begins with a finite time to fill the I-layer with charge.

FORWARD BIAS TO REVERSE BIAS

The turn-off time is not a reverse of the turn-on time. When a large reverse bias is applied to a forward bias PIN diode a large current flows limited only by the impedance of the voltage source and the circuitry of the bias feed to the PIN diode. [The RF choke and the low pass filter to supply the bias current should have a very low dc impedance.] The edges of the die closest to the contacts deplete of charges quickly; however, the charges near the center of the die have to diffuse out to the external contacts. As more and more charges are removed, the reverse voltage across the I-layer begins to increase aiding the removal of the charges. By using spiked voltage drivers and by reducing the source impedance, the switching time for a diode can be substantially reduced. Figure A.8 shows the charges in the I-layer and their removal as a function of time.

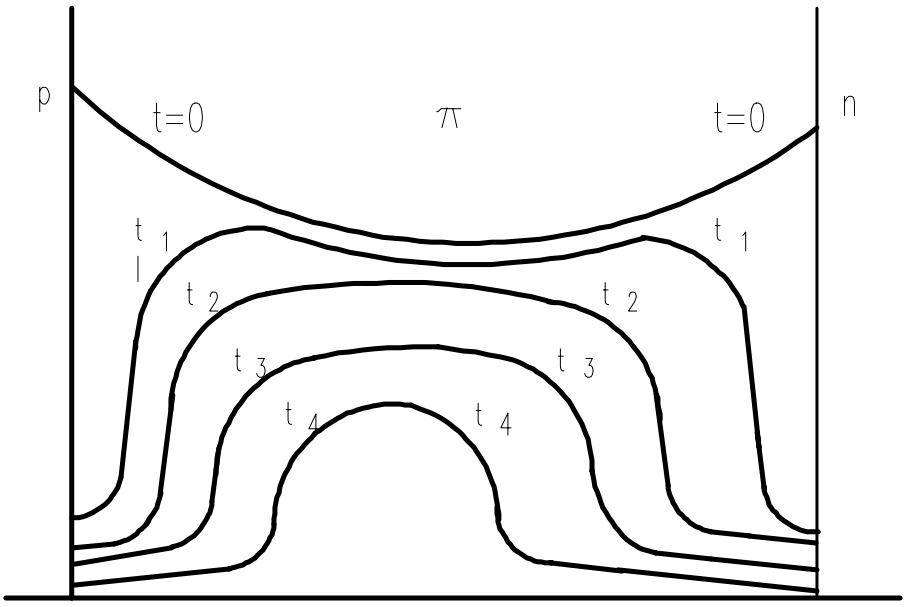

Figure A.8 Charge removal from chip versus time