6/24/2020

Name of Session

Gaunt, W. J.

**Design and Simulation of Low Power Time-Domain Current-Mode Analogue Neural Network architecture in 180nm CMOS**

Dr P. Georgiou

This project details a new method of on-chip signal processing, working towards a time domain input artificial neural network. The report introduces the elements that make up the simple perceptron model of the neuron, describing how the Multiply Accumulate operation is has been made using basic analogue building blocks, and a finite state machine is used to provide a time domain pulse to feed the signal forward. The second half of the report details an attempt to create a more complex artificial neural network in silico. Some time domain circuits of interest are also presented, some of which have been tested and verified.