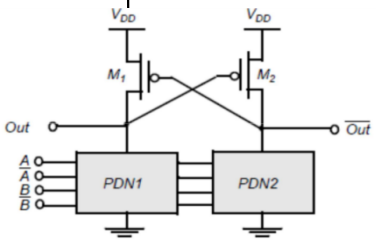
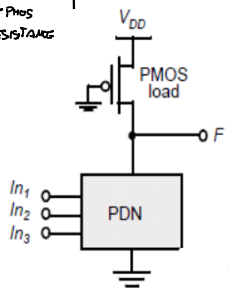
LOGIC IMPLEMENTATIONS

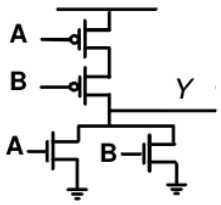
DCVSL
DIFFERENTIAL CASCODE VOLTAGE SWITCH LOGIC



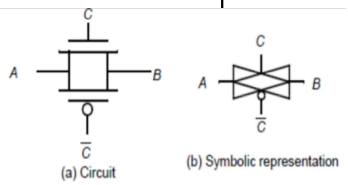
PSEUDO NMOS LOGIC
- $V_{OL} \neq 0$
- STATIC POWER WHEN PDN ACTIVE OF $P_{ST} = P(0) V_{DD} I_{PMOS}$
- PULL DOWN RESISTANCE FOR τ_P IS $R_{eqn} = \frac{R_n}{1 - \frac{R_n}{R_p}}$



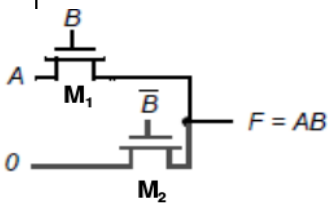
FULLY COMPLEMENTARY CMOS LOGIC
FC-CMOS



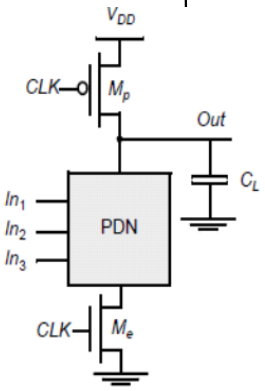
TRASMISSION GATE



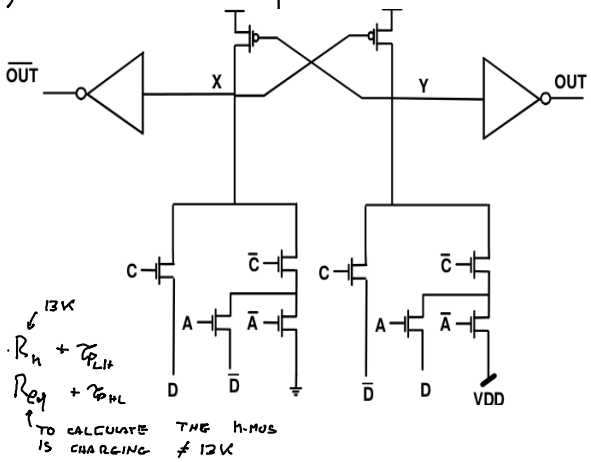
PASS TRANSISTOR LOGIC



DYNAMICS LOGIC



DIFFERENTIAL / COMPLEMENTARY PASS TRANSISTOR LOGIC
DPL / CPL



- $\tau_{LH} = ln(2) C_{INT} \cdot R_n + \tau_{PLH}$ (13K)
- $\tau_{HL} = ln(2) C_{INT} R_{eq} + \tau_{PHL}$

R_{eq} TO CALCULATE THE n-MOS IS CHARGING $\neq$ 13K